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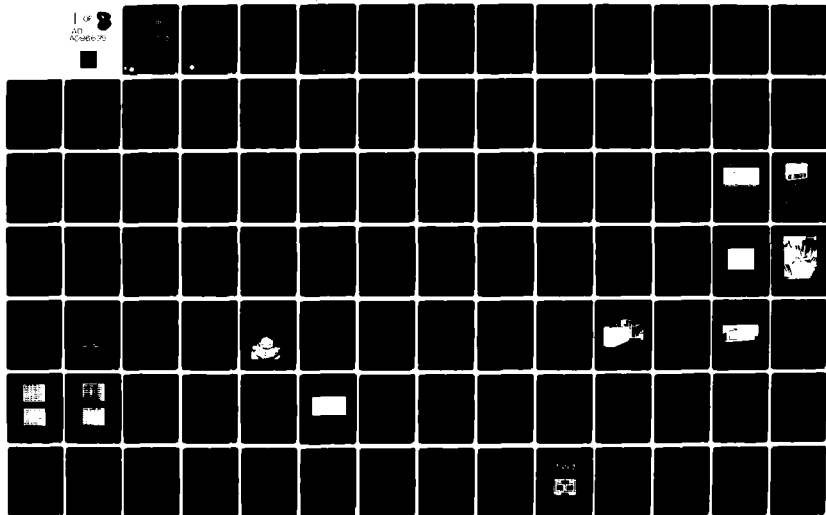
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L. J. Sienkiewicz, R. E. Stapleton, F. S. Youngk  
D. Leksell

Final Report  
Contract No. DAAB07-76-C-0027

LEVEL II

February 20, 1980

Electronics Research & Development Command  
U. S. Army  
Fort Monmouth, New Jersey 07703

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)  This final report describes the special requirements of the Department of Defense for lightweight, low power alphanumeric displays for field applications, with emphasis on a manufacturing approach to such displays. The prevailing technical philosophy of the related advantages of an active matrix of electroluminescent pixels driven by		



a matrix of switching elements featuring CdSe-based thin film transistors and its implementation is explained in the context of three phases of technical activity. The first is laboratory-scale verification, followed by two distinct prototype production efforts, the second formulated to eliminate problems and build on experience derived from the first. Both feature the so-called all-stencil mask approach wherein the switching matrix circuit is developed from a series of sequential vacuum depositions through metal aperture masks. All three program phases provide working displays featuring a powder phosphor medium whose operating temperature characteristics were markedly improved during the third program phase. Extensive and successful efforts applied to transistor synthesis during Program Phase II resulted in more than adequate and very reproducible transistor performance. Transistor design could be further optimized, particularly in regards to reducing the on-state impedance of the elemental power transistors.

The assertion that CdSe transistors can indeed function satisfactorily in this application runs contrary to a widely held belief. It rests, however, on the proviso that the matrix drive electronics be carefully designed and operated to obviate the so-called "drift" phenomenon by a scheme successfully reduced to practice during the subject program. The conclusions from the four years of this activity are that thin film transistor addressed displays will be manufactured in a commercially competitive mode for special applications some time during the next several years. The display medium will be thin film electroluminescent phosphor and size and resolution will be limited to about that reported here. However, the use of stencil masks in manufacture will be partly or wholly replaced by modern lithographic and dry etching procedures. It appears likely that the first such production displays will not use thin film transistor scanning and drive circuitry.

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## SUMMARY

The Manufacturing Methods and Technology Engineering program, Contract DAAB-07-76-C-0027, was undertaken to develop and demonstrate a first manufacturing technology for small, 256-character flat panel displays, of a type required for the Army's DMD (Digital Message Device), based on an active-matrix addressed electroluminescent display previously developed by Westinghouse Corporation along with Army support under Contract DAAB07-72-C-0061.

Further aims of this program were to evaluate operating and lifetime characteristics of the manufactured displays, their ability to withstand specified environmental conditions of temperature, humidity, altitude, shock and vibration, and their readability under specified lighting conditions. The manufacturing approach entailed manufacturing thin-film-transistor (TFT) active circuitry on a glass substrate in a single, computer-controlled pilot circuit fabrication facility, followed by deposition of the electroluminescent phosphor as the light emitter, and finally packaging or encapsulation. Because of size limitations of the pilot manufacturing facility, the DMD display was designed as two identical halves, which were then to be made individually in the automated machine and later assembled into a single DMD unit.

The TFT-addressed electroluminescent (or TFT-EL) displays of the preceding program were made in the laboratory with manually-operated vacuum systems using a variable-aperture mask system to define the various thin film patterns deposited by evaporation through the mask onto the glass substrate. In the early phases of the present program, while "dedicated" aperture masks were being prepared for the pilot manufacturing facility, several good quality prototype DMD TFT-EL displays (8 rows of 32 characters) were made in the laboratory system and evaluated for electro-optical performance and also for possible inclusion in a DMD unit modified for the purpose by the manufacturer, Magnavox Corporation.

Necessary modifications included different mounting provisions and new designs for the drive, logic, and power supply circuitry, since the TFT-EL display has different electrical requirements than the currently-employed gas discharge display.

After the complete new aperture mask set was installed in the pilot manufacturing unit, approximately 18 months were spent in making several hundred circuits for 1/2-DMD panels and in attempting to solve numerous problems associated with aperture masks, line and spot defects in the completed 1/2-panels, and machine performance. A considerable effort was spent developing automatic probe testing apparatus for exhaustive testing of the display circuits, but probe scratches caused an inordinate amount of circuit damage.

Concurrently with the development and improvement of the manufacturing process, facilities were assembled and developed for the life and environmental tests including temperature, humidity and altitude chambers, ON-OFF panel exercisers, phosphor evaluation ovens and excitation supplies, and a viewability exerciser. A new design of TFT-EL panel drive electronics was breadboarded and evaluated, and a limited effort on TFT scanner circuitry was conducted (later restricted to a sister program on High Contrast Electroluminescent Displays, Contract DAAB07-77-C-2697).

From the 1/2-DMD panels made in this period, some fairly good DMD displays were assembled, two of which were delivered as engineering samples with documented test data on viewability, contrast ratio, and power dissipation.

Preliminary electro-optical, readability, life and environmental tests were performed on some of the other sample panels, although several were ruined by high voltage transients in the newly-constructed viewability exerciser. The cause of this destructive voltage transient was found and corrected. During this manufacturing experience and from these tests, fairly serious problems emerged with respect to phosphor lifetime at elevated temperatures, deleterious effects of high humidity due to inadequate packaging and persistent spot defects and bus bar shorts and opens. Some of the latter could be treated by post-fabrication

"surgery", but the need for basic improvement in the manufacturing process was evident. The phosphor and packaging problems were attacked by task force teams and notable advances were made in both problem areas.

In October, 1978 a program reorganization was inaugurated to implement a program wind-down made necessary by Westinghouse management's decision to discontinue all R&D efforts in active matrix-addressed flat panel displays. At that time, a new assessment was made of the various problems remaining in the pilot circuit manufacturing process. As a result, a decision was made to use a basic cell redesign and greatly simplified aperture mask set facilitated thereby in order to cut the per-substrate process from a 4-hour, 13-mask, 43-step process to a 1 1/2-hour, 9-mask, 26-step process.

In spite of the very short time remaining in the program, these changes were effected, new design 1/2 DMD circuits were manufactured and tested, and approximately 10 DMD displays were assembled, 8 of which were delivered at the program conclusion. The improved process included a bus bar mask and process redundancy strategy that greatly reduced bus bar opens previously the most prominent and most difficult to repair fault - and resulted in several circuits with zero bus bar opens. The new circuit design provided multiple and distributed test structures with test probe landing pads that permitted the previously developed automatic probe test unit to be used. In addition, an automatic bus short tester was designed and used, as well as inspection and measurement jigs to quickly determine coordinates of faulty elements for ease in excision of permanently ON elements.

The net result of these process improvements was a substantial gain in basic quality of circuits made in the pilot manufacturing facility, but the little time remaining in the program - less than one month - and the small crew operating the facility (2) did not permit an effective shakedown phase. Nevertheless, the participants in this final phase shared a conviction that the rate of panel improvements, given a few more months of operation, would have resulted in a production capability which, though rather slow, would have yielded high-quality, low-defect circuits.



When this program was first formulated, it was based on two fundamental concepts relating to the device and its manufacture. The first was the concept of a matrix of active, light-emitting pixels controlled by a network of switching elements distributed over the viewing surface. The second was synthesis of network circuitry by stencil masking of sequential depositions. If the result of our subsequent technical activity could be summarized in a single statement, it would emphasize reaffirmation of the active matrix concept but rejection of the all-stencil mask approach to manufacturing. Several years ago, one could plausibly argue that the automated all-vacuum sequential-deposition approach to manufacturing was so much more favorable than the hybrid lithographic-stencil path, for example, because of the labor-intensive features and all the equipment and other paraphernalia one saw on a typical silicon line. However, not only has the size of silicon used in manufacturing increased to 5" diameter, but the trend towards automated wafer-handling equipment to provide metal patterning from deposition to lift-off is accelerating. Future efforts in that area of manufacturing matrix-addressed displays should take advantage of silicon VLSI technology, not only in manufacturing but also in design concepts such as fault-tolerance, and extending even to through-the-substrate contacting, taking advantage of highly directional techniques of reactive ion etching.

Within the scope of this program and the all-stencil mask approach, we have determined that the greatest weakness was perhaps failure to recognize and properly to provide for the transistor interconnect problem. The ability of the CdSe thin film transistor to do the job required of it was convincingly demonstrated. Certainly, these devices drift in the conventional sense and in no way could one fabricate with them a 16-bit single chip microprocessor. That, however, is not the point. We have shown that properly matching the matrix drive circuitry design to transistor performance, certainly no insurmountable problem in these days, renders the so-called drift problem inconsequential. The first commercially and militarily viable solid state displays remain most likely to be matrix-addressed, probably by thin film transistors, featuring the thin film electroluminescent phosphor, the silicon drivers, and fabricated by a hybrid lithographic-stencil process.

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## 1. INTRODUCTION

### 1.1 Purpose of the Program

The work conducted under this program served two purposes: the first was the response of Electronics Research and Development Command (ERADCOM), U.S. Army, to the Science and Technology Objectives Guide issued by the Office of the Chief of Staff of the Department of the Army. The second was Westinghouse's own intention to develop commercially the Thin-Film Transistor Display technology which had been pioneered in-house during the nineteen sixties. Accordingly, the program was jointly funded and directed principally at establishing manufacturing methods for the display component rather than intensive device development itself. Since this final report has been prepared by Westinghouse to meet requirements of its contract with the Army, the statement of program purpose which follows relates primarily to military rather than to commercial aspects.

The general need for new solid-state display components to meet future Army requirements was established by several directives. The first was to develop an effective and reliable automated system to allow for the integration and capability enhancement of a new generation of computer systems; in particular, the development of a family of intelligent terminals, display, and associated peripheral equipment for the enhancement of the input, storage, display, retrieval, processing, and output of digital (alphanumeric and graphic) information. A second directive was to develop a near real-time capability for transmission of Missile Control and Guidance outputs in imagery and graphical formats to maximize Electronic Counter Measures capability. This involves hardware and software to convert imagery obtained from reconnaissance into

digital format, transmission of new data via telemetry to a receiver, and reproduction of the imagery for immediate interpretation and use. Equipment requirements for tactical Command, Control and Communications reliability, operability and flexibility were stated to include sufficient terminals to provide input/output capability at every level as required by the Commander.

In particular, the Science and Technology Objectives Guide directs the development of graphical devices throughout the fire support system that will interface with command and control devices in both fire support and maneuver communications. Some examples of applications are:

- hand-held ground surveillance radar
- tactical air data overprints for aviation maps
- readout capability for satellite-derived imagery in the tactical area
- technical and instructional documentation structuring, storage, retrieval and editing.

The last application mentioned above includes the evaluative use of ARTADS equipment such as the Digital Message Device (DMD). The specifications for the display component of this hand-held battlefield-integrated command and control terminal was responsible for the final form of the present program. The existing DMD configuration is shown in Figures 1.1 and 1.2. This is a reproduction of a brochure prepared by the Sensor and Signal Processing Division of the Magnavox Corporation which, under contract, produced such units earlier developed by the Army ARTADS organization.

Operating versions of the DMD presently feature the Burroughs "Self Scan" DC gas discharge display panel. Operationally, this component renders it very easy to initiate a light-emitting discharge at a second point in the panel in the immediate vicinity of a first discharging point. The Self-Scan panel utilizes this effect by incorporating a multiphase clock producing a sequence of voltages to propagate a

# Magnavox DMD



## DISPLAY:

Rugged plasma display, 256 characters (formed by 5 x 7 dot arrays), power consumption proportional to number of characters displayed and to brightness. Display illumination level is adjustable.

## KEYBOARD:

Sealed, flat surface, pressure actuated, back-lighted for night operation and durable.

## PROGRAMMABLE CONTROLLER:

16-bit microprogrammed, 100ms cycle time, 600ms add time, 9 registers (3 index), 1 watt peak power (1008), fully military (all general-purpose computer).

## SOFTWARE:

Support package available. Allows user to develop programs on an IBM 360.

## DATA TRANSMISSION:

FSK (1200 or 2400 bps) at 600 or 1200 bits per second.

## BITE:

Self-contained ability to fault-isolate to nearest replaceable module.

## ERROR DETECT and CORRECT:

Data is Hamming-coded and is time-dispersed by 16 character blocks. Optional double-block (repeat) transmission mode allows accurate communication in spite of adverse noise environment.

**SIZE:** 11 x 7.7 x 5.7 in. (27.9 x 19.6 x 9.4 cm)

**WEIGHT:** 9.7 lb (4.56 kg) (with battery)

## BATTERY:

Sealed, Nickel Cadmium or Lithium, BB-506 form factor, 5.91 in. (10 cm) length, 12/24 Vdc nominal.

## ALTERNATE POWER:

Connector for external power permits operation from 20 to 50 Vdc.

**OPERATING TEMPERATURE:** -10°C to +71°C

**WATERPROOF:** Submersible to 5 feet (1.51 m)

## APPLICABLE MILITARY SPECIFICATIONS:

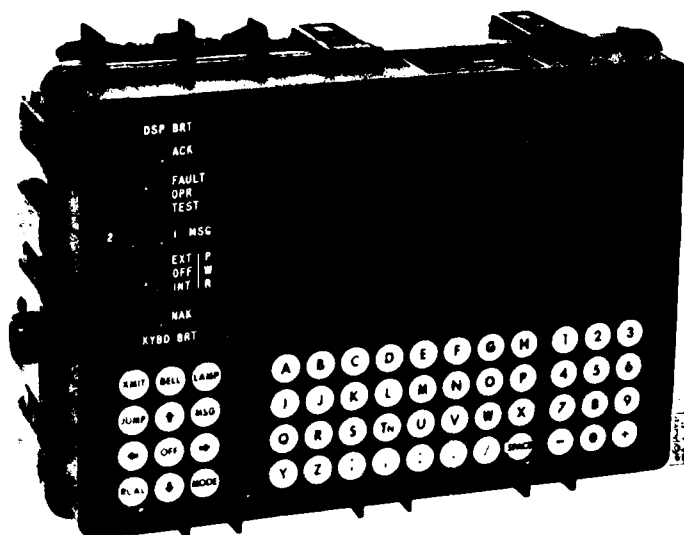
401-Std-454, 701-Std-461  
MIL-P-11268, RPD-Std-1

## APPLICATIONS:

FACEDM, DMD, 108" DMD, and Ballistics.



Figure 1.1 Front page of a brochure prepared by Magnavox Corporation describing the DMD.



# DMD

## DATA AUTOMATION:

The Digital Message Device (DMD) provides simplified, portable, two-way, source data automation in standard message formats or in free text.

## AUTOMATIC ENTRY SEQUENCE:

The operator is led through the message-entry sequence by the display. Entries are made via the keyboard either as direct data or as coded selections from

a displayed menu. A menu item is selected by pressing the indicated keyboard letter.

## PROGRAMMABLE:

The "personality" of the DMD (man-machine interface characteristics) as well as the message formats and entry menus are programmable via a removable memory module.

## COMMO COMPATIBLE:

The DMD interfaces with standard radio equipment (FM and AM including SSR) as well as two-wire telephone equipment.



Magnavox Corporation  
Signal & Data Processing Division  
P.O. Box 1000  
Spartanburg, South Carolina 29302

**Magnavox**



Figure 1.2

Second page of the DMD brochure prepared by Magnavox Corporation.

scan-glow across the display.<sup>(1)</sup> The full operation has been explained in the literature.<sup>(2)</sup>

While the Burroughs panel met some critical requirements of the DMD which were not attainable by CRT technology, ERADCOM has determined that the relative fragility, high weight, and power demand of this gas discharge panel makes pursuing alternative display concepts highly desirable. In particular, the Westinghouse Thin-Film Transistor Addressed Electroluminescent Display technology seemed to have the potential of combining both reduced weight and power consumption with extraordinary rigidity. Unlike the situation with the Burroughs panel, however, the Westinghouse unit had never been made in any quantity. In fact, one could argue that it had previously only demonstrated an intriguing level of performance after each unit had been coaxed through the laboratory in a very labor-intensive process. Table 1.1 purports to show these and other aspects of the differences between the Burroughs and potential TFT-electroluminescent panels.

Against this background, the purpose of this program may be briefly stated as the development of Manufacturing Methods and Technology Engineering for a Thin-Film Transistor Addressed Electroluminescent Display which is, accordingly, the formal title of the program.

## 1.2 The Flat Panel Concept

By default, any display component which is not a cathode ray tube seems to have been assigned the description of "flat panel," and, of course, the TFT-addressed display, be the display medium electroluminescent phosphor, liquid crystal, or whatever, is included in this broad description. As their name suggests, flat panels are geometrically plane and rectangular. They are also "thin" in the sense that their dimension in the direction of viewing is substantially less than that normally required for the neck and gun assemblies of conventional cathode ray tubes. However, the semantics have been complicated by the relatively recent development of so-called "Flat CRTs" by both U.S. and foreign

TABLE 1.1 COMPARISON OF PERFORMANCES OF  
DISPLAY COMPONENTS FOR THE  
DIGITAL MESSAGE DEVICE

Property	Present D. C. Plasma Panel (Burroughs)	Potential for TFT-addressed Electroluminescent Panel
Weight	1+ lb.	5 oz
All-dots-on power dissipation	4w	0.8w
Display Mode	Alphanumeric Only	Alphanumeric and graphics
Dimmability	Limited by scan glow at low levels	Continuous to zero
Sunlight Visibility	Marginal	Good with high contrast thin film EL
Viewing Angle	$\pm 25^\circ$	$\pm 80^\circ$
Operating Temperature	0 to 60°C	-55° to 125°C

organizations. N.H.K. (Japan Broadcasting Corporation) Technical Research Laboratories in Tokyo has been, for some time, developing a color TV display system incorporating planar positive-column cells. Texas Instruments of Dallas has also developed a flat CRT capable of producing full color by using multiple electron beams generated from an area cathode and then formed and digitally addressed by a switching stack.<sup>(3)</sup> However, for the purposes of comparing flat panel and CRT displays for tactical systems, the flat CRTs probably better fit the Cathode Ray Tube category shown in Table 1.2. This analysis emphasizes the importance of developing alternative display devices for applications such as the DMD and the manufacturing methods necessary for their production in meaningful quantities.

All flat panel display technologies, unlike the CRT alternative, feature the addressing of a so-called matrix of pixels. A pixel can be a two-terminal device which responds optically to electrical signals. The matrix is geometrically regular in the X and Y directions, perpendicular to normal viewing. In the (horizontal) X-direction, a row of pixels all have a common first terminal. Each pixel is connected by its second terminal in common with those of other pixels in the same column in the (vertical) Y-direction. Through such a connection each pixel receives video information as shown in Figure 1.3.

In principle, matrix addressed display panels can be classified and characterized according to the display medium which transforms electrical signals impressed on the lines ("bus-bars") into imagery. Comparative characteristics of the leading contenders for flat panel display purposes are shown in Table 1.3. Here we observe the apparent desirability of the thin-film electroluminescent display medium. The characteristics listed in Table 1.3, therefore, determined to a large extent the nature of the component with which this program was concerned. However, selection of display medium was not the only consideration.

All the display media listed in Table 1.3 can, in principle, be driven either by a so-called "passive" or an "active" matrix. The passive



TABLE 1.2 COMPARISON OF FLAT PANEL AND CRT  
DISPLAYS FOR TACTICAL SYSTEMS

<u>FLAT PANEL</u>	<u>CATHODE RAY TUBE</u>
Needs Development	Mature Technology
<u>Wide Tactical Applicability</u> Low Volume, Lightweight Displays possible with Negligible Depth and Miniaturized Drive Circuits,	Not practical for portable and handheld applications due to tube depth and the weight of bulb and deflection hardware.
<u>Low Power Consumption for Page-size</u> Display including Drivers, on the Order of 10W	Power consumption including high volt- age, deflection and filament, greater than 100W
<u>Sunlight Legibility</u> possible with TFEL and black layer	Requires high brightness tube and filters resulting in low reliability
<u>Parallel Data Input</u> Interfaces easily with digital systems	Serial input at 60 Hz refresh rate requires complex interface.

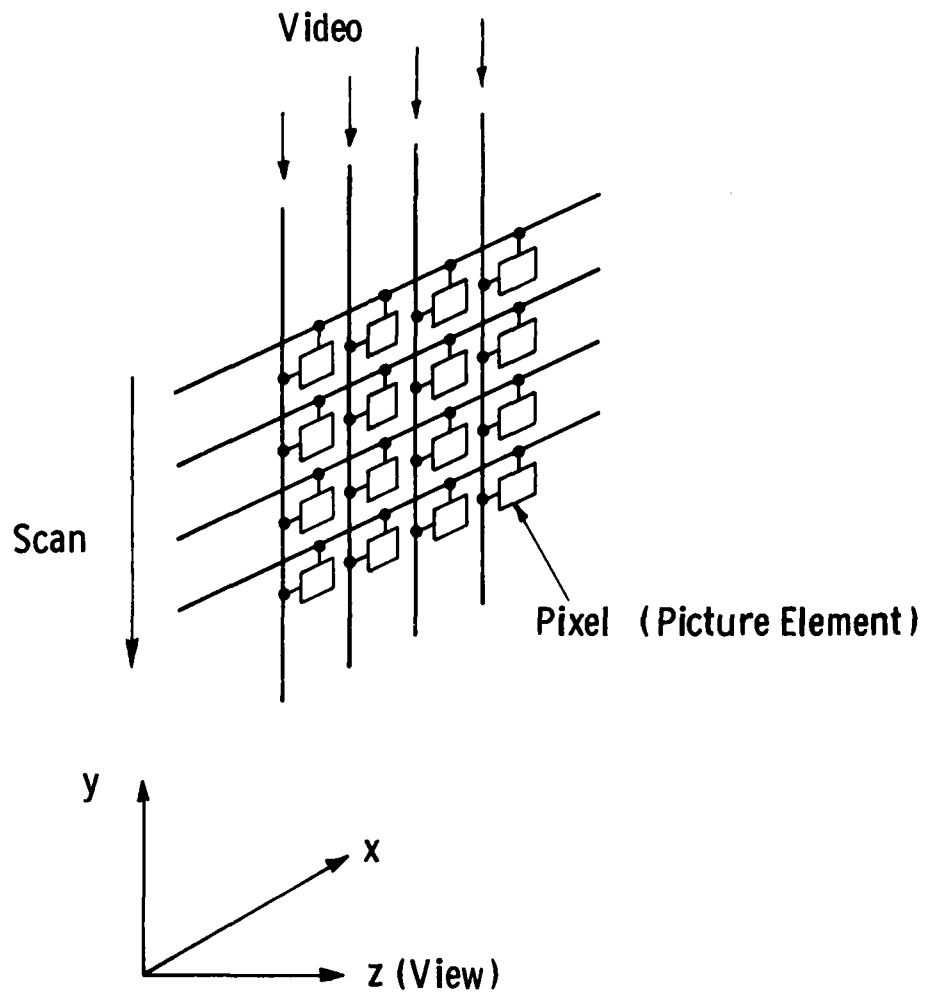


Figure 1.3 The concept of matrix addressing featured in flat panel displays.

TABLE 1.3 COMPARISON OF CONTENDING  
DISPLAY MEDIA FOR  
SOLID STATE FLAT PANELS

	Thin Film Electroluminescence	Liquid Crystal	Plasma Panel	Electro- chromic	Electro- phoretic	LED
State of Development	Limited Availability	Limited Avail.	Avail- able?	In Research	In Research	Somewhat Available
Sunlight Legibility	good	good	marginal	good	good	poor
Power Consumption	low	very low	high	very low	very low	high
Operating Temperature Range	Full Military	very limited	low temp. limit	unknown	unknown	high temp. cycling limit
Ruggedness	Excellent	limited	poor	unknown	unknown	excellent

matrix is essentially that depicted in Figure 1.3. The pixels therein are strictly two-terminal devices and energy consumed by optical emission is delivered entirely by the bus-bar system. The operation features line-at-a-time addressing wherein video for a row of pixels is simultaneously dumped onto all vertical lines as the appropriate horizontal line is addressed. Sequential scanning of all horizontal lines coupled with appropriate and timely impression of video signal levels on the vertical lines synthesizes the required image. This is, of course, provided that all lines are properly electrically isolated and that the frame rate is fast enough in relationship to some memory capability of the pixels.

In the active matrix version of any display medium, the pixel structure is more involved, consisting essentially of the passive pixel in series with some kind of electrically alterable impedance at each picture point. The active pixel is thus generally a four-terminal structure. A comparison between the two types is shown in Figure 1.4. This diagram attempts to show how, in the active version, the WRITE operation, which sets the impedance level, responds to the video signal, on the column bus-bar, only when the switch is closed by the row bus-bar. Although the active pixel is more complex, we shall now see why it has something special to offer in terms of display performance and, consequently, why Westinghouse thin-film transistor technology was featured in this program. These arguments do not hinge exclusively on the selection of thin-film electroluminescent phosphor as the display medium but are, nonetheless, slanted with this in mind.

The most commonly quoted advantages of the active matrix concept as far as display performance is concerned relate to:

- luminance
- power consumption
- resolution
- drive circuit complexity
- data refresh rate.

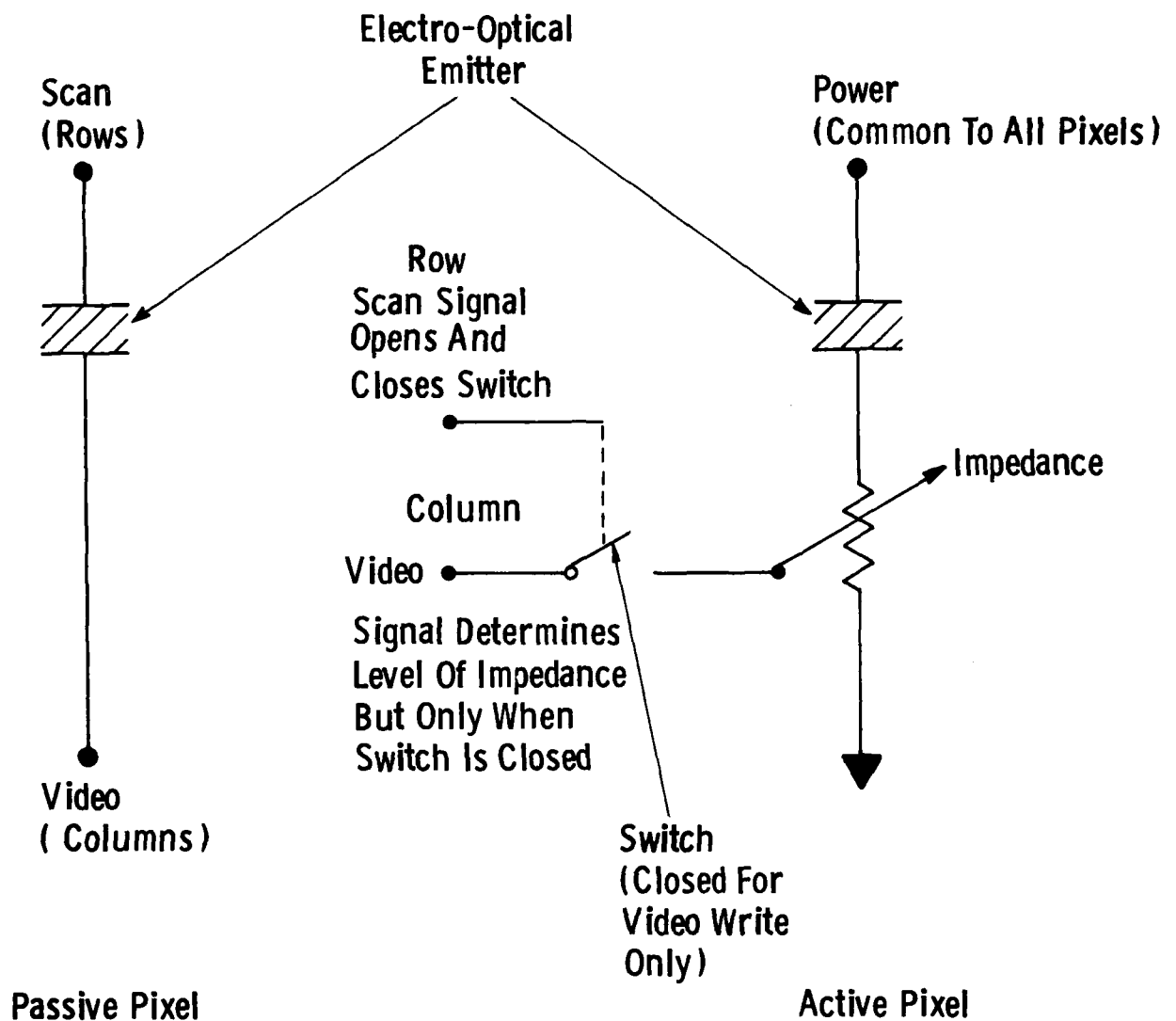


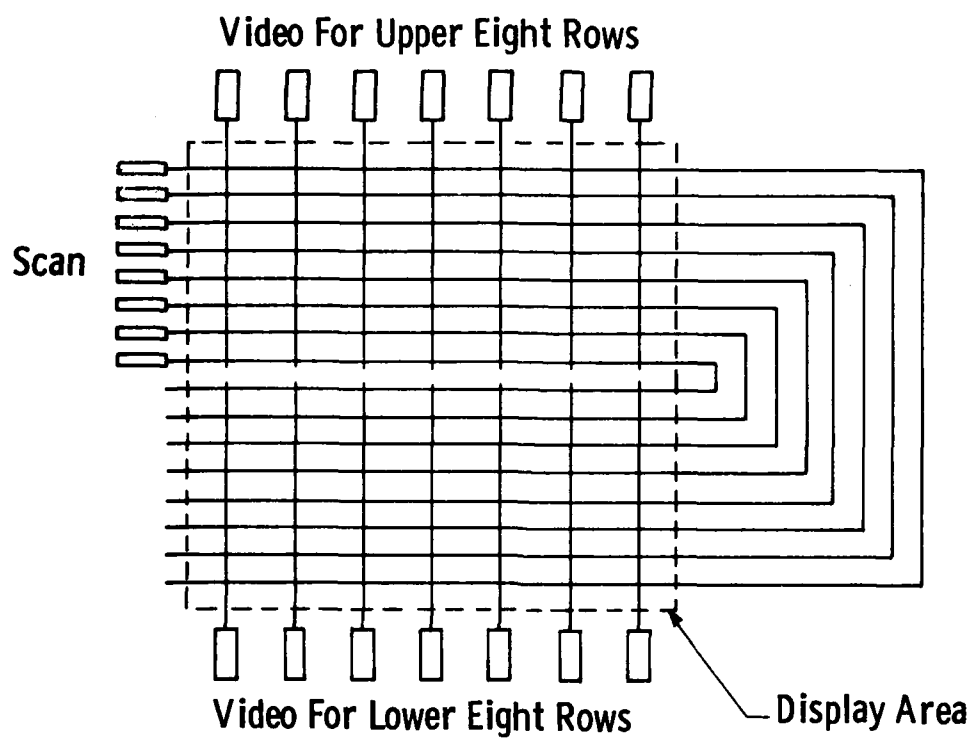
Figure 1.4 Basic differences between pixels of active and passive displays.

All of these factors are extremely important in the military field applications discussed previously in Section 1.1. We shall now elaborate on each in turn vis-à-vis the potential advantages of the active matrix. During the discussion, however, we shall consider only the basic passive matrix wherein all lines, both vertical and horizontal, are continuous. There exist concepts of passive matrices wherein the aggregate display is assembled from basic passive modules exemplified in Figure 1.5. While this does alleviate some of the demands on the display such as luminous efficiency brightness, refresh rate, etc., there is a rather low limit to the extent such trickery can be practiced in the passive display.

Luminance. In a basic passive display having  $N$  rows, each line is driven with a  $1/N$  duty cycle. Effective display luminance is thus proportional to  $1/N$  times the average pixel luminance while it is being driven, unless the display medium itself has some kind of inherent memory. While electrophoretic passive pixels for example do indeed possess this facility, electroluminescent phosphors generally do not. They certainly do not to the extent that can be provided by memory which can be built into the active matrix pixel, effectively to "lock" the variable impedance (shown in Figure 1.4) at a fixed level between refreshes. An ability to write a particular impedance level in and sustain it for a frame time means that the light emitting elements can be driven with a 100% duty cycle. This in turn provides display luminance not  $1/N$  but unity times the pixel luminance.

It follows that, all other things being equal, lower drive voltages to power light emission can be employed generally resulting in higher reliability. Alternatively, at given allowed drive voltage levels, active panels can be viewed effectively in higher brightness ambients.

Power Consumption. Within the scope of existing technology, power consumed in the drive electronics for passive panels typically exceeds several times the limiting system dissipation as determined by the display medium. This is due to the requirement to switch power from line to line. On the other hand, only signal level power is switched in the



**Figure 1.5** Variation of the passive panel which alleviates some of the demands on the display medium.

active matrix making it possible to approach conditions wherein system power is that of the display medium itself. This consideration is particularly important for battery-powered portable systems such as the DMD.

Resolution. For given display dimensions, maximum row resolution is limited not only by average luminance, which is proportional to  $1/N$ , but also to tolerance to crosstalk, which is proportional to  $N$ . Since in active matrices neither row resolution nor crosstalk are dependent on the number of lines, high resolution formats with row counts exceeding 500 lines, for example, become feasible.

Drive Circuit Complexity. To operate an  $M \times N$  passive pixel matrix, drive level voltages of typically 100 - 200V must be applied to  $M+N$  inputs making extraordinary demands on conventional integrated driver technology. In the case of the active matrix, drive voltage can be applied to a single pair of terminals and only signal level voltages need be applied to the  $M+N$  inputs. Since overall system cost and complexity is heavily weighed by the driver component, these system characteristics can be favorably and substantially affected by featuring the active version of the matrix.

Data Refresh Rate. The minimum refresh rate to avoid observer perception of flicker in a passive panel is about 30 Hz, regardless of the animation rate of the image. Thus, an  $M \times N$  passive matrix display requires a minimum of  $30 \times M \times N$  data bits per sec. A higher rate may be required to achieve sufficient brightness. Even in the case of an animation rate of 6 Hz for dynamic images, the 100% effective duty cycle of active matrices (with pixel memory) requires a refresh rate of only  $6 \times M \times N$  data bits per sec. For static images, the refresh rate for active matrices is limited only by the pixel memory itself. Pixel memories of one second or more are now achievable. Consequently, the active matrix requires less than  $1/5$  for dynamic images (and  $1/30$  for static images), the data bit refresh rate of passive matrices, all other things being equal.



In review, we have so far attempted to support the thesis that a display consisting of an active matrix driving thin-film electroluminescent phosphor offers the greatest potential for specific applications such as in the DMD. What we will now do is explain the role of thin-film transistors and powder phosphor which constituted the display configuration for the present program.

Once one has decided he needs an active matrix with dimensions exceeding several inches, the selection of a technology for cost-effective synthesis of the array of switching elements becomes remarkably simple because there is only one, namely that of thin film transistors. At the time the present program was conceived and initiated, Westinghouse Research Laboratories had developed this technology to a level which convincingly demonstrated its feasibility, at least on a laboratory scale.<sup>(4-6)</sup> Some examples of the technical status of phosphor dot array displays in this field prior to the beginning of the current program are shown in Figures 1.6 and 1.7. Both figures demonstrate a 20 lpi capability developed under Contract DAAB07-72-0061 sponsored by the former Army ECOM organization and are extracted from Quarterly Reports on work performed under that Contract in the period November 1973 to September 1974. The device configuration is a powder phosphor medium driven by an active matrix featuring thin-film transistor switching. Table 1.3 has, however, previously identified the potential superiority of thin-film electroluminescent phosphor as a display medium. There are substantial differences between this and the powder type used in Figures 1.6 and 1.7, although each is usually zinc sulphide-based in flat panel display work. Generally speaking, the all-vacuum deposited thin-film version performs much better, with higher brightness, higher temperature and longer life performance. By virtue of its transparency, and in conjunction with a black background, it can provide readability in extremely bright (10,000 fc) ambients. The powder phosphor is, on the other hand, nominally very easy to apply to the active matrix. It may thus be viewed, as indeed it was during the later phases of the current program, simply as a medium with which to develop manufacturing

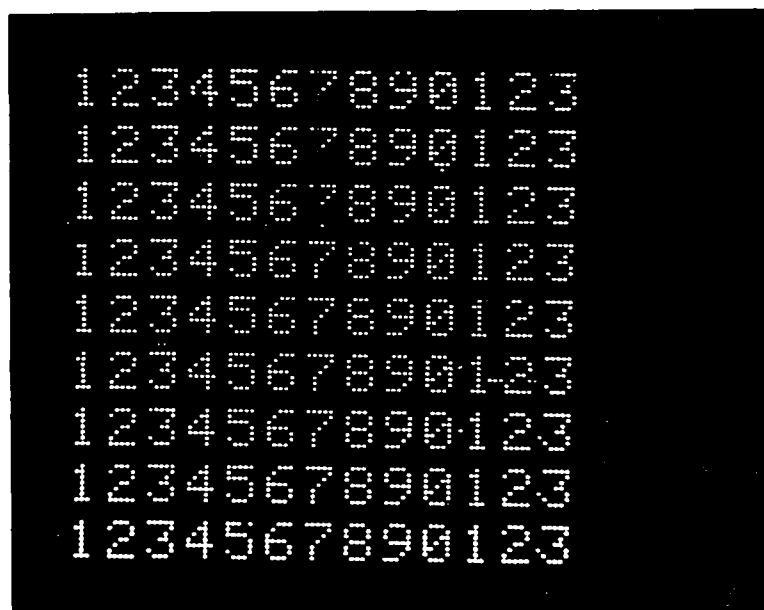


Figure 1.6 Example of Westinghouse Thin-Film Transistor Addressed Display Technology prior to the beginning of the current program.



Figure 4.7 A second example of nest-in-house technology prior to the beginning of the current program.

methods for thin-film transistor addressed active switching matrices. In a parallel effort, ERADCOM sponsored research at Westinghouse to develop thin-film electroluminescent phosphors for thin-film transistor addressed displays under a separate Contract, DAAB07-77-6-2697. The strategy presumably was to separately, yet simultaneously, focus on the weaknesses in thin-film transistor addressing manufacturability, and on the weaknesses in thin-film electroluminescent phosphor, addressing its basic development. The objective of this was to converge on the ultimate component--a thin-film transistor-addressed-active-switching-matrix driving a thin-film electroluminescent pixel array.

The concept of a flat panel engineered to serve the purpose described in Section 1.1 is not complete without one final consideration. Historically, the peripheral circuitry required to impress video data, ordinarily supplied in a serial stream, onto the vertical bus-bars had been accomplished by means of silicon integrated circuitry, usually referred to as the horizontal scanner. The sequential one-at-a-time activation of the horizontal bus-bars had likewise been accomplished by a peripheral silicon circuit called a vertical scanner. A feature of the thin-film transistor addressed display is its capability in principle of being fabricated simultaneously with horizontal and vertical scanners on a single substrate; these scanners were made like the display addressing circuitry, entirely from thin-film transistors. Against this background, the specific flat panel concept formulated to meet the needs discussed in Section 1.1 becomes more focussed. The present program has concerned itself with a flat panel display featuring an active matrix with thin-film transistor switching elements, integrated or otherwise connected thin-film transistor-based scanners, and a powder phosphor display medium. The overall task has been to develop Manufacturing Methods and Technology Engineering for such a component as a prelude to subsequent and related activity directed at an integrated scanner-switching matrix circuit driving a thin-film electroluminescent phosphor medium.

### 1.3 The Manufacturing Concept

The last paragraph of the previous section has defined the concept of the component with which this program is concerned. The task of this section is to review briefly the development of fabrication methods and to focus more specifically on the approach adopted during the current program.

What one is basically trying to make here is a thin-film transistor circuit. (The subsequent powder phosphor application is really a separable and less demanding facet of the technology and its discussion is postponed to Section 7 herein ). The basic element of a thin-film active circuit is the transistor itself. A cross-sectional view of such a device is shown in Figure 1.8. It is formed by the patterned sequential deposition of metal, semiconductor and insulator materials. Extensive, more complete descriptions have been described in Section 2.4.1.

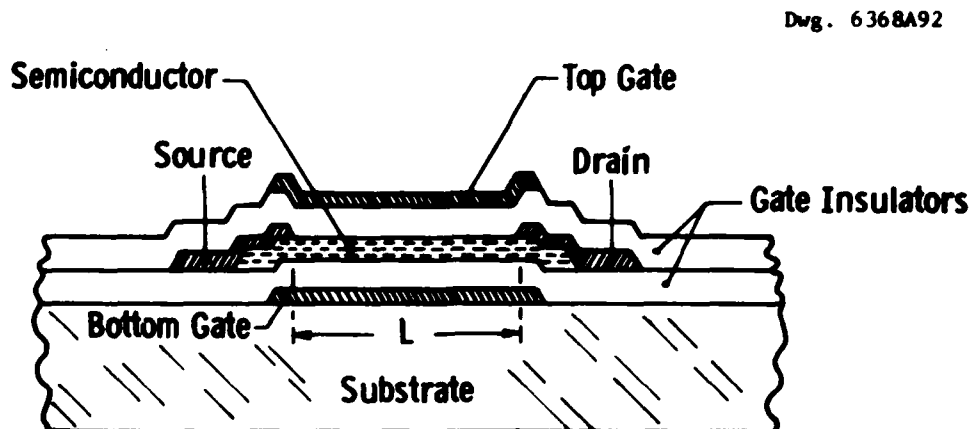


Figure 1.8 Cross section, perpendicular to current flow, of a typical thin-film transistor.

lines and capacitors are formed in much the same way as the transistor. Prerequisites to the task of fabricating the circuit are the design of the electronics and the layout, just as they are in the case of conventional silicon integrated circuit technology. Usually, in the case of thin-film circuits, however, at least some of the physical patterning is achieved by alien procedures. The various options for patterning thin-film circuits are shown in Figure 1.9. Referring to Figure 1.9, an example of variable aperture masking is the so-called X-Y method, which is conveniently suited, but nonetheless limited, to matrix patterns which are geometrically regular in both the X and Y directions. The desired pattern is generated by the controlled movements of a set of two metal masks placed in contact with each other and the substrate. By appropriate absolute and relative movements of each separate mask to a location required for the evaporation being made, virtually any required pattern can be synthesized. The mechanics of the XY method are illustrated in Figure 1.10 and Figure 1.11. This technique has been historically favored at Westinghouse because it obviated some of the technical obstacles associated with other delineation schemes. These obstacles have been overcome by advances in computer-aided design and mask generation equipment demanded by the silicon industry in more recent years.

Referring again to Figure 1.9, dedicated stencil masking involves pattern delineation with a set of multiple aperture masks. Each mask is "dedicated" to a particular evaporant although, unlike the XY method, only one mask is used at a time.

Pattern delineation can also be obtained by a variety of means following non-patterned deposition or depositions. In Figure 1.9 these have been segregated into lithographic and "other," which includes laser cutting, a variation of the laser trimming technique. Such techniques in their pure form eliminate the need for stencil masks altogether. Some of the advantages and disadvantages of the four approaches can be implied from the comparative properties of each, as depicted in Table 1.4.

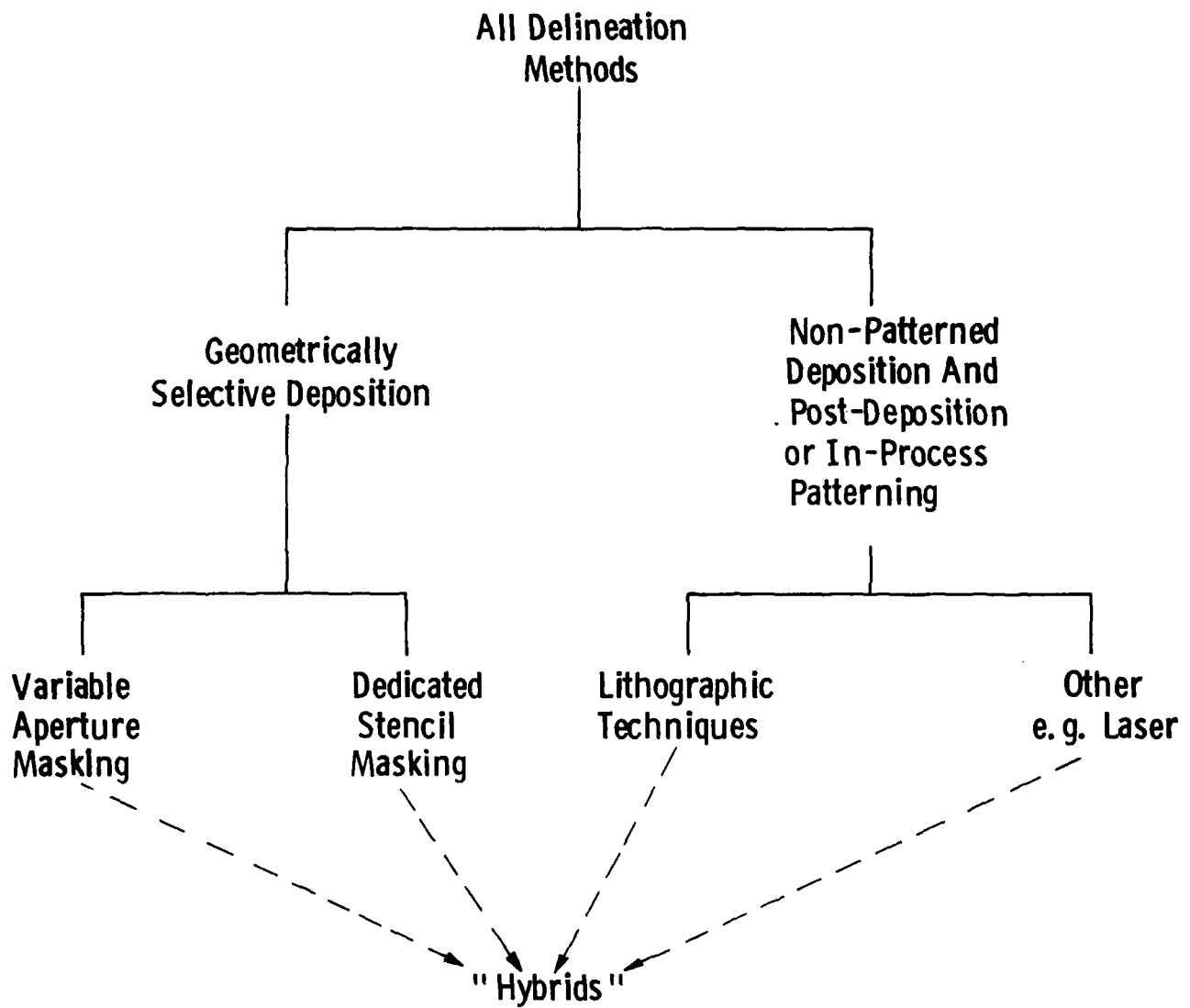
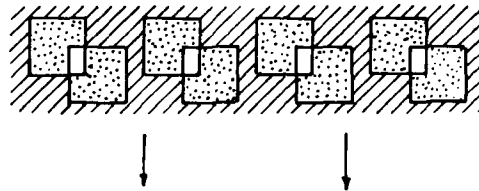


Fig. 1. 9 – Broad classification of thin-film pattern delineation methods.

Draw. 62-9A25

Overlapping Rectangular Openings from Two  
Contacting Masks having the Same Pattern of  
Apertures



Typical Deposited Pattern after Evaporation  
through Mask Set Above

Any Rectangular Pattern, Including Continuous  
Lines, can be Generated in this Fashion

Figure 1.10 The principle of the XY approach to thin-film pattern delineation.

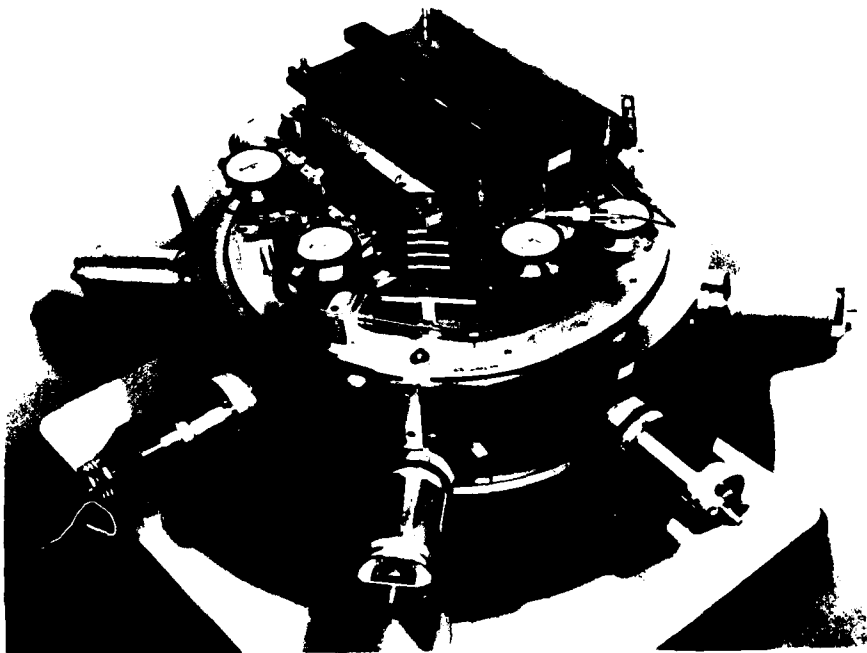


Figure 1.11 The XY mask movement fixture.



TABLE 1.4 RELEVANT COMPARATIVE PROPERTIES OF THE  
FOUR BASIC APPROACHES TO THIN FILM  
DEPOSITION PATTERNING SHOWN IN FIGURE 1.9

	APPROACH			
	Geometrically selective deposition		Post-deposition * patterning	
	Variable Masking	Dedicated Masking	Lithographic	Other
Difficulty of Mask Design and Procurement	Nominal	Substantial	Nominal	None
Throughput	Slow	Fast	Slow	?
In-Process Quality Control	None	None	Yes	Yes?
Extendable to Large Area	No	No	Yes	Yes?
Geometric Resolution	100 LPI	100 LPI	Higher	Higher
All Vacuum Process	Yes	Yes	No	No
Proven	Yes	Yes	(Yes)	No

\*Actually, certain "films" in this case need not be formed by vacuum deposition. Plating-up, for example, can serve passive functions such as interconnecting and bus bar synthesis.

Finally, Figure 1.9 implies the existence of so-called hybrid techniques. An example which has gained considerable favor in our group in recent years features conventional stencil-mask-defined and vacuum-deposited thin-film transistors. These are interconnected into the required circuit by prior or subsequently created passive circuit elements, which could, for example, be realized by photolithographic delineation of non-patterned depositions. While there are probably several other workable schemes, this approach seems capable of effectively combining the best of the four different pure art-forms in Figure 1.9. The logistical difficulties associated with the design and procurement of dedicated masks and implementing their use have traditionally been quite formidable. Only in recent years when computer-based graphics have become available has the problem seemed tractable. However, Westinghouse prides itself on having now reduced the methodology as described in Section 4 to a fine art.

In spite of this, there is a customary turn-around time irritation when one wants to alter the pattern, and this has been responsible for the lingering survival of the XY mask approach. The latter naturally cannot readily be employed to generate anything other than regular patterns. This renders mask design for (integrated) scanner circuits, for example, a major challenge. This is not true of dedicated masks, once the design and procurement methodology has been established.

As far as laboratory-scale fabrication schedules are concerned, throughput rates are not particularly important. However, we have observed that operation errors tend to occur more as a function of elapsed time involved in processing. This in itself favors the dedicated approach. In addition, in a quasi-production environment, throughput per se is extremely important. The materials content of displays, within the framework of the concept of Section 1.2, is extremely low, perhaps a few dollars. In principle, their labor content can be rendered commensurably small. The two together are, in fact, insignificant compared to the depreciation of required capital equipment and other period costs.

Therefore, it is mandatory to maintain high throughput in a cost-minimizing production venture of components of this type.

An indisputable advantage of approaches featuring post-deposition patterning is an in-process control facility. One can conveniently maintain quality assurance of appropriate circuit features such as bus-bar continuity as fabrication proceeds. In the all-vacuum environment characteristic of stencil masking of whatever type, in-process testing is not readily achievable although this is partially offset by the "pristine surface" argument.

As far as display format specifications are concerned, the post-deposition patterning approaches would seem to have an edge. This is not quite so clear in the case of resolution but it is certainly true for display area. It is very unlikely that dimensions much in excess of 6-10" can be achieved at competitive resolutions of about 50 lpi with any kind of stencil masking due to the difficulty of fabricating the masks themselves and their subsequent use in a vacuum system.

For the purpose of the present program, Westinghouse argued in favor of the dedicated mask approach. Once one discards consideration of difficulty associated with mask design and procurement, all other factors in Table 1.4 rule in its favor or are inconsequential as far as existing program requirements are concerned. The only exception to this rule is perhaps the lack of "in-process control." We naturally recognized this and sought to overcome it by utilizing ingenuity and devising trickery to minimize the need for such activity. This was done to a large extent by full exploitation of our expertise in mask design and procurement which we felt was more than equal to the task. This does not mean that the variable masking approach was immediately discarded. In fact, it was widely utilized early in the program to develop critical circuit fabrication geometries on an empirical basis. For this, it was well suited. This was, however, the full extent of its role. Throughput rates, all-important in a manufacturing methods environment, were selected for the dedicated mask concept by an order of magnitude.

The Westinghouse stance in favor of the dedicated mask approach to fabricating the active switching matrix secured the approval of the customer and led to the manufacturing scheme whose gross features are shown in Figure 1.12. The task of explaining the details of the scheme is relegated to Section 3.1 in this report.

#### 1.4 Overview of Program History

Westinghouse submitted its formal proposal for the Manufacturing Methods Contract to the U.S. Army Electronics Command (then ECOM) at Fort Monmouth, New Jersey through its Industrial and Government Tube Division in Horseheads, New York, on November 5, 1975. Work began in May 1976 and this first phase of the program continued through December 1977, at a cost to ECOM of about \$300,000. During the same period, Westinghouse infused a substantially greater sum to supplement other funds it had already invested in program-related technology.

At the beginning of the program, one of two aspects of Westinghouse's relevant technical capability is well summarized by the displays illustrated previously in Figures 1.6 and 1.7. These relatively low resolution displays had, however, been fabricated by the XY method and embodied substantial, post-deposition, very highly skilled labor to coax them to relatively defect free operation. The other aspect of our capability was our earlier development, construction and inaugural operation of a large capacity, computer controlled automatic vacuum system specifically designed for quasi-pilot production of large area (4"x4") thin-film transistor integrated circuits. This equipment is illustrated in Figure 1.13 and had been used in an attempt to "mass-produce" all thin-film digital timers during 1975.<sup>(8)</sup> It is more fully described in Section 5.2. While only several operating timer units were eventually fabricated, this was done with the dedicated mask scheme, for which mode of fabricating the automatic vacuum system had been designed exclusively. Thus, at the beginning of contract activity proper, our technical capability might be summarized as follows:

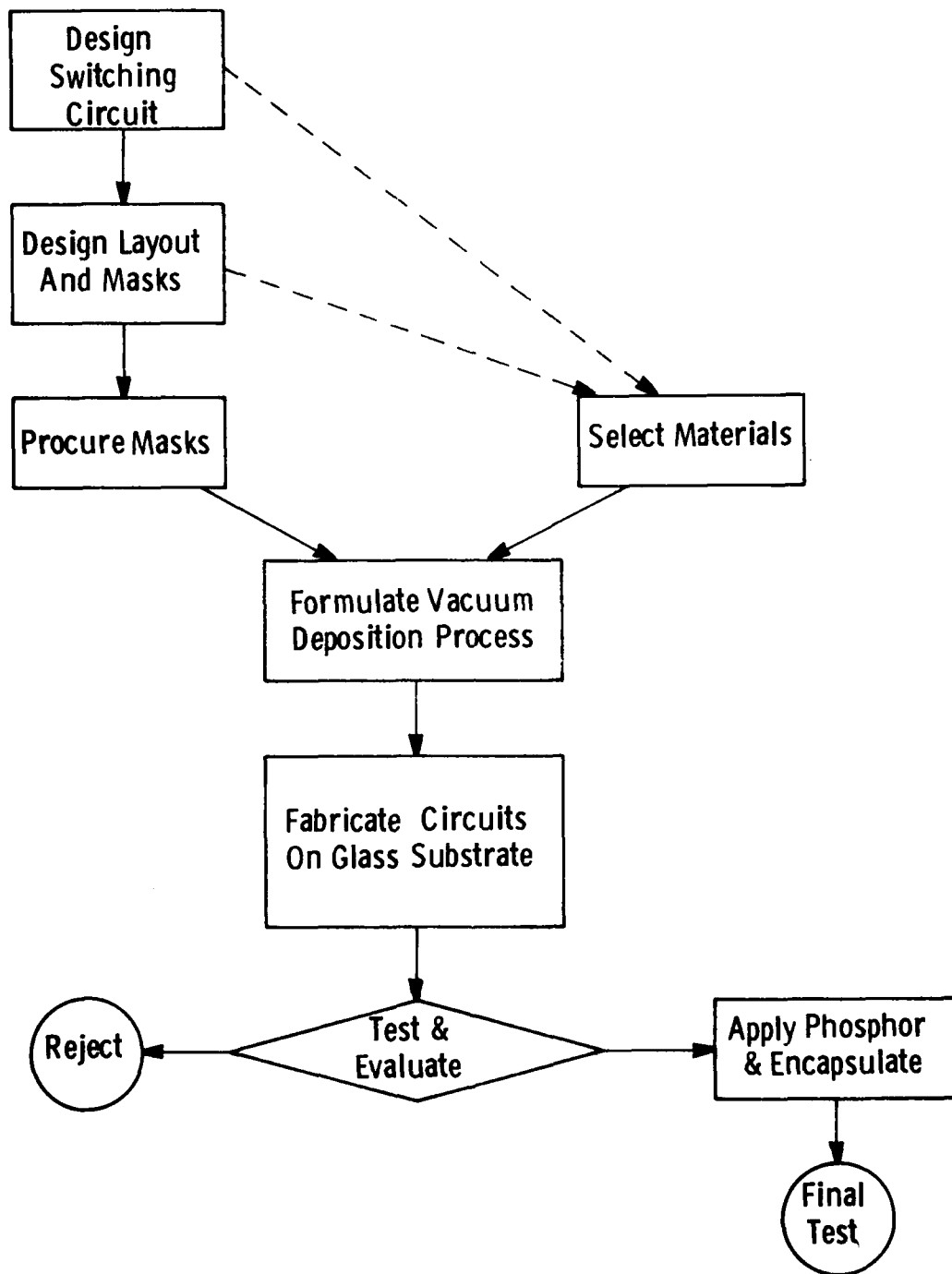


Figure 1.12 Gross features of the manufacturing concept adopted by Westinghouse for fabricating thin-film transistor switching matrices with the dedicated mask approach.

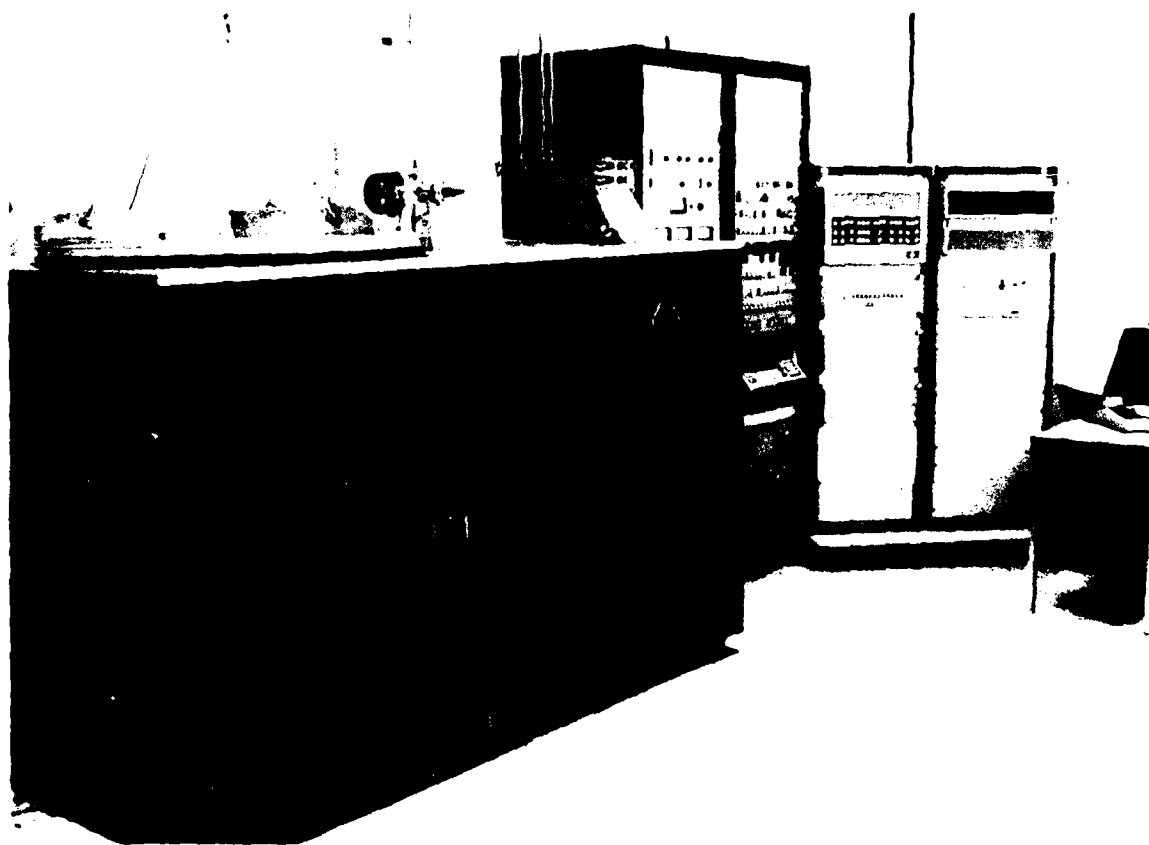


Figure 1.13 Westinghouse's computer controlled, quasi-production oriented, automatic vacuum system available at the beginning of this program.

1. Ability to produce working 6"x6" thin-film transistor addressed (powder) electroluminescent phosphor displays, characterized by
  - 20 lpi line density
  - fabrication by slow and costly XY mask technology.
2. An automatic vacuum system featuring dedicated masks characterized by
  - actual prior fabrication of digital circuits
  - a very low yield
  - high throughput potential.

By necessity, both parties, ECOM and Westinghouse, recognized that technical objectives should reasonably match this capability. In terms of deliverable hardware, the objectives for the May 1976 to December 1977 phase were formulated around working displays to meet the needs of the DMD, shown in Figures 1.1 and 1.2. A mock-up of the display component is shown in Figure 1.14. More precise technical specifications follow later in Section 2.5. The specific objectives were couched in terms of delivering such units in quantities as follows:

- two engineering samples: the purpose here was to verify successful transferral of previously demonstrated XY fabrication skills acquired in the laboratory to the pilot facility featuring its dedicated mask approach and the DMD geometrical format.
- two confirmatory samples: these samples had to meet demanding environmental tests specified in Document SCS-501 (Appendix A) to verify phosphor application and encapsulation technology, and the capability of the thin-film transistors themselves to meet the same rigorous testing.
- 20-piece pilot run: The number of units was to be made with the identical process as were the

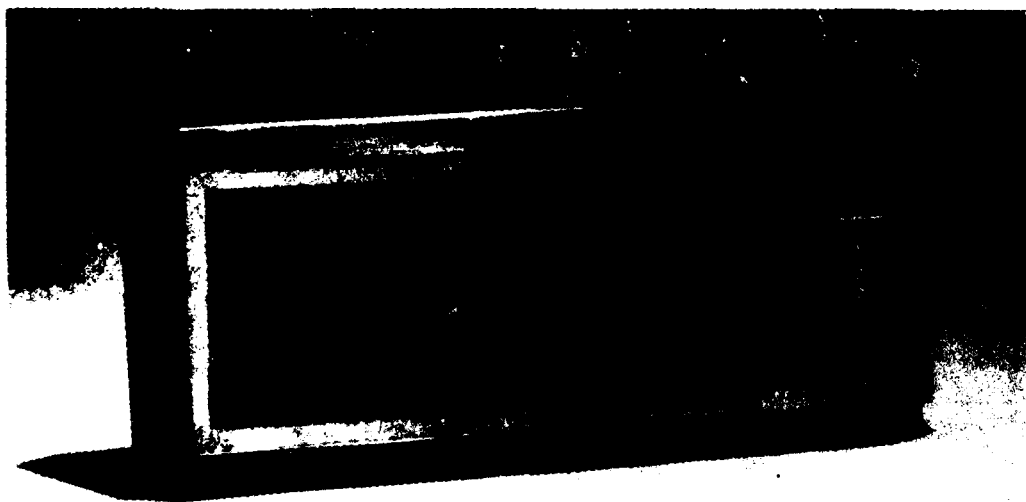


Figure 1.14 Mock-up of display component in terms of which technical objectives for the first phase of the program were formulated.



confirmatory samples within a specified time period. This was to ensure conformance with the customer's stance that feasibility of manufacturability at a level commensurate with future military requirements was the ultimate objective of the project.

One could then readily assess the nature of our mission within the framework of a Manufacturing Methods Development task as:

1. Transfer X-Y display circuit fabrication expertise to the automatic vacuum system ("pilot facility") with its dedicated stencil mask mode.
2. Coax pilot facility operation to a performance level commensurate with its theoretical capacity. In other words, make a whole lot of circuits with a high yield.
3. Verify the performance of displays so fabricated to specifications in SCS-501. Whereas there were many other details to be worked out, this was the essence of the technical strategy for the first phase of the program.

Actual progress towards meeting these goals is best summarized by photographs depicting the performance of the engineering samples in Figures 1.15 and 1.16. Their delivery to ECOM was accompanied by the contract required Test Report in November 1977. The conclusion of this exercise was that laboratory XY expertise had been transferred to pilot production with dedicated masks, only to the extent, however, that these pieces represented the best efforts at the end of some 20 months of activity. By December 1977, we had been unsuccessful in fabricating units meeting confirmatory sample requirements and any kind pilot production run seemed out of the question in the near future. However, both parties to the contract agreed that continuing the program for a further eighteen months was worthwhile in view of the substantial progress that had been made and the potential and increasing demand for the product.

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SAMPLE #1, SIDE A, CHARACTERS ON

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SAMPLE #1, SIDE B, CHARACTERS ON

Figure 1.15 Engineering sample No. 1 delivered to ECOM at the end of the first phase of the program in December 1977.

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SAMPLE #2, SIDE A, CHARACTERS ON

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SAMPLE #2, SIDE B, CHARACTERS ON

Figure 1.16 Enginerring Sample No. 2.

The second phase of the program was originally scheduled to run from May 1978 to April 1979 at a cost to ECOM of about \$250,000, supplemented again by a significantly greater infusion of funds by Westinghouse. What subsequently happened, however, was the October 1978 disclosure by Westinghouse to discontinue pursuit of this technology for commercial purposes and only to maintain such activity to honorably fulfill contract requirements. Consequently, the planned second phase subsequently evolved into a third, as shown in Table 1.5, which serves for defining the breakdown of phases in the remainder of this report.

TABLE 1.5 DEFINITION OF PROGRAM PHASES

Phase	Start	Finish	Approximate Cost to ECOM-ERADCOM
I	May '76	Dec '77	300,000
II	May '78	Oct '78	140,000
III	Oct. '78	July '79	80,000

At the time of entry into the second phase, both parties agreed to a much wider scope of deliverable items. During the first phase of this program, some progress had derived in the High Contrast Electroluminescent Display companion Contract DAAB07-77-6-2697 developing thin-film phosphor, whose performance advantages over powder were explained in the discussion of Section 1.1. Likewise, measurable progress in the development of an all-thin-film vertical scanner had recently been made. Consequently, the Phase I pilot run objective was ambitiously modified as shown in Table 1.6.

TABLE 1.6 CHANGES IN DELIVERABLE ITEM  
REQUIREMENTS FOR PHASE II,  
MAY 1978

DELETE: 20 piece pilot run (powder phosphor without TFT scanners at a  
rate of 10 per month)

ADD: 20 piece pilot run as follows:

Number of Pieces	Manufacture Rate	Description	
		Phosphor	Scanners
12	10 per month	Powder	No
3	not specified	Thin Film	No
3	10 per month	Powder	Yes
2	not specified	Thin Film	Yes

The strategy for the second phase of the program was highly directed at a convincing demonstration of manufacturability of the thin-film circuit matrices. The intention was to work the bugs out of this critical aspect of the task and develop the thin-film phosphor and scanner fabrication technology under the companion program DAAB07-77-C-2697. Expertise was to be transferred at a future appropriate time to this Manufacturing Methods program as it had been previously with the XY circuit fabrication approach. This technical strategy was accompanied by Westinghouse's investment in establishing Class 100 clean conditions for the automatic vacuum system environment. Airborne dirt was widely believed responsible for the numerous defects which had ostensibly prevented routine fabrication of operating circuits. Finally, in January 1978, Westinghouse formally adopted a Matrix Management structure<sup>(9-11)</sup> for the remainder of the program under which to maximize the benefits from its skills and management expertise in this field.

Results during the second phase of the program were very slow. One panel with relatively few defects was made by September 1978 and this is shown in Figure 1.17. Several other fairly high quality circuits were obtained from the automatic vacuum system but little meaningful testing to the full rigor of the confirmatory sample requirements spelled out in SCS-501 (Appendix A) was undertaken. On the contrary, high temperature (72°C) life-testing indicated how seriously deficient our powder technology was for this purpose. This was just the beginning of the emergence of a philosophy concerning certain technical myths in this field of endeavor. It is almost universally believed that the performance limits and manufacturability of thin-film transistors alone prevent copious production of the subject display. In practice, one finds that making uniform, reproducible transistors adequate to the immediate task is by far the easiest part of the entire operation.

In spite of, or because of, the frantic activity applied to the program in 1978, Westinghouse made its decision in September not to pursue this technology for its own purposes. In spite of many alleged breakthroughs, the relatively primitive and labor-intensive laboratory

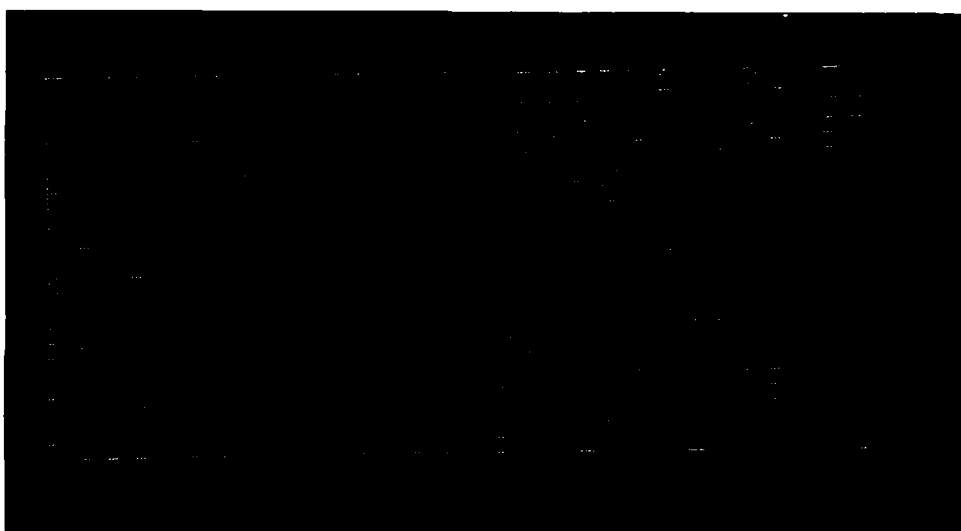


Figure 1.17      Example of the state-of-the-art at the conclusion of Phase II.

XY method remained as productive as the pilot facility as far as producing components of any legibility was concerned. However, a corporate commitment was made to continue operations to fulfill as honorably as possible our contractual obligations. This was done under Phase III of the program, which saw new management and major changes to the overall approach. For this reason, the entire next section is devoted to the strategy for Phase III. This seems appropriate since much of the technical detail described subsequently relates to Phase III activity exclusively even though, naturally, it draws heavily from the efforts applied and successes achieved earlier in the program.

#### 1.5 Phase III and a New Technical Strategy

The entry into Phase III in October 1978<sup>\*</sup> under new management was made with the institution of hearings. Former program participants from both the engineering and technical support ranks were quizzed exhaustively as to their own assessment of the technical status of program work and as to their technical recommendations. What follows now is a review of the findings of those hearings. This is supplemented by a description of a technical strategy which was formulated for the remainder of the contract period with the knowledge and consent of the customer.

The material relating to the findings of the hearings has been segregated into five subsections, dedicated to sequential facets of the display manufacturing activity. These are:

- Thin Film Circuit Production
- Automatic Circuit Testing
- Powder Phosphor Application
- Encapsulation
- Final Test.

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<sup>\*</sup>This was over two years after the beginning of contract activity and some six months from its final scheduled termination.



Each of these subsections reviews the October 1978 status, the major problems, and the then-recommended approach as perceived at the hearings. These are followed by Subsection 1.5.6, dealing exclusively with the Phase III strategy. To some extent this material presupposes the reader's knowledge of some details of the technology. The writer has chosen, however, to risk the discomfort of a few members of his audience in order to provide a comprehensive overview of the execution of the program before bombarding them with technical minutiae. The gross features of the manufacturing approach have already been described in Figure 1.12.

#### 1.5.1 The Status of Circuit Manufacturing in October 1978

This activity refers to the gamut of operations running from the acquisition, testing and cleaning of masks and clean glass substrates, their installation in the vacuum system, the thin-film deposition sequence, unloading and annealing the circuits and preparing the system for the next run. ("Circuit" in this context means the glass-circuit composite ).

Status. The vacuum deposition facet of this activity was fully operational. With its former work force of typically two full-time engineers and four technicians, the approximate throughput was 18-20 substrates per month. Of these, about 10-14 were deemed to be confirmatory sample grade (CSG). However, each of these substrates reportedly received a mix of about 16 engineering or technician man-hours for the repair of typically 3-4 "shorts", 3-4 "opens" and the "scratching out" of 3-4 defective transistors. These counts were most likely understated. A most significant technological achievement was the consistent and reproducible characteristics of the transistors fabricated.

Problems. Problems were segregated into two groups: those affecting yield without regard to throughput and vice versa. Of course, this segregation was somewhat arbitrary with certain problems affecting both yield and throughput.

In order of decreasing severity, those identified in the first group were:

1. Excessive power transistor leakage
2. Inadequate pre-deposition glass substrate cleaning
3. Inadequate mask cleaning and inspection
4. Pattern defects due to imperfect mask pre-alignment and in-process registration
5. Inadequate transistor voltage capability and excessive leakage ("instability")
6. Faulty handling procedures.

In summary, there was substantial disagreement concerning items 1 and 5 above, even among personnel intimately acquainted with this activity. It is clear we really had not fully translated required optical performance of the panel into electrical test requirements of the individual transistors. However, it was widely agreed that items 2, 3, 4 and 6 had received totally inadequate attention relative to their importance and, were this situation to be corrected, "problems" 1 and 5 would likely disappear or be substantially alleviated.

Problems more generally related to throughput, again in decreasing order of severity, were:

1. Multiplicity of steps
2. Less (4 to 5) than total utilization of machine capacity (8 substrates per run)
3. Slow evaporation rates
4. Constraints imposed by the existing design and construction of the vacuum deposition system.

Items 3 and 4 above are factors we really cannot hope to do anything about in the near future and are not really limiting with our existing technology. Item 1 was of major concern and was really not intractable.

The fabrication of each circuit then required a total of 45 steps and took over 4 hours. This burden derived from an obsolete circuit layout geometry which also related to the "yield" group of problems. Item 2 above results from the dedication of one substrate position for mask precoating and source pre-conditioning, and two positions to in-process mask "mopping". A separate factor was monitoring-crystal life. These were then used in a 100% duty cycle during  $\text{Al}_2\text{O}_3$  depositions.

Recommended Approach. One important way in which both yield and throughput problems could be greatly alleviated was redesign of pattern layout geometry and mask engineering. There was general concurrence in this viewpoint. The 45 step - 4 hr sequence was believed replaceable by a 25 step - 2-1/2 hr sequence. In the past, we had shied away from this seemingly forbidding task for two main reasons:

1. Its elapsed time requirement
2. Its cost - probably \$5-10,000 (labor and materials).

A commitment to this particular task was believed likely to have a profound impact on technological progress - so much as to render even the "unused capacity" feature inconsequential.

#### 1.5.2 The Status of Automatic Circuit Testing in October 1978

Automatic testing in this context is the process wherein the electrical characteristics of annealed substrates are comprehensively measured, recorded, and graphically presented by computer. Its purpose is two-fold: on the one hand, it is a process control link, providing feedback to the vacuum system operation by detecting system malfunctions or otherwise abnormal operating conditions. On the other, it grades substrates so that minimal effort is lost in the application of phosphor to substrate circuits of less than acceptable equality. A further potential use of this equipment is automatic repair such as short detection and clearing.

Status. All the hardware for this system had been assembled and was 100% operational. A supporting software package controlled the test sequence and provided summary test data in a form which permitted quick appraisal of circuit quality by the operator. Each circuit required less than 5 minutes set-up time and the duration of the data-acquisition mode without human intervention was about 10 hours. Approximately \$90,000 had been invested in this system. Major disagreement existed as to whether it was an essential component of a commercial production facility, either in its present configuration or in some variation. However, its usefulness for the purpose of the pilot runs called for by the contract was definitely disputed. Use of this equipment was not specifically required by the contract. At the maximum rates of production we then presently envisaged — about 5-6 substrates per week — one school of thought maintained testing could be done manually more efficiently.

Problems. The reason this equipment had not functioned as planned concerned the nature of the substrate-circuit system being tested. To work properly, the circuit would have had to be deposited on glass with flatness specifications which were not readily available. The existing pattern had further geometrical and physical features, not readily accommodated by the probe assembly of the tester, such as fragility of the metal films being probed and run-out (general geometrical imperfection) of the pattern.

Recommended Approach. Continued use of the full comprehensive testing capability of the automatic tester was not a high priority item for the purpose of meeting the confirmatory sample requirement. Also, it probably was not essential for pilot runs of the limited scope called for by the contract. It appeared, however, to be of significant use in a limited mode of automatic scan for bus-bar continuity, for example. In a manual step mode, it could also assist in spot checking of transistor characteristics.

### 1.5.3 Status of Powder Phosphor Application in October 1978

The input to this step of the manufacturing sequence is the substrate with its circuit, repaired or otherwise. The step is complete after the phosphor layer is applied, a brief light-up test is conducted, repairs are made, if feasible, and the substrate is delivered to encapsulation.

Status. At present, the former standard process was being changed from one in which phosphor particles suspended in a starch solution are sprayed onto the panel to a so-called "hybrid technique." The existing spray starch vehicle had previously produced samples which were only marginally bright in the 200 fc ambient specified for the viewability test. In addition, it was grossly inadequate for the 72°C, 600 hr life test. The new hybrid process, then in its final verification phase, has resulted from intensive activity initiated in June 1978. The voluminous technical data, progress, and setbacks in this effort had been extensively documented in the minutes of the so-called phosphor group meetings held weekly since then. Every indication is that the new hybrid process could meet the demanding 72°C, 600 hr life test. However, as with the original spray-starch vehicle, yield depended predominantly on the quality of the transistors, in particular, their ability to stand off typically 110 vrms in the generation of a dark element. Consequently, of the remaining 10-14 substrates delivered for phosphor per month, only about 4 remained confirmatory sample grade after phosphor application.

Problems. The single then perceived problem concerning powder phosphor application was incomplete verification of the new hybrid process. Optimism stemmed from the detailed and extensive understanding of factors limiting phosphor performance gained since June by working with so-called Nesa Chips and Postage Stamps. However, it had been observed that when Riston lifts and has to be stripped, the solvent used has the habit of damaging silver epoxy repairs. The lifting tends to start on repaired regions, especially at the edges.

Recommended Approach. It was generally felt that the new hybrid process verification should be completed and that panel legibility and performance could be subsequently further improved if desired by the so-called "second-level" procedure. Black-surround seemed to have nothing to offer powder phosphor procedures within the scope of this program. These last two issues were somewhat controversial.

#### 1.5.4 The Status of Encapsulation in October 1978

This step refers to activity wherein two phosphor coated circuits are mounted on a glass backing and are sealed by a front glass plate attached with transparent epoxy. This is essentially the final hardware product defined by program requirements.

Status. Verification of our favored process featuring "Stycast" epoxy and a silicon rubber edge seal had been delayed by lack of availability of EL-coated half panels and also, to a certain extent, to the only recent inaugural operation of essential test facilities. Nonetheless, the procedure did produce an assembly which is mechanically and aesthetically "excellent." There was a good indication that, without power, the panel survived testing in the specified hot/humid environment. We had no indication this process was adequate for protection of the phosphor-binder sub-system in the 72°C life test, that is - adequate to reproduce the dry box testing used to verify the phosphor application step.

Problems. The overall problem here was the absence of a verified encapsulation procedure. We reasonably assumed that, were a copious supply of working half-panels available, we would observe failures of the package under one or more of the demanding tests which must be passed. However, we also assumed that the cause of these failures could be systematically identified and dealt with in a way similar to that in which the so-called 72°C phosphor life problem was resolved earlier.

Recommended Approach. Pending the availability of an adequate supply of CSG half-panels, it was believed that the encapsulation

procedure should be verified immediately, and as convincingly as possible, either with reject half-panels or with similar and readily available substitute components. Subsequent activity should naturally focus on any failures so observed.

#### 1.5.5 Status of Test and Evaluation in October 1978

This activity concerns the one-time task of constructing the panel test equipment and the institution of the ongoing tests themselves. There are basically six categories of test, details of which are spelled out in the written contract. These are:

1. Shock and vibration
2. Humidity
3. Altitude
4. Temperature
5. Viewability
6. Life

Status. All facilities necessary for the conduct of the above tests had been assembled and were fully operational. In addition, software for conducting the complex viewability test had been written and tested. However, little actual testing had been completed due to the unavailability of product to test. Two panels had been subjected to altitude and one to shock and vibration. All three passed those tests.

Problems. There was a possibility that the design of the viewability exerciser unnecessarily stressed the power transistors. We had previously damaged panels electrically during viewability tests.

Recommended Approach. Other than a determination of the possible problem mentioned above, no further actions were recommended at that time. It was believed a good idea, if possible, to locate all facility test equipment in a single area to minimize handling losses, which did not appear minimal.

#### 1.5.6 Technical Strategy Adopted for Phase III in November 1978

The strategy presented here was formulated to address the issues raised in Subsections 1.5.1 through 1.5.6 above. The general approach was to switch emphasis to pilot manufacturing as opposed to product development. We had earlier verified that the product could, by and large, be made to perform as intended. Nonetheless, it could only be made in a very slow labor-intensive process with very low yield. The thought was that if something more closely resembling a pilot manufacturing line could be established, the technological momentum of higher throughput, more rapid process feedback, and consequently greater process control would begin to provide a meaningful indication of the basic and overall manufacturability of the product. This was believed to be more consistent with the intended spirit of the funded program.

The elements of the technical strategy formulated in November 1978 were the following:

1. Redesign the circuit layout and procure revised masks during November to February 1978; these masks to feature Kovar-cored construction.

The reasons for this strategem were the following:

- (1) The existing pattern geometry reflected our state-of-the-art as it was in this field almost three years earlier. Extensive experience and many new ideas had emerged during the interim period regarding its improvement in terms of providing higher throughput and yield ratio.
- (2) We had worked with the existing pattern for over two years with only limited success in producing a unit which met viewability requirements. It was, therefore, unlikely that without drastic action of this nature we were going to radically improve output, particularly



with only one-fifth of the original manpower and with a time limitation of less than nine months. In spite of further generous Westinghouse support supplementing remaining customer funds, it was evident that the program manning level would have to be drastically cut back to the stated level.

(3) We had firm evidence that Kovar-cored masks have much superior performance compared to our then-existing Be-Cu cored ones. Had we wanted to take advantage of this experience, even with the existing pattern, much of the time and money associated with a total redesign effort would have to be expended anyway. The obvious reason for not having undertaken this task earlier was the cognizance of the time constraint; we had only three months to complete what had previously taken over one year.

2. Develop a nickel evaporation expertise to replace the former aluminum-copper-chrome 3-metal system.

The main purpose of this approach was to take maximum advantage of the investment in the redesign of the masks. Whereas the mask redesign itself offered product and process simplification, here was an opportunity to reduce further the complexity of the manufacturing system. In addition, one problem identified at our hearing was the failure vulnerability of the copper link previously used to attach gold-indium transistor source and drain pads to the aluminum bus-bars. Another was the relative "unrepairability" of the aluminum bus-bars. The reasons we selected nickel were the following:

- (1) We had previously had at least some limited experience with it on other projects.
- (2) It was not physically, chemically, or metallurgically incompatible with any other of the deposition materials we were going to continue using.

(3) Electrical conductivity was reasonable.

(4) Nickel films were potentially less vulnerable to mechanical damage.

The problems which we had to keep in mind were as follows:

(1) Nickel's reputation for not sticking to glass.

(2) Higher temperature induced during the evaporation.

This activity was scheduled to run in parallel with the mask redesign effort. The intention was to converge towards inaugural production with the new design and the new material in early March 1979 leaving time for debugging before having two clear months to run in a production mode. In view of the uncertainty, fall-back positions were to use the new material with original mask design and, failing that, the original masks were to be used with the original materials. It was not possible to use the original materials with the new masks without a modification. This was a risk we felt we could live with.

3. Develop addressing electronics to reproduce recent experience demonstrating lower source and gate drive voltages also in the November-April 1979 time period.

In the development of a flat panel display for TV images under sub-contract with MIT Department of Architecture, Westinghouse found that substantially improved drive and performance characteristics were obtained from the display by separating in time the video write and phosphor excitation operations. Not only were substantially reduced logic voltages found adequate, but turn-on of power transistors during voltage stress was avoided and the effective retention time of the memory capacitor in the elemental circuit was extended from the nominal frame time of 1/60 second to better than 30 seconds.

We determined, therefore, that a low frame rate without flicker should consequently be obtainable with the DMD display by use of this technique. This, in turn, would allow the peripheral circuit power to become a very small fraction of the total panel power demand,

except at low brightness settings. Further, it would permit use of relatively low data rates (less than 100K bit/sec) for panel refresh.

Another advantage that was expected to derive from the new drive method related to compensation for transistor drift. TFT transistors made to date showed a degree of short- and long-term drift of threshold voltage under positive or negative gate bias conditions which greatly exceeded that shown by modern silicon MOS transistors. This drift stemmed from carrier traps and ionic drifts and, though troublesome, it was reversible and could be characterized by constant parameters. Considerable effort would probably be required to reduce this drift to a negligible value for all applications. Until such a time that TFT driftiness is eliminated, undesirable effects in TFT circuitry resulting from the driftiness could be avoided by use of dynamic circuits which periodically exercise the transistors in the gate-positive and gate-negative modes. At a lower frame rate, such as 5 Hz for example, a relatively large fraction of the total line time can be spent for this purpose, and a reset duty cycle of 0.8% is easily provided.

4. Characterize and, if necessary, modify packaging technology beginning immediately and continuing until April 1979.

It was not known in October 1978 how good or otherwise our existing encapsulation methods would perform under life testing as specified by the contract. Therefore, our first task was to evaluate what we had. If the results were negative, we were to proceed with development of this technology until the regular production phase of the program was to begin in early May. Specific objectives in terms of performance could not be meaningfully formulated because unlike other tasks in this strategy, there was no indication that the required maintenances were technically attainable. On the other hand, development activity was naturally to cease were the required performance demonstrated sooner.

5. Reassess role of automatic circuit testing and reduce its scope to a level more commensurate with existing program needs.

Our hearings had revealed controversy as to the ultimate usefulness of the existing concept of automatic circuit testing. The technical nonfeasibility of the approach was, however, fairly clear. On the other hand, the hardware system used for operation was clearly well suited to a related task constituting a bottleneck in pilot production, namely

- bus-bar open and short location prior to cleaning
- transistor evaluation for process control.

The new mask design was specifically formulated to provide a more testable and fault-clearable product. Whereas the original concept of automatic circuit testing was intended to embrace capability for dealing with the two points above, its sophistication in being designed to do much more than these essential chores had rendered it technically too demanding on the product and process. Therefore, in summary, our intention was to back off in scope and sophistication and apply the general concept to a more critical need, more limited in nature.

This strategy with its five elements was followed closely through the third and final phase of the program, possibly with one exception. During early 1979 it became evident that thin-film electroluminescent phosphor technology was quickly rendering powder phosphor obsolete. However, there remained nothing on the horizon to supplant thin-film transistor switching of an active matrix for driving an array of phosphor elements. Consequently, the customer requested that no further effort towards the respectable performance we recently had coaxed from our powder phosphor methodology should be expended. All available resources were to be directed towards fabricating the essential thin-film transistor switching matrices. Partly because of this, and partly because of the stark reality of the overall situation, all the deliverable item requirements shown in Table 1.5 were replaced by eight displays meeting the former confirmatory sample requirement, and

not made at any specified rate. The powder phosphor processing was largely a medium with which to evaluate circuit fabrication technology. This was to be directed subsequently at the ultimate product, a thin-film transistor addressed thin-film electroluminescent display.

## 2.0 COMPONENT DESIGN

### 2.1 Fundamental Configuration

The device which forms the basis of this Manufacturing Methods and Technology Engineering Program is a 256 character flat panel alphanumeric display. The display has an active area of 6.56" by 2.88" and the total device is 7.06" by 3.38" and is approximately 0.125" thick. The mechanical arrangement of the device is shown in Figure 2.5. In order to manufacture the display in the available Pilot Manufacturing Facility, it was necessary to form the display surface in two parts. The Pilot Manufacturing Facility can handle TFT circuits up to a maximum size of about 4" by 4". Thus, the display is made from two identical 3.55" by 3.40" substrates.

### 2.2 Geometrical Features and Contacting

The active display area of the panel consists of 222 x 77 (17,094) elements. In the horizontal direction, the elements are spaced on 750  $\mu$ m centers, and in the vertical direction they are spaced on 950  $\mu$ m centers. Each element has a lit area that is rectangular in shape and is equal to or greater than 0.015" by 0.021". If it is found necessary to increase the lit area to improve viewability or brightness, this can be accomplished by using a "second level" process. The display medium is a powder AC electroluminescent (AC-EL) phosphor. The phosphor, which emits in the green region of the visible spectrum, is driven by a thin film transistor matrix. Each display element is controlled by two transistors, a capacitor and a set of interconnecting busbars. Every element is addressable through the edge finger contacts. Typical signal voltages are  $\pm$  30V, and typical power voltages are 50 to 100 Vrms. Power (5 to 10 kHz, either square wave or sinusoidal) is supplied to the phosphor through edge contacts, and the device is grounded through corner contacts. Brightness control is achieved by EL drive voltage or pulse width modulation.

The circuit schematic showing six adjacent display elements appears in Figure 2.1. The design layout is delineated in Figure 2.2 and a photograph of two elements of a fabricated surface is illustrated in Figure 2.3

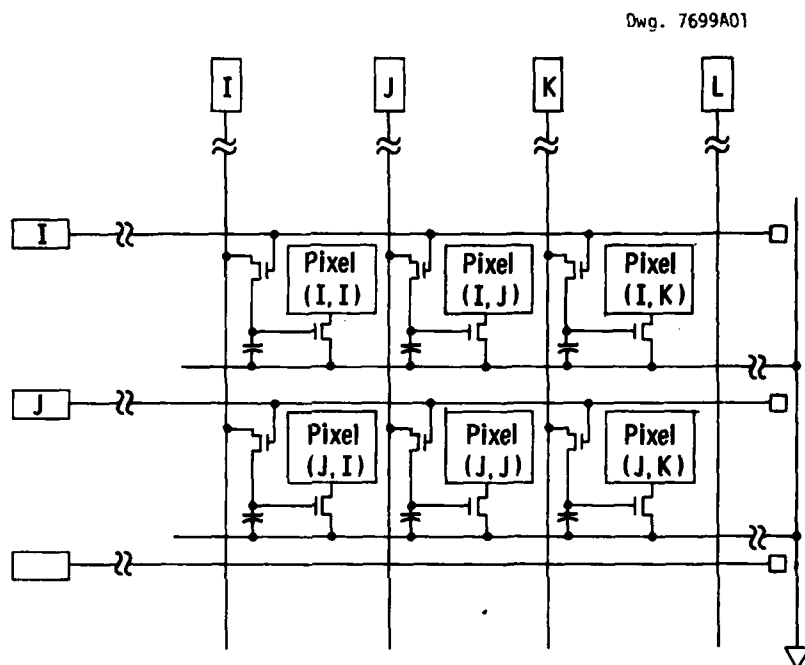


Figure 2.1 Bus-bar visualization for new layout.  
(see also Figure 7.1)

### 2.3 Mechanical Construction

In cross section the device consists of an active matrix area with edge contacts corresponding to the overall 7.06" x 3.38", which will be 0.05" thick. A front cover plate and back reinforcement plate are sealed and laminated onto the active matrix modules (half panels) so that the total display thickness is about .150".

For purposes of discussion, the subsequent steps are called "packaging processes." They involve the coating of the thin film circuit with a laminar photoresist to insulate and passivate the active components. Following this the circuit is sprayed with phosphor in a high dielectric constant binder, and then a transparent top electrode is applied. Finally, the display is sealed. A detailed description of the packaging process is given in Section 8.2.

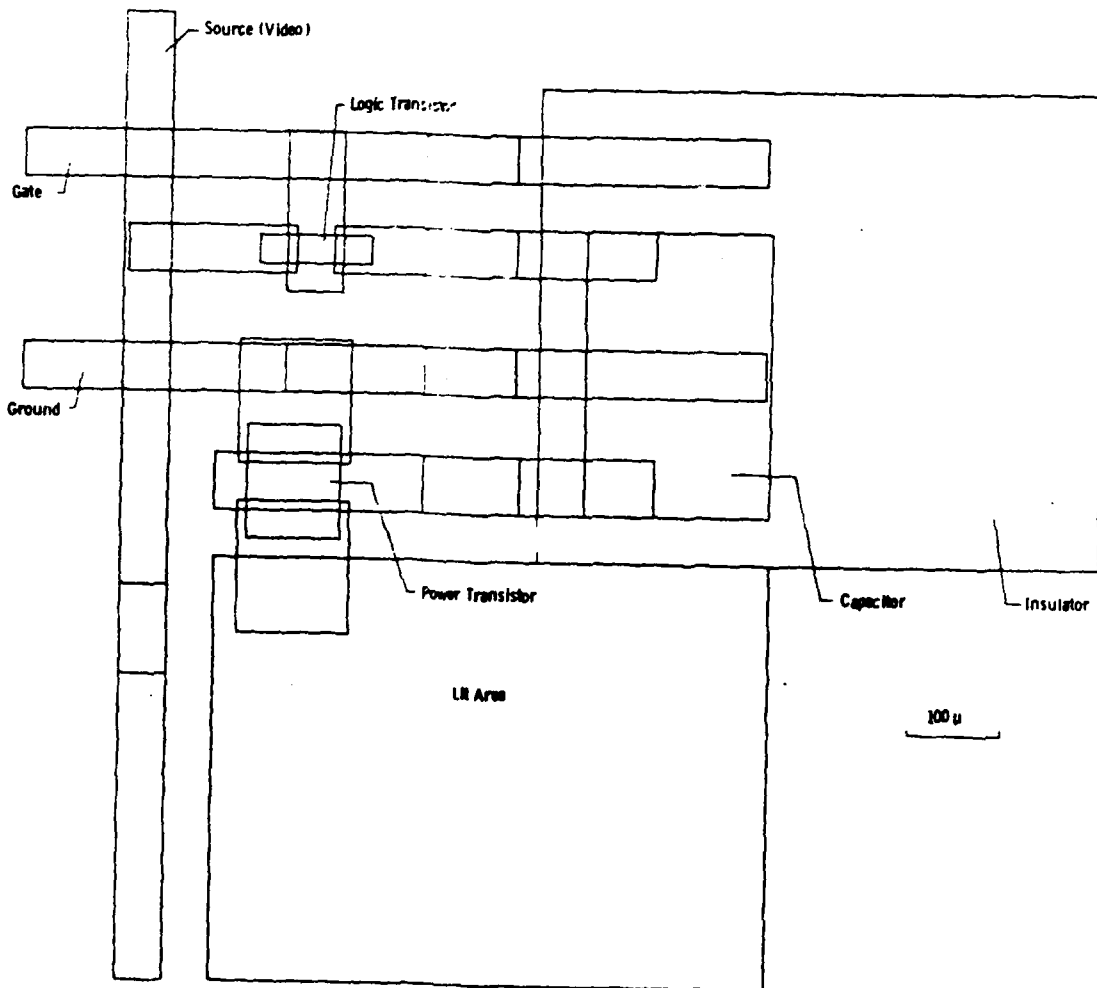


Fig. 2.2 Artwork of the elemental circuit of the new design



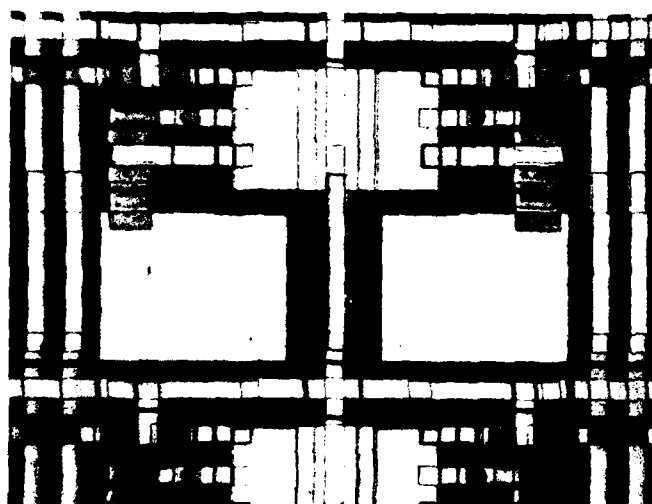
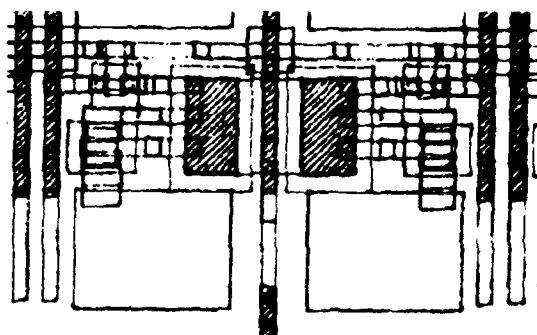


Fig. 2.3 The layout featured in Phase 2

## 2.4 Theory and Analysis of Operation

### 2.4.1 The Thin Film Transistor

The theory of the operation of TFT s for thin semiconducting layers up to the current saturation is treated by Borkan and Weimer<sup>(13)</sup> under the assumptions that the mobility of the charge carriers throughout the conducting channel is independent of the gate voltage and that the gate capacitance is also independent of the gate voltage, i.e., there is no trapping of carriers at the semiconductor-insulator interface. Current saturation at a drain voltage approximately equal to the gate voltage. Operation of the TFT at higher drain voltages result in a gradual (and in some cases, zero) increase in the drain current. Models to explain the behavior in the saturation region invoke the concept of a space charge limited current in the drain region. The high resistance of the channel in this region causes most or all of the voltage drop to appear across this zone and as the drain voltage increases, the length of the space charge region increases so that current, which must be continuous along the channel, increases less than linearly (or not at all). Solving the problem in the saturation region requires the solution of the Poisson equation and the result must be fitted to the I-V characteristic in the unsaturated region. This has been difficult to do in a meaningful way because of the strongly approximate character of the models involved, especially with respect to the effects near the drain end of the TFT.

A much more satisfactory analysis and one that is particularly suited to our TFT s (with one caveat) was provided by Geurst.<sup>(12)</sup> The 'caveat' is that whereas our TFT s are made so as to have very little gate to source-drain overlap, Geurst's model assumes an infinite gate overlap. This will limit the model to low frequency operation. In other respects, viz., an infinitesimal semiconductor layer with two double insulators and two gates, the model is expected to fit our TFT's.

Figure (2.4) shows the model of a TFT used by Geurst in his analysis.

Dwg. 7714A25

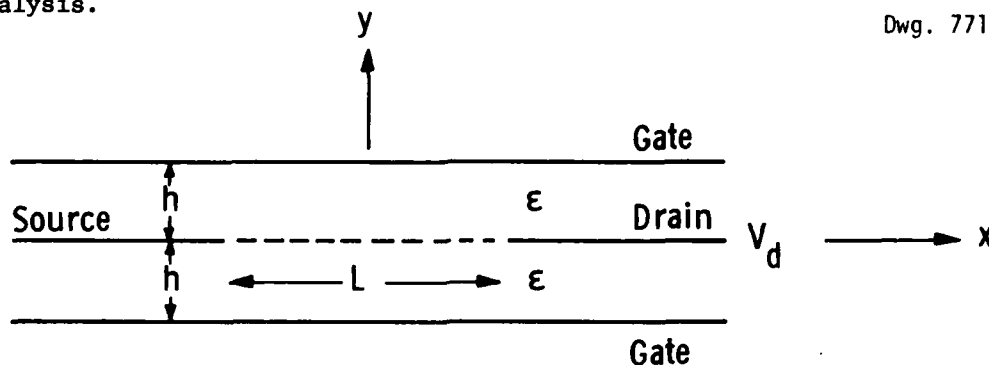


Fig. 2.4 Geurst TFT Model

The two gates are assumed to be tied together in operation and all voltages are relative to the source electrode which is taken to be ground.

The linear current in the channel is

$$I = \sigma v \quad (1)$$

where  $\sigma$  is the surface charge density in the channel and  $v$  is the carrier drift velocity, each of which is a function of position,  $x$ , in the channel. The current, of course, is independent of  $x$  but is a function of the gate and drain voltages.

The surface charge density,  $\sigma$ , can be determined from the familiar expression

$$\rho = \text{div}(\mathbf{D}) \quad (2)$$

applied to an infinitesimal layer.

$$\sigma = \rho t = t \frac{\partial D_x}{\partial x} + D_y^+ - D_y^- - q \frac{N_o}{L} \quad (3)$$

where  $N_o$  is the number of carriers initially present in the semiconductor and  $q$  is the absolute value of the charge. Negative  $N_o$  corresponds to the number of empty traps. The first term on the right hand side goes to zero as  $t \rightarrow 0$ . For finite thickness, the first term will still be very small relative to the others unless  $\frac{\partial D_x}{\partial x}$  can get very large, which would appear to be a possibility. We will, however, follow Geurst's analysis and show that the  $t \rightarrow 0$  limit leads to meaningful results and leave the first term effects for further study.

$Dy^+$  and  $Dy^-$  represent the electric displacement vectors in the insulator on either side of the channel. Equation (3) can be reduced to

$$\sigma = 2\epsilon \left( Ey^+ + \frac{V_o}{h} \right) \quad (4)$$

where  $2\epsilon V_o/h = -qN_o/L$ ,  $\epsilon$  being the insulator dielectric constant. The factor of 2 comes from the even symmetry of the structure. The double gate just doubles the induced charge.

The drift velocity,  $v$ , depends upon the component of the electric field along the  $x$  direction in the semiconductor.

$$v = \mu Ex \quad (5)$$

where  $\mu$  is the electron drift mobility. The current is then given by

$$I = -2\mu\epsilon \left( Ey^+ + \frac{V_o}{h} \right) Ex \quad (6)$$

Since  $Ex$  is continuous across the channel-insulator interface, Equation 6 can be written

$$I = -2\mu\epsilon \left[ \left( Ey + \frac{V_o}{h} \right) Ex \right]^+ \quad (7)$$

This says that the current in the channel is determined by the values of the components of the electric vector at the upper side of the semiconductor channel. Equation 7 can therefore be regarded as a boundary condition on the electric field in the insulator. An additional boundary condition is

$$Ex = 0 \quad (8)$$

on all the source, drain and gate electrodes. Equation 7 is seen to be a generalization of the current equation derived in the "gradual approximation" by Borkan and Weimer.<sup>(13)</sup> Near the source electrode the electric field is almost entirely in the transverse direction, i.e.,  $Ex \ll Ey$ . Replacing  $Ex$  by  $-\partial V/\partial x$  and  $Ey$  by  $-(V_g - V(x))/h$ , we get the approximate expression valid for small drain voltage  $V_d$ ,

$$I = -2 \frac{\mu\epsilon}{h} \left\{ V_g - V(x) - V_0 \right\} \frac{\partial V(x)}{\partial x} \quad (9)$$

where  $V_g$  is the gate potential measured with respect to the source. Equation 9 is seen to be equivalent to Borkan and Weimer's.

Geurst recognized that if the electric field vector is represented by a complex number

$$\xi = E_y + iE_x + V_0/h \quad (10)$$

then  $E$  is an analytic function since the electric field satisfies the Cauchy relations

$$\frac{\partial E_y}{\partial x} = \frac{\partial E_x}{\partial y} \quad (11)$$

and

$$\frac{\partial E_y}{\partial y} = \frac{\partial E_x}{\partial x}$$

which can be seen by substituting  $E_x = \frac{\partial V}{\partial x}$  and  $E_y = \frac{\partial V}{\partial y}$ .

The second equation gives

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0 \quad (12)$$

which is just the Laplace equation that the potential must satisfy in the charge-free insulator.

Given Equation (10), we can write

$$\xi^2 = \left( E_y + \frac{V_0}{h} \right)^2 = E_x^2 + 2i \left( E_y + \frac{V_0}{h} \right) E_x \quad (13)$$

The boundary condition given in Equation 7 can be written

$$I = -\mu\epsilon \text{Im}(\xi^2) \quad (14)$$

where  $\text{Im}(\xi^2)$  stands for the "imaginary part of  $\xi^2$ ."

The boundary value problem is now changed to one that is simpler to treat by making coordinate transformation that changes the

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MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY--ETC(U)  
FEB 80 M W CRESSWELL, P R MALMBERG, J MURPHY DAAB07-76-C-0027

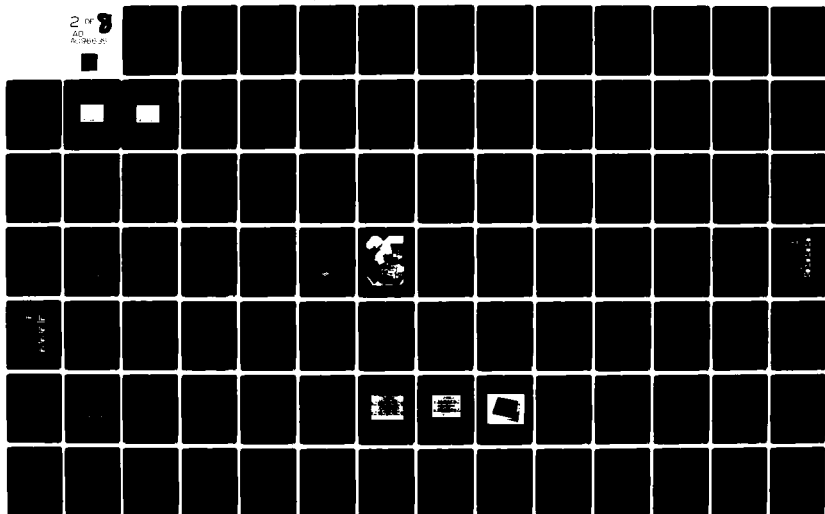
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rather complicated boundaries of Fig. 2.5(a) into a much simpler one (2.5b).

By representing a point in Fig. 2.5(a) by the complex number

$$z = x + iy \quad (15)$$

and defining the transformation

$$W = e^{\frac{iz}{h}} = u + iv \quad (16)$$

we make a one to one transformation of a point in the  $(x,y)$  space onto a point on the  $(u,v)$  plane. The mapping is shown in Fig. 2.5 with selected point mappings given in Table 2.1. One can see that the transformation maps a line of constant  $y$  in Fig. 2.5(a) onto a ray emanating from the origin in Fig. 2.5(b). The line  $x = -\infty$  maps onto the point at the origin.

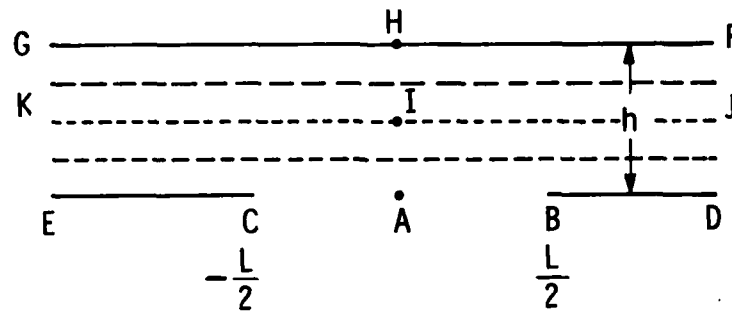
TABLE 2.1

CONFORMAL MAPPING OF FIGURE 2a INTO FIGURE 2b  
 USING THE TRANSFORMATION  $w = \mu + iv = e^{\frac{\pi}{h}(x+iy)}$

<u>Point</u>	<u>Coordinates in 2a</u>	<u>Coordinates in 2b</u>
	$(x, y)$	$(\mu, v)$
A	$(0, 0)$	$(1, 0)$
B	$(L/2, 0)$	$(e^{\frac{\pi L}{2h}}, 0)$
C	$(-L/2, 0)$	$(e^{-\frac{\pi L}{2h}}, 0)$
D	$(\infty, 0)$	$(\infty, 0)$
E	$(-\infty, 0)$	$(0, 0)$
F	$(\infty, h)$	$(-\infty, 0)$
G	$(-\infty, h)$	$(0, 0)$
H	$(0, h)$	$(-1, 0)$
I	$(0, h/2)$	$(0, 1)$
J	$(\infty, h/2)$	$(0, \infty)$
K	$(-\infty, h/2)$	$(0, 0)$



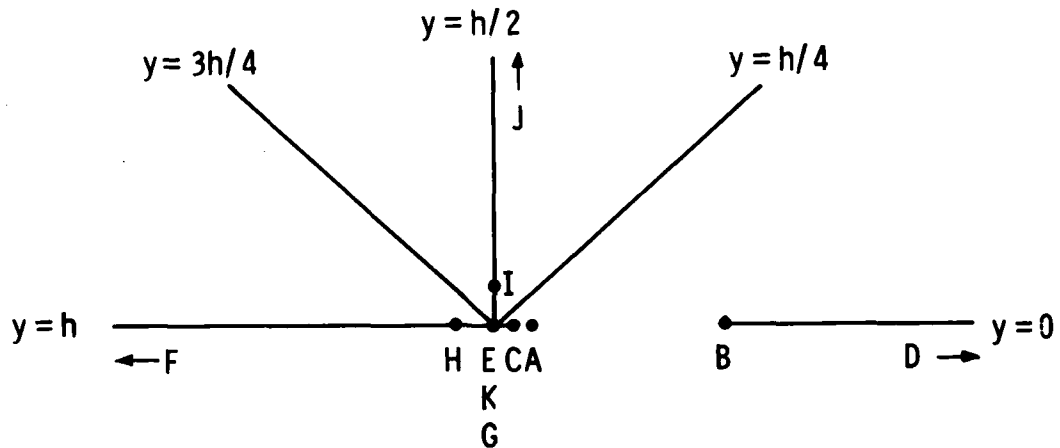
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$$z = x+iy$$

FIGURE 2.5(a)

Complex plane representing upper half of TFT



$$w = u+iv = e^{\pi z/h} = e^{\left(\frac{\pi x}{h}\right)} \cos\left(\frac{\pi x}{h}\right) + i e^{\left(\frac{\pi x}{h}\right)} \sin\left(\frac{\pi y}{h}\right)$$

FIGURE 2.5(b)

Transformed plane showing that the lines  $y = 0$  and  $y = h$  map, respectively, onto the positive and negative real axes in  $w$  space. The line at  $y = h/2$  in the insulator maps onto the imaginary axis.

The complex function  $E^2(z)$  is transformed into the complex function  $F(\omega)$  defined by

$$F(\omega) = E^2(z(\omega)) . \quad (17)$$

Since  $E$  is an analytic function, it follows that  $F(\omega)$  is also an analytic function. The boundary conditions satisfied by  $F$  are

$$\text{Im } F = 0 , \quad -\infty < \mu < \lambda \quad (18)$$

$$\text{Im } F = \frac{I}{\mu \epsilon} , \quad \lambda_1 < \mu < \lambda_2 \quad (19)$$

$$\text{Im } F = 0 , \quad \lambda_2 < \mu < \infty . \quad (20)$$

Aside from these boundary conditions there are other requirements that help to define the solution. Since the gate electrode overlaps the source and drain electrodes to an infinite extent in this model, it follows that at large distances from the channel, the electric field must be vertical as  $x \rightarrow \infty$  and  $x \rightarrow -\infty$  from which we get the auxiliary conditions

$$E_y \rightarrow \frac{V_g}{h} \quad \text{as } x \rightarrow -\infty, \quad 0 < y < h \quad (21)$$

and

$$E_y \rightarrow \frac{V_d - V_g}{h} \quad \text{as } x \rightarrow +\infty, \quad 0 < y < h . \quad (22)$$

These last conditions imply

$$\text{Re } F \rightarrow \left( \frac{V_o - V_g}{h} \right)^2 \quad \omega \rightarrow 0 \quad (23)$$

$$\text{Re } F \rightarrow \left( \frac{V_d - V_g + V_o}{h} \right)^2 , \quad \omega \rightarrow \infty . \quad (24)$$

By  $\omega \rightarrow 0$  we mean  $\mu \rightarrow 0$  and  $v \rightarrow 0$ , and by  $\omega \rightarrow \infty$  we mean either or both of  $\mu \rightarrow \infty$ ,  $v \rightarrow \infty$ . The line  $x = \infty$  maps onto the infinite half circle in the upper half of the  $\omega$  plane so that  $\omega \rightarrow \infty$  implies any point on that circle.

This is a good point to discuss the choice of the model with source-drains and gate extending to infinity. Because the field is strictly vertical in those limits, we have a convenient way of expressing the auxiliary boundary conditions in terms of the drain and gate voltages viz. Eq. (21) and (22). A more complicated situation exists when the gate is aligned with the channel. In other words, when there is no gate-to-source or gate-to-drain overlap. Without the advantage of the vertical field at infinity, we must replace the simple auxiliary conditions [Eq. (21) and (22)] by the more formal expressions

$$V_g = \int_{\text{source}}^{\text{gate}} (E_x dx + E_y dy) \quad (25)$$

$$V_d - V_g = \int_{\text{drain}}^{\text{gate}} (E_x dx + E_y dy), \quad (26)$$

where  $c$  denotes any path between the electrodes. Of course, the integrals are independent of the path chosen but depend upon the end points.

The solution to the problem of the aligned gate (or anything other than the infinite gate) is somewhat more complicated, but nevertheless tractable; however, we shall follow Geurnst and pursue the infinite gate solution.

An analytic function is completely specified within an arbitrary boundary on the complex plane if it is specified at all points on the boundary. The general solution of the boundary value problem specified by Eq. (18) through (24) is

$$F(\omega) = -\frac{I}{\mu\epsilon\pi} \log \frac{\omega - \lambda_2}{\omega - \lambda_1} + \frac{A_1}{\omega - \lambda_1} + \frac{A_2}{\omega - \lambda_2} + B. \quad (27)$$

Examining Eq. (27) we can see that on the real axis it is real everywhere but in the space between  $\lambda_1$  and  $\lambda_2$ , where it becomes complex with an imaginary part equal to  $\left[ \frac{-I}{\mu\epsilon} \right]$ . The remaining terms are strictly real on the real axis.

The remaining terms require some discussion. Any analytic function that fits the boundary conditions is allowed and is acceptable, provided it does not lead to unphysical effects. One certainly could not object to a constant B, and we will see that it is needed. Functions with poles e.g.  $\left(\frac{1}{(\omega - \lambda)} n\right)$  are analytic everywhere except right at the pole itself; however, anything but simple poles i.e.  $\frac{1}{\omega - \lambda}$  would lead to infinities in the field near region of the pole, and so must be excluded. Since the electric field is related to our  $F(\omega)$  function in a square root fashion, the simple pole will lead to a square root singularity and that is integrable, so that the potentials remain finite everywhere.

We have put poles at  $\lambda_1$  and  $\lambda_2$  on the real axis. These are the only two places that one can have singularities since they are the only transition points in the problem, the edges of the source and semiconductor and the drain and semiconductor, respectively. The constants  $A_1$  and  $A_2$  are to be determined from the boundary conditions along with B.

The constant  $A_1$  can be dispatched immediately. The point  $\lambda_1$  is the source-semiconductor edge. Since the supply of electrons from the source is unlimited, we cannot have a field going to infinity there—integrable or not. Otherwise we should have an infinite current. We must therefore set

$$A_1 = 0. \quad (28)$$

With  $A_1 = 0$ , we will ultimately get  $E_x = 0$  at the source end of the channel, whereas it becomes infinitely large at the drain end. The conductivities at these two places are found to be infinitely large and zero, respectively.

Applying Eq. (23) and (24) in these respective limits to Eq. (27) we find

$$\left(\frac{V_o - V_g}{h}\right)^2 = \frac{-I}{\mu e \pi} \log \frac{\lambda_2}{\lambda_1} - \frac{A_2}{\lambda_2} + B \quad (29)$$

and

$$\left( \frac{V_d + V_o - V_g}{h} \right)^2 = B. \quad (30)$$

One more condition is needed completely to specify the solution. Keeping in mind the  $I$  is regarded as an independent constant just as are  $A_2$  and  $B$ , until they are fitted to the input parameters, we see in Eq. (29) and (30) that we have three constants and two equations. The third condition is rather subtle. Considering the definition of the current  $I$  in Eq. (7) and the boundary conditions Eq. (18) and (20) we see that the boundary conditions are requiring the current in the form of Eq. (7) to vanish on the metal electrodes. The strict boundary condition in the pretransformed problem is Eq. (8),  $E_x = 0$ . But  $I$  can also be zero if  $\left[ E_g + V_o/h \right]$  is zero. We must ensure that we have only  $E_x = 0$  in our solution. This is accomplished by requiring that the real part of  $F$  is always non-negative on the boundary. As Gernst shows, there is a point on the gate or the drain electrode where the modified field vanish i.e.

$$E_x = \left( E_y + \frac{V_o}{h} \right) = 0. \quad (31)$$

The corresponding point,  $\mu_{o2}$ , in the transformed  $\omega$  space must correspond to a minimum in the real part of  $F(\omega)$  and that

$$F(\mu_o) = 0. \quad (32)$$

Differentiating the expression

$$F(\omega) = \frac{-I}{\mu\epsilon\pi} \log \frac{\omega - \lambda_2}{\omega - \lambda_1} + \frac{A_2}{\omega - \lambda_2} + B \quad (33)$$

we get

$$\frac{\mu_o - \lambda_2}{\mu_o - \lambda_1} = \frac{A_2}{\lambda_2 - \lambda_1} \bigg/ \frac{-I}{\mu\epsilon\pi} \quad (34)$$

And using Eq. (32)

$$\frac{-I}{\mu\epsilon\pi} \log \frac{\mu_o - \lambda_2}{\mu_o - \lambda_1} + \frac{A_2}{\mu_o - \lambda_2} + B = 0, \quad (35)$$

which is our third equation for the constants. Now combining Eq. (29), (30), (34) and (35), we finally arrive at a transcendental equation relating the current in the channel to the drain and gate voltages. By defining the dimensionless quantities

$$j = \frac{I}{\frac{\mu\epsilon}{hL} (V_g - V_o)^2} \quad (36)$$

$$\eta = \frac{V_d}{V_g - V_o} - 1. \quad (37)$$

The equation takes the form

$$\log \left\{ \left( 1 - \frac{\lambda_1}{\lambda_2} \right)^{-1} \frac{\pi L}{h} \left[ 1 - \frac{1 - \eta^2}{j} \right] \right\} + 1 - \left( 1 - \frac{\lambda_1}{\lambda_2} \right)^{-1} \frac{\pi L}{h} \left[ 1 - \frac{1 - \eta^2}{j} \right] + \frac{\pi L}{h} \frac{\eta^2}{j} = 0 \quad (38)$$

A most interesting result here is that the ratio  $\frac{L}{h}$  enters as an independent parameter. This may not occur in the case of an aligned gate.

Curves showing the dependence of  $j$  on  $\eta$  are taken from Geurst's paper and are reproduced in Figure 2.6. We can rewrite these relationships to show the dependence of  $I$  on  $(V_g, V_d)$  as

$$I = - \frac{\mu\epsilon}{hL} (V_g - V_o)^2 j \left( \frac{V_d}{V_g - V_o} - 1 \right). \quad (39)$$

Notice that the output impedance is related to the geometric factor  $(h/L)$ .

Comparison of these results with experimental measurements shown in Figure 2.6 shows the correctness of the model. No detailed fitting of this model to our experimental results has been carried out as yet, however, we expect to do it sometime in the future.

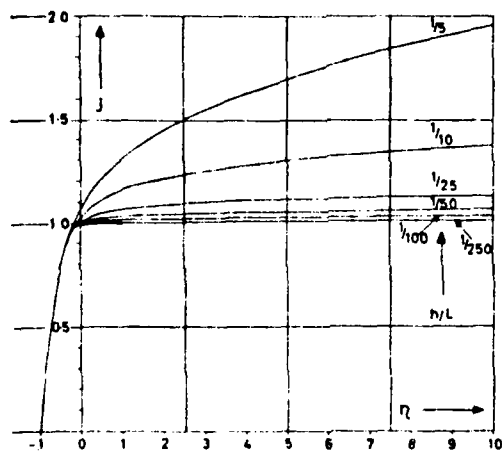


Fig. 2.6 The dimensionless drain current

#### 2.4.2 The Elemental Drive Circuit

There are numerous considerations that bear on the design and operation of the TFT-EL display cell shown schematically in Figure 2.7, and it is the purpose of this section to discuss the more important of them. The cell design necessarily starts with the electro-optical characteristics and electrical drive requirements of the EL phosphor,  $C_{el}$ , which must be controlled by a power transistor,  $T_p$ , of adequate current capacity, voltage rating, and OFF resistance. The storage capacitor,  $C_s$ , which serves to hold the cell brightness level constant between line refresh epochs, must be large enough to prevent significant change in the gate voltage of  $T_p$  between refreshes, yet small enough geometrically to fit within the confines of the display cell. Again, the logic transistor,  $T_l$ , must have high enough forward conductance in the ON state to charge storage capacitor  $C_s$  in a time short compared to the line access time, while at the same time providing sufficiently low leakage in the OFF state to allow the storage capacitor to hold its charge over one frame period. Finally, it is desirable that the control signals on the source and gate buses be at logic levels comparable to those used in ordinary CMOS integrated circuits, which levels are also compatible with thin film transistor drive circuits. In addition to these factors concerning the choice of characteristics of components within the cell, the geometric design and layout of the cell is further restricted by such considerations as stray capacitances between pairs of elements within the cell and between cell nodes and the semi-transparent EL excitation electrode which serves as the front window of the display and which carries a relatively high ac voltage. Voltages and currents induced in the cell and in the display matrix buses have important implications for the operation of the cell and overall display, and consequently affect the design of driving circuits peripheral to the display proper. Parasitic capacitances between the front electrode and cell circuitry which have a direct bearing on the operation of the cell are shown in Figure 2.7 as capacitors C-1 and C-2.



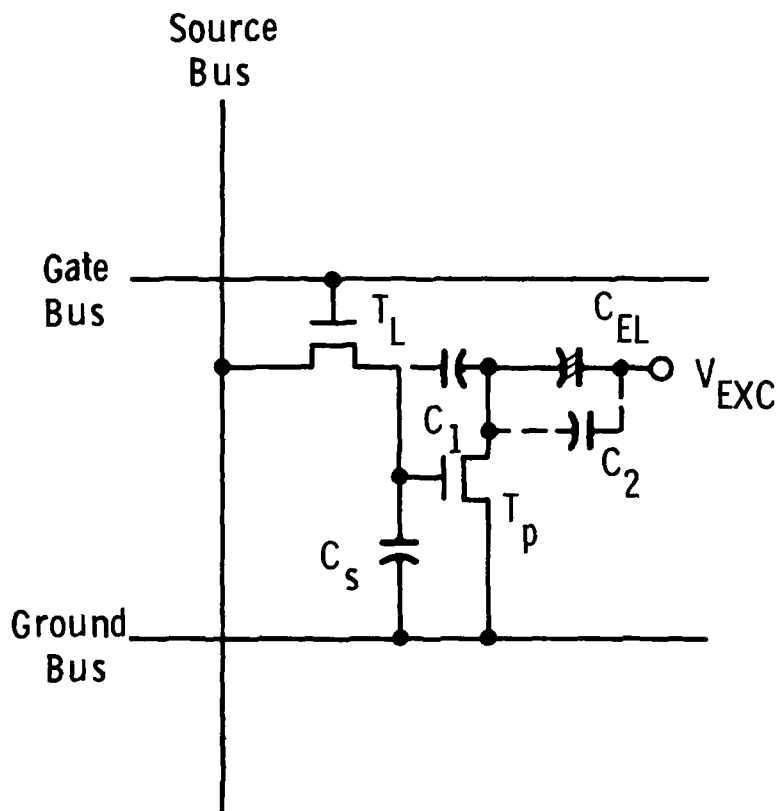


Figure 2.7 Display element schematic with output gate parasitics.

A typical voltage- and current-to-brightness relationship for powder EL phosphor as used in the display cell is shown in Figure 2.8. In this case a useful brightness level of 15 fL is achieved at 60 V<sub>rms</sub> and 30 μA<sub>rms</sub>, corresponding to 84 V<sub>pk</sub> and 42 μA<sub>pk</sub>. In the same figure it will be noted that at a voltage level of 20 V<sub>rms</sub> and 10 μA<sub>rms</sub> the brightness is down by a factor of 100 to 0.15 fL. Characteristics of the power transistor, T<sub>p</sub>, must be consistent with these load parameters. Logic and power transistor characteristics shown in Figure 2.8(a) and 2.8(b) are typical for transistors that have been designed into the present panels. Referring to (b) and assuming that a forward voltage drop of 2V is permissible in series with the EL element, it is apparent that a forward bias of +8V on the gate of T<sub>p</sub> will handle the 43 μA peak current of the phosphor element, and that at a gate voltage of 0V appreciably less than 10 μA will flow, satisfying the OFF condition for the phosphor. Although this figure shows only the characteristics for drain-to-source voltages of up to 15V, other measurements of these characteristics show the zero bias or OFF state to continue at very low current levels out to several hundred volts. Thus it will be seen that a control voltage swing for the gate of T<sub>p</sub> of 0 to +8V should be adequate, neglecting changes in that voltage which might occur during a frame time.

Choice of the capacitance C<sub>s</sub> starts with a knowledge of a realistic leakage current or OFF current characteristic for the logic transistor T<sub>l</sub>, which governs the loss of charge on C<sub>s</sub> during the time between successive refreshes or line-at-a-time addressing of a particular line in the array. The characteristics as shown in (a) do not adequately show the zero gate bias current or OFF current for this transistor. However, measurements of many logic transistors show that an OFF current of 1 nA (10<sup>-9</sup>A) is not difficult to obtain. Assuming a frame time of 0.017 seconds and an allowable voltage drift across C<sub>s</sub> of 1V, the necessary value of C<sub>s</sub> is given as

$$C_s = 10^{-9} \text{A} \times 0.017 \text{s} / 1 \text{V} = 17 \text{ pF}.$$

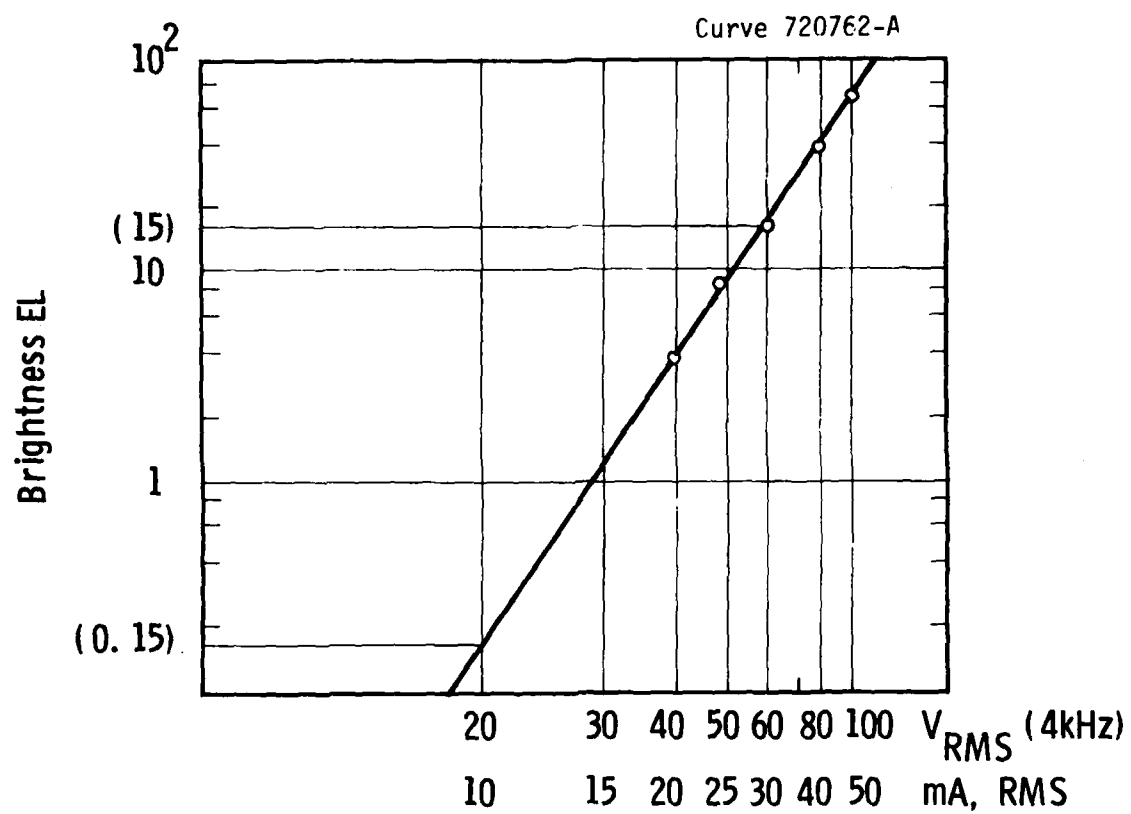


Fig. 2.8 Brightness, voltage and characteristics of the powder EL phosphor.

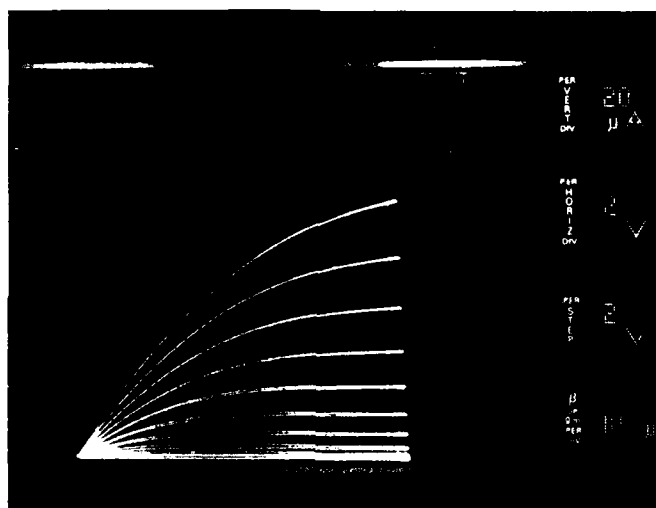
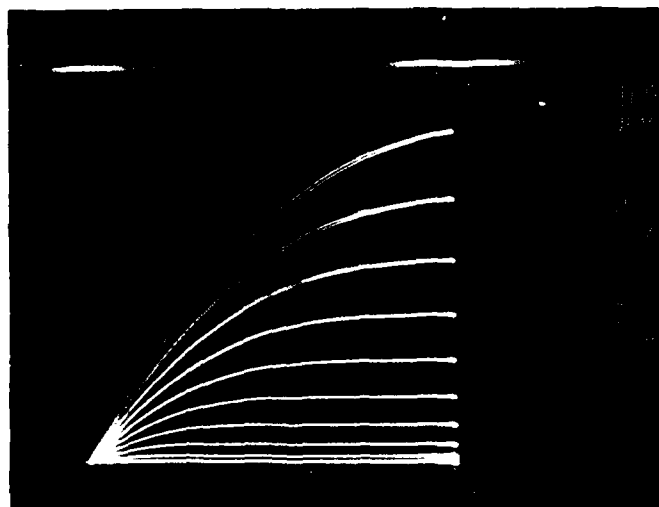


Figure 2.8(a) Characteristics of a typical logic transistor ( $T_L$ ).



100 mA/Ver. Dir.

2V/Hor. Dir.

2V/Step

Figure 2.8(b) Characteristics of a typical power transistor ( $T_p$ ).

Table 2.2 shows the capacitances of the different cell elements and parasitics as labeled in Figure 2.7, as realized in the final cell design. The storage capacitor  $C_s$  with a capacitance of 15 pF would allow slightly more than 1V drop in 0.017s at a  $T_\ell$  OFF current of  $10^{-9}$ A, but this is easily allowed for by slightly increasing the span of the impressed control voltage. In a fully populated DMD display, the 77 rows of the display would allow a maximum of 0.22 mS for access to each line, assuming a 60 Hz refresh rate. The ON resistance of  $T_\ell$  must be such that the storage capacitor is charged in a time short compared to 0.2 mS. Assuming that a 0.02 mS time constant would satisfy this requirement, the ON resistance for  $T_\ell$  is given by

$$R_{on,T_\ell} = 2 \times 10^{-5} \text{ s} / 1.5 \times 10^{-11} \text{ F} = 1.3 \times 10^{-6} \Omega ,$$

corresponding to a forward current of 0.8  $\mu$ A at a drain-source voltage of 1V. This ON resistance is easily achieved by the transistor characteristics shown in (a) for a gate voltage of +2V or greater. It is easy to see that the logic transistor with the characteristics shown could easily write the video information into the storage capacitor  $C_s$  ten times faster than this, useful in writing a line during the flyback period of conventional TV signals, by using a gate voltage of +4V to +6V. This is important in the design of larger displays for use with standard TV signals.

The 1 nA OFF current assumed as an upper limit for  $T_\ell$  in some cases has been shown to be conservative by two to three orders of magnitude; if this were the only consideration in choosing the size of  $C_s$ , a substantially smaller value would be permissible in those situations. A further consideration, however, is the size of the induced signal due to the parasitic capacitances  $C_1$  and  $C_2$  coupled from the excitation voltage appearing on the front electrode of the display. Table 2.2 gives representative values for those capacitances, which depend on the area of the electrodes, the thickness and nature of the dielectric layer, and the number of capacitor plates. In the present

design,  $C_s$  uses three plates, the outer two being at ground and the central one being the storage node. When the cell is lit,  $T_p$  is ON, and because of its high conductance the ac voltage on its drain is very small and the voltage coupled between drain and gate through parasitic capacitance  $C_1$  is negligible. In this case, the voltage couple from the excitation source through parasitic capacitance  $C_2$  governs, and is given by

$$\begin{aligned} (V_{C_s})_{ac} &= V_{exc} \times C_2 / (C_s + C_2) \approx V_{exc} \times C_2 / C_s = 60 \times .023 / 15 = 1.5 \times 10^{-3} \\ &\approx 0.1V \end{aligned}$$

which is negligible compared to the control voltage range impressed on  $C_s$ . When the element is OFF, the full ac excitation voltage appears both at the front electrode and at the drain of  $T_p$ , and so the induced voltage is then given by

$$\begin{aligned} (V_{C_s})_{ac} &= V_{exc} (C_1 + C_2) / (C_s + C_1 + C_2) \approx V_{exc} (C_1 + C_2) / C_s \\ &\approx 60V \times 0.17 / 15 \\ &\approx 60V \times 1.1 \times 10^{-2} \\ &\approx 0.7V. \end{aligned}$$

Again, this voltage is not appreciable compared to the range of voltage needed to control the output device. However, if  $C_s$  were a factor of ten or more smaller, which seems permissible if a lower leakage logic transistor  $T_\ell$  were employed, these induced voltages on the gate of the power transistor could be comparable to or surpass the range of the control voltage needed on that gate and would appreciably influence the design of the logic and addressing circuitry.

All of the foregoing discussion leaves out the question of drifts of transistor thresholds, which would add to the range of control voltage needed to maintain ON or OFF control of the display elements in the presence of such drifts. It is felt that transistors with drifts

sufficiently small that this factor can be disregarded are achievable, and in addition, electronic means for accommodating a small range of transistor threshold drift seems possible, as will be described in Section 9.5.

It should be noted that because of the very high ON/OFF conductance ratios provided by the TFT s, the current carrying capability and useful transconductance can be varied over a rather large range by varying channel length and width dimensions; in particular, the power transistor could be made to turn ON and OFF with a smaller gate voltage swing by use of a wider channel, permitting use of peripheral circuitry at lower logic levels.



TABLE 2.2  
Display Element Capacitances

Capacitor	Area $10^3 \mu^2$	Capacitance (pF)
$C_s$ (storage)	124	$15^1$
$C_1$ (gate-drain, $T_p$ )	1.25	$0.15^1$
$C_2$ ( $V_{exc}$ to gate, $T_p$ )	32	$0.023^2$
$C_{el}$ (EL element)	500	$5.0^3$ ( $10.0^4$ )

<sup>1</sup>Dielectric is  $5000\text{\AA}$ ,  $\text{Al}_2\text{O}_3$  ( $K \approx 8$ ,  $C \approx 0.12 \text{ pF}/10^3 \mu^2$ )

<sup>2</sup>Dielectric is  $37\mu$  Riston ( $K \approx 3$ ,  $C \approx 7 \times 10^{-4} \text{ pF}/10^3 \mu^2$ )

<sup>3</sup>Dielectric is sprayed EL phosphor ( $C \approx 1.0 \times 10^{-2} \text{ pF}/10^3 \mu^2$ )

<sup>4</sup>Dielectric is brushed EL phosphor ( $C \approx 2.0 \times 10^{-2} \text{ pF}/10^3 \mu^2$ )

### 2.4.3 The Busbar Complex

In the TFT-EL display matrix, three sets of busbars are needed to service the array of display cells, namely, the source busses, the gate busses and the ground busses. In addition, a semi-transparent continuous metal film outer electrode is used to supply EL excitation power. Since the display is organized for line- or row-at-a-time addressing, the binary video information for each row of cells must be supplied by a set of vertical busses, referred to as source busses, which connect to the source electrodes of the logic transistors  $T_\ell$  (see Figure 2.7). The gate electrodes of the logic transistors  $T_\ell$  for the row being addressed are connected to a horizontal gate bus which is pulsed positively in sequence with the other gate busses to connect the storage capacitors in that row to their respective source busses via the switch or logic transistors,  $T_\ell$ . The ground return for the drain electrodes of the power transistors  $T_p$  and for the ground electrode of the storage capacitors  $C_s$  is furnished by a set of parallel ground busses which may be oriented either vertically or horizontally; both orientations have been employed in this program, as shown in Figures 2.9 and 2.10. A ground plane which would also provide electrostatic shielding between circuit nodes and the high voltage ac excitation could also be used for this function, and has been included in several conceptual circuit designs and layouts.

In all addressable flat panel displays the busbar systems including crossover insulation are a major consideration in the display design, and must satisfy various criteria including minimal area, environmental ruggedness, adequate current and voltage capacity, low resistance, and low visual interference with the output medium. Frequently, semi-transparent conductors are employed to satisfy the latter, and in the present case of the TFT-EL display, a front or "window" electrode in the form of a semi-transparent gold film is applied over the EL phosphor and is used to carry the ac excitation power.

The capacitances of the busses to each other and to circuit elements have functional importance in the circuit operation, especially

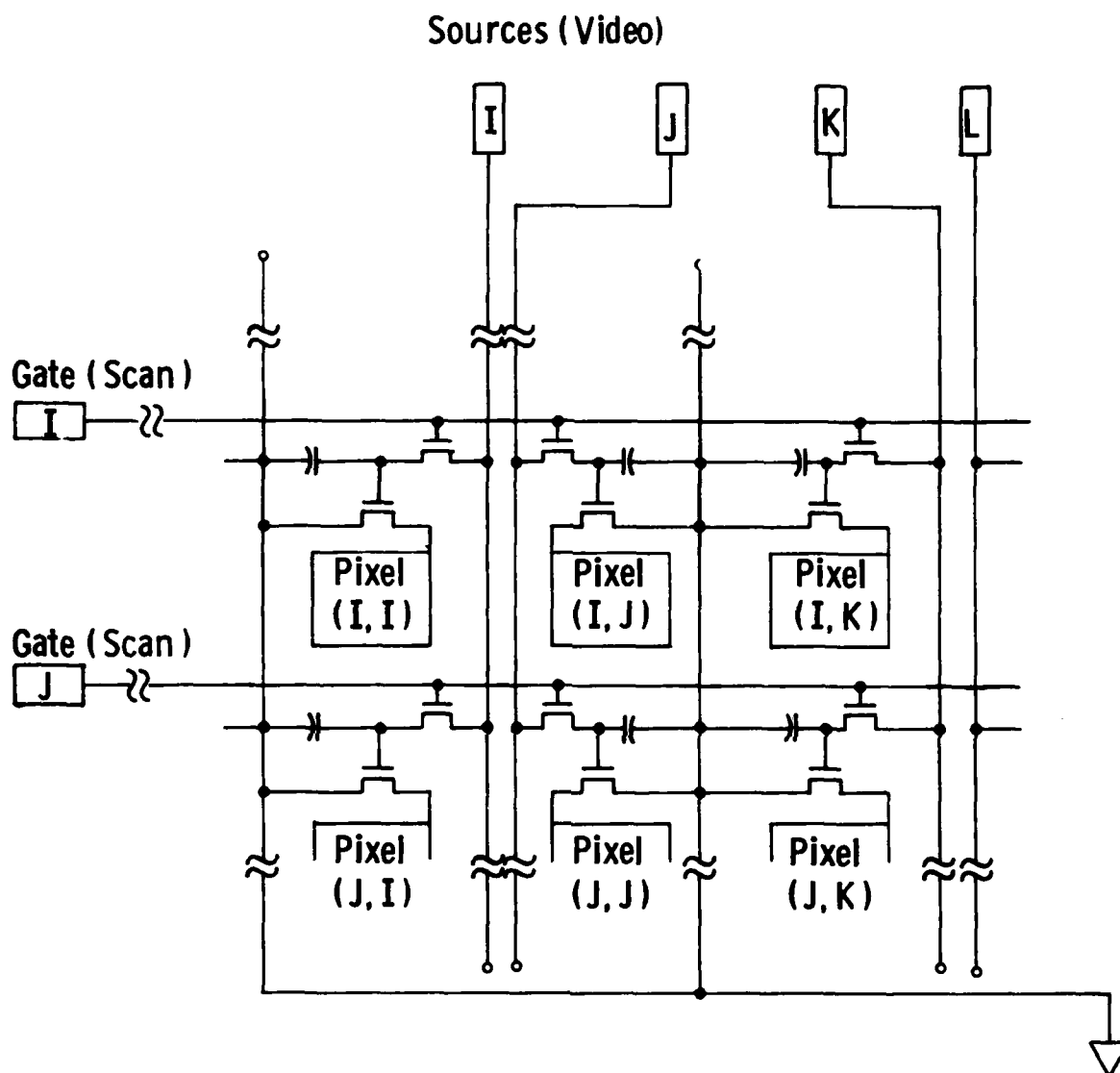


Figure 2.9 Bus-bar configuration for old layout.

Dwg. 7699A01

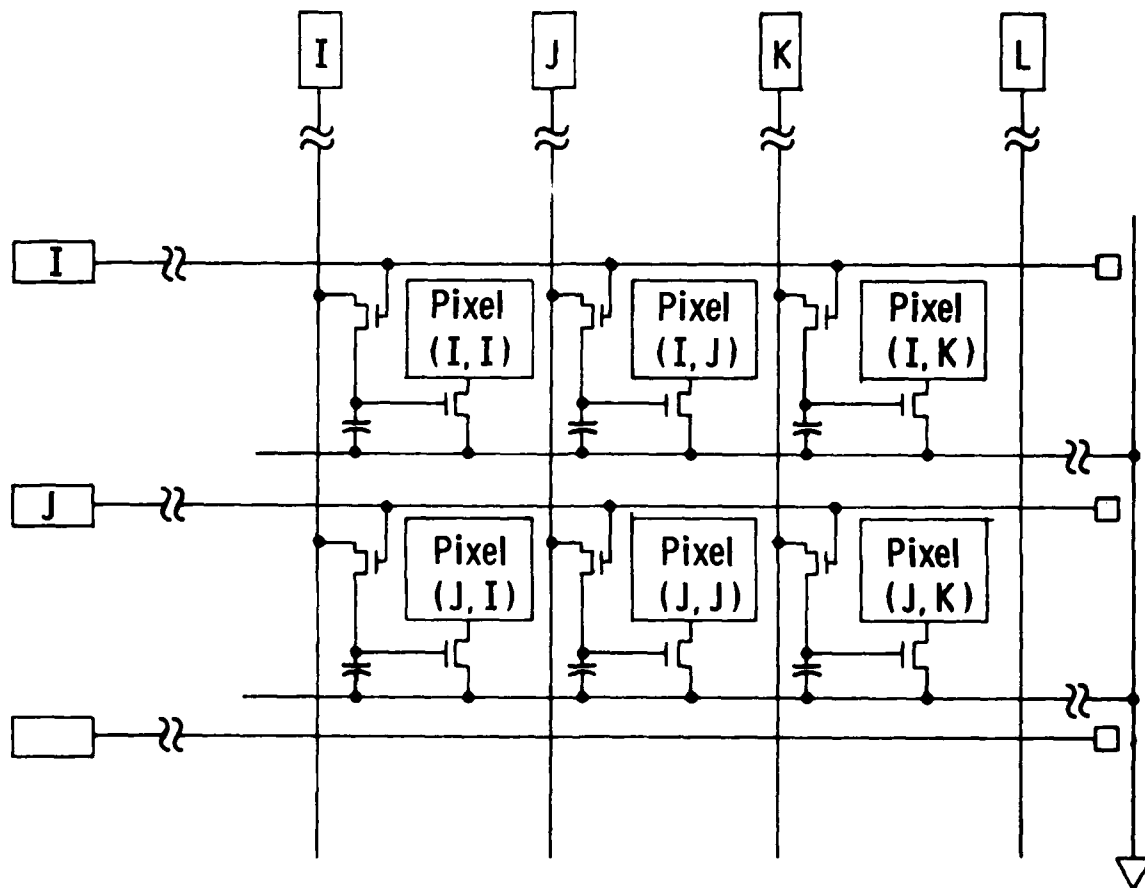


Figure 2.10 Bus-bar configuration for new layout.  
(See also Figure 7.1)

with respect to the peripheral drive circuitry, and must be considered during the analysis of circuit operation. In the TFT-EL display, the busses and insulators are all thin films, and capacitive effects dominate with respect both to current loads and induced voltages. It follows that voltage rates of rise, peak-to-peak excursions, and repetition rates or operating frequencies determine the magnitudes of both load and induced currents. In view of the small cross-section areas of these thin film conductors, bus resistance can become a problem, particularly in connection with EL excitation currents. The possibility of long-term conductor deterioration from ion migration due to excessive current densities, a problem often faced in conventional IC design, does not appear in the present TFT-EL panels, since calculated peak densities of  $3 \times 10^5 \text{ A/cm}^2$  are far below the  $10^7 \text{ A/cm}^2$  degradation threshold.

In evaluating the electrical performance of the bus system and in modifying the design to achieve satisfactory operation, a practical and altogether suitable approach is to assess the magnitude of currents, voltages and dissipations in a given or initial design, and then make suitable changes in bus geometry and/or composition necessary. Worst case conditions, such as all elements OFF or ON, or lines of elements switching alternatively ON and OFF, are used to evaluate performance at operational extrema. This approach has been used in the present program, and the resulting bus system characteristics and performance are described in Figures 2.11 and 2.12 along with the following four tables. The major inter-bus and bus-to-circuit capacitances are indicated in Figure 2.11 while Fig. 2.12 indicates the overall bus layout and bus lengths. Table 2.3 lists resistive features of the busses and Table 2.4 the capacitive characteristics.

In Table 2.5 is presented the resulting electrical performance of this bus complex in terms of operating voltages and currents, IR voltage drops, and  $I^2R$  power dissipation in the busses. Bus resistances measured on two substrates are roughly twice calculated values, due principally to the fact that metallic films deposited in

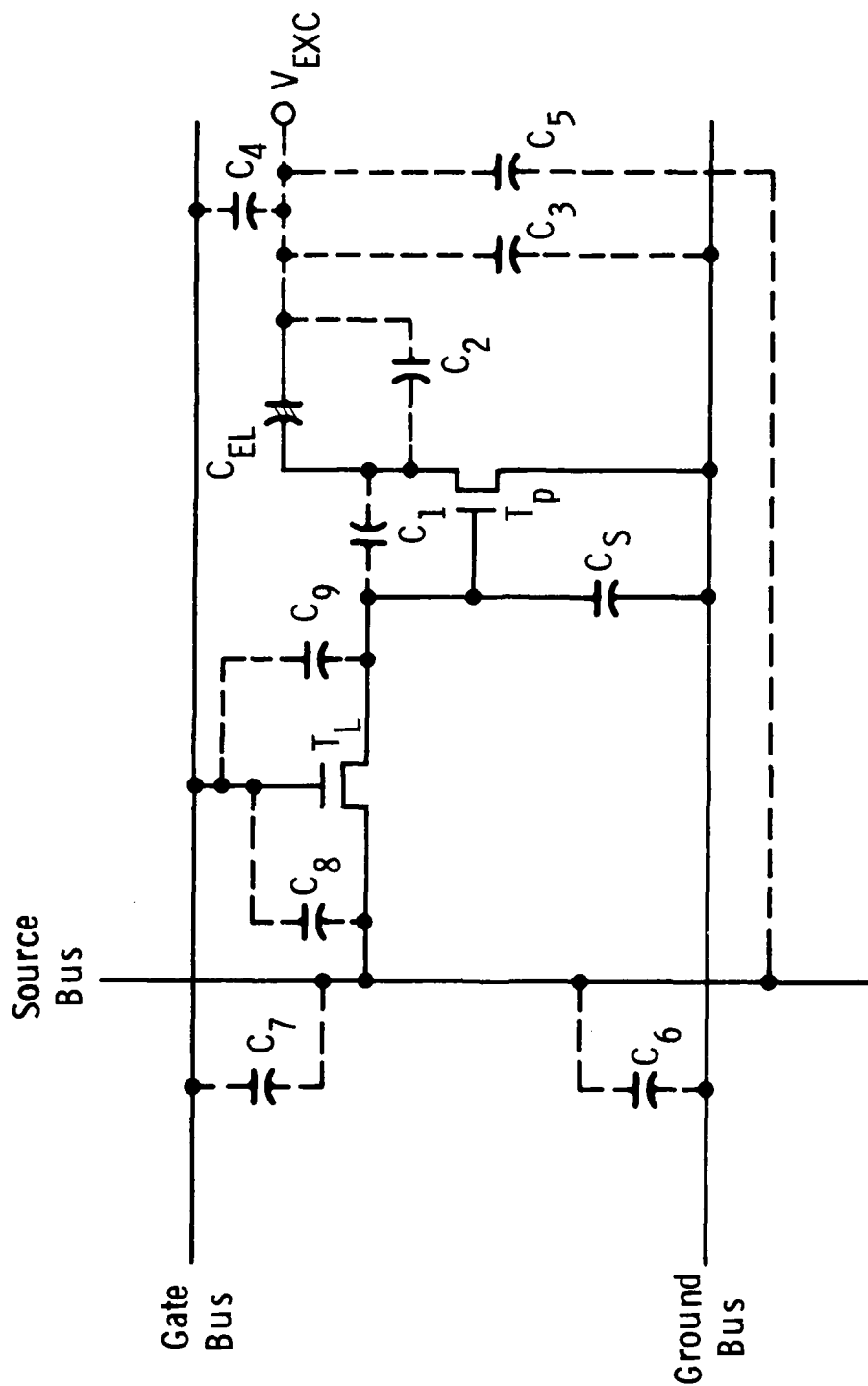


Figure 2.11 Major inter-bus and bus-to-circuit capacitances.

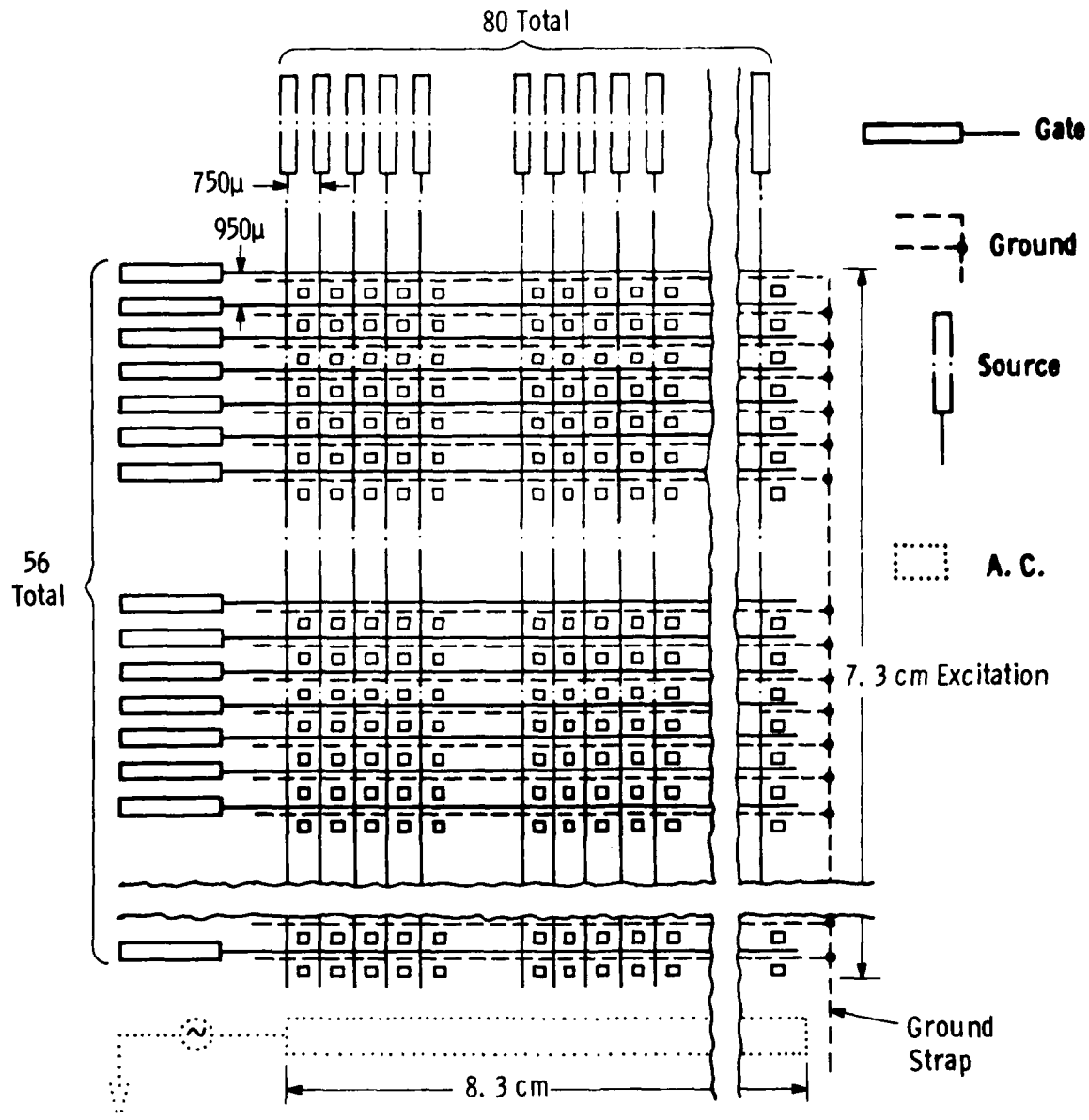


Figure 2.12 Bus bar complex half DMD - New design.

400Å layers are apt to show higher than bulk resistivity used to obtain the calculated value. Likewise, the thin gold semi-transparent excitation electrode has a two to three times higher resistance per square than calculated from its thickness and the bulk resistivity of gold.

Capacitive loading on the various busses is distributed on a cell-by-cell basis, as Table 2.4 indicates, except for the bus-to-excitation electrode capacitance which completes the loading. Thus, the total capacitive load for the source bus, shown in 41 pF in Table 2.4.3-3, is comprised of the bus totals for  $C_5$ ,  $C_6$ ,  $C_7$ ,  $C_8$  given in Table 2.4.3-2 and is similarly for the gate and ground busses. The planar EL excitation electrode (last line of table), extending over the entire active area of the substrate, realizes its maximum capacitance load when all elements are ON, at which time the load consists of all the EL capacitive elements in parallel. In Table 2.5 the operating conditions assumed are typical of those used in the viewability exerciser. Voltage drops, as well as dissipated power due to load currents are quite low, except for the ground strap, which would consume about 0.45W for the case of all elements lit, using a brushed phosphor. In this case, the accompanying voltage drop of over 5V could cause a variation in cell brightness in the vertical direction. For the usual case of 35% of the elements lit as in an alphanumeric display, this loss would be reduced 8-fold to 56 mW in the ground strip bus. The total losses of all other busses in the bus complex would then be only 14 mW. Use of a thicker metal layer for the ground strap could reduce its losses to a negligible value.

The interaction of the busses due to their inter-capacitances can give rise to rather large spurious voltages, if the impedance of the driving or controlling circuitry is not sufficiently low. Table 2.6 shows the currents or voltages that are induced to the source and gate voltages if an infinite or zero, respectively, driver impedance is assumed. These induced voltages arise from capacitive division, the equivalent circuit being shown in Figure 2.13(a). Worst cases are represented by lines 2,3,5 and 6 in the table, where voltages of 10V and up would be induced into the busses if left floating ( $Z_{DR} = \infty$ ).



Dwa. 7710A55

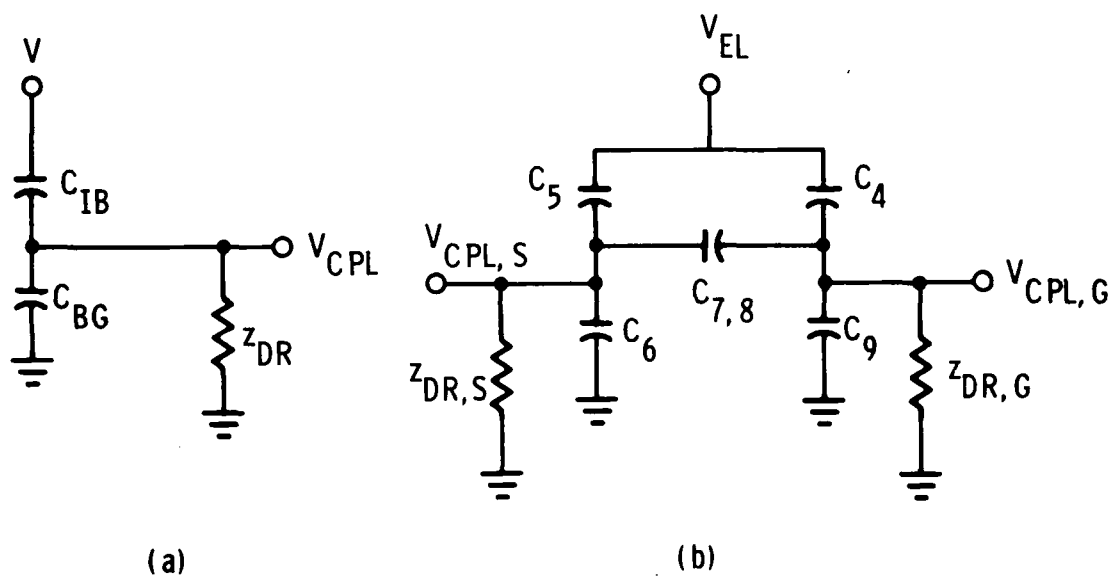


Figure 2.13 Equivalent circuits for interbus coupling.

The last column shows the maximum output impedance of the driver circuit required to keep induced voltages below 1V. Where high impedance CMOS or TFT scanning circuits are used, these impedances may not be easily achieved. However, these worst case situations can be avoided by appropriate control strategy, as is discussed below in Section 9.5. For instance, if the horizontal scanner loads the video signal onto the source busses sequentially rather than in tandem, line 4 of Table 2.6 would represent this case instead of line 5, and the voltage induced on a gate bus with high impedance driver would be only 0.2V instead of 17V. The case represented by line 2 of Table 2.6 namely all gate busses pulsed positively in parallel, is encountered in operation of the ON-OFF exerciser described in Section 9.4, and provides design criteria for that exerciser. It does not occur, however, in normal operation of the display.

An extreme situation arises if gate and source busses are all floating or have very high impedance drivers. The situation is as shown in Figure 2.13(b), where the capacitor labels refer to those of Figure 2.11 and Table 2.6, and where the values assumed are those for the array as a whole (last column in the table). The EL excitation voltage  $V_{el}$  couples to both gate and source busses with driver impedances  $Z_{DR,G}$  and  $Z_{DR,S}$  which are high compared to the 5 kHz reactance of any of the capacitances, i.e., much larger than 100 K $\Omega$  per bus, or 2 K $\Omega$  per array. As a result, neither drive set serves to hold down the voltage induced, and so the relatively large interbus capacitances  $C_7$  and  $C_8$ , which would normally help attenuate this signal, are ineffective. The induced voltages are given by

$$V_{cpl,s} = V_{el} \frac{C_5 C_9 + C_4 C_5 + C_4 C_d}{(C_4 + C_9)(C_5 + C_6 + C_d)},$$

where

$$C_d = \frac{(C_7 + C_8)(C_4 + C_9)}{C_7 + C_8 + C_4 + C_9},$$

and, similarly,

$$C_{cp, g} = V_e \frac{C_4 C_6 + C_4 C_5 + C_5 C_e}{(C_5 + C_6)(C_4 + C_9 + C_e)}$$

where

$$C_e = \frac{(C_5 + C_6)(C_7 + C_8)}{C_5 + C_6 + C_7 + C_8}.$$

Inserting values from Table 2.4 and assuming:  $V_{el} = 168 V_{p-p}$  gives  $V_{cpl, s} = 0.212e_l = 36V$ , and  $V_{cpl, g} = 0.251e_l = 43V$ , both of which are unacceptable for panel operation. Accordingly, it is essential that suitably low impedance, i.e., 100 K $\Omega$  or less, drivers be provided for these busses. Further discussion of control circuits which take these factors into account is given in Section 9.

TABLE 2.3  
Busbar Resistances

Bus	Symbol	Resistance	
		Calculated	Measured <sup>3</sup>
Source <sup>2</sup>	$R_{SB}$	1.1 K $\Omega$	2.2 K $\Omega$
Gate <sup>2</sup>	$R_{GT}$	1.3 K $\Omega$	2.5 K $\Omega$
Ground <sup>2</sup>	$R_{GN}$	1.3 K $\Omega$	2.2 K $\Omega$
EL Excitation <sup>3</sup> Electrode	$R_{D,EX}$	—	20 $\Omega/\square$

<sup>1</sup> Average of substrates 9156-3,6

<sup>2</sup> Ni, 800Å thick, 50 $\mu$  wide

<sup>3</sup> Au, 20Å thick

TABLE 2.4

Busbar Capacitances,  $\frac{1}{2}$  DMD, New Design

Designation	Bus or Element to	Capacitances, pF (Calculated)			
		Per Cell Occupied <sup>1</sup>	Vacant <sup>1</sup>	Per Bus Horiz. Vert.	Per Array
C <sub>1</sub>	T <sub>p</sub> Drain T <sub>p</sub> Gate	0.15	0	12	8.4
C <sub>2</sub>	Exc. T <sub>p</sub> Gate	0.024	0	—	—
C <sub>3</sub>	Exc. Ground	0.068	0.026	6.5 <sup>2</sup>	—
C <sub>4</sub>	Exc. Gate	0.030	0.024	3.4 <sup>2</sup>	—
C <sub>5</sub>	Exc. Source	0.045	0.034	—	3.3 <sup>2</sup>
C <sub>6</sub>	Source Ground	0.30	0	24	17
C <sub>7</sub>	Source Gate	0.30	0	24	17
C <sub>8</sub>	T <sub>l</sub> Source T <sub>l</sub> Gate	0.06	0	4.8	—
C <sub>9</sub>	T <sub>l</sub> Drain T <sub>l</sub> Gate	0.06	0	4.8	—
C <sub>el</sub>	Exc. T <sub>p</sub> Drain	5.0 <sup>3</sup>	0	400	280
—	Exc. All(T <sub>p</sub> OFF)	10.0 <sup>4</sup>	0	800	560

<sup>1</sup>Total No. Occupied = 4480; Total No. Vacant = 4091<sup>2</sup>Includes test pads @ 0.016 pF<sup>3</sup>Powder phosphor, sprayed<sup>4</sup>Powder phosphor, brushed

TABLE 2.5  
Electrical Performance of Busbar System ( $\frac{1}{2}$  DMD, New Design)

Bus	Capacitive Load, pF	Resistance R( $\Omega$ )	Operating Voltage, V Neg. Pos.	Transition Time, $T_t$ ( $\mu$ S)	Charging Current, $I_{ch}$ (mA)	Repetition Frequency, $f_r$ (Hz)	Voltage Drop, $\Delta V$ (V)	Dissipation <sup>2</sup> per Bus Array (mW)
Source	41	1100	-10 +10	1.0	0.8	5 kHz	0.5	0.002 0.1
Gate	34	1300	-20 +10	50	0.2	60 Hz	0.1	0.0003 0.02
Ground	417 <sup>3</sup> 817 <sup>4</sup>	1300 1300	-84 +84 -84 +84	100 100	1.11 2.19	5 kHz 5 kHz	0.7 1.4	0.80 45 <sup>5</sup> 1.03 58 <sup>5</sup>
Ground Strap	—	90	— —	—	62 <sup>3</sup>	—	2.8	— 58 <sup>5</sup>
	—	90	— —	—	122 <sup>4</sup>	—	5.5	— 447 <sup>5</sup>
Excitation	23,300 <sup>3</sup> (Total)	17.6	-84 +84	160	62 (Total)	5 kHz	0.5	— 11 <sup>5</sup>
Electrode	45,700 <sup>4</sup> (Total)	17.6	-84 +84	160	122 (Total)	5 kHz	1.1	— 43 <sup>5</sup>

$$^1 \Delta V_{max} = RI_{max}/2$$

$$^2 P = RI_{rms}^2/3 = 2RI_{ch}^2 T_{tr}/3$$

<sup>3</sup> Sprayed phosphor,  $T_{tr}$  ON

<sup>4</sup> Brushed phosphor,  $T_{tr}$  ON

<sup>5</sup> 5 kHz sine wave,  $\frac{1}{2}$  period

<sup>6</sup> All elements ON, with 35% lit (average for a display)

TABLE 2.6  
Effects of Bus-to-Bus Coupling  
( $\frac{1}{2}$  DMD, New Design)

	Affected Bus	Disturbing Bus	Inter-Bus Capacitance $C_{CB}$ (pF)	Effective Bus to Ground Capacitance $C_{BG}$ (pF)	Voltage Swing (V)	Transition Time $T_t$ ( $\mu$ S)	$V_{cpl}$ Peak (V) $Z_{dr} = \infty$	$I_{cpl}$ Peak ( $\mu$ A) $Z_{dr} = 0$	$Z_{dr}$ (K $\Omega$ ) for $V_{cpl} < 1V$
1.	Source	Gate (1)	0.36	41	30	5	0.3	1.8	$\infty$
2.	Source	Gate (56)	20	20	30	5	10	120	8.3
3.	Source	Exc.	3.3	37	168	100 (5 kHz)	14	8.6	125
4.	Gate	Source (1)	0.36	33	20	1	0.2	7.2	$\infty$
5.	Gate	Source (80)	27.4	4.8	20	1	17	550	1.8
6.	Gate	Exc.	3.4	23.8	168	100 (5 kHz)	21	9.0	111

#### 2.4.4 The Phosphor System

The phosphor system means the components of the electro-luminescent structure which are applied over the thin film circuit matrix providing preliminary viewability testing of the composite structure prior to final encapsulation. The theory and structure of operation of the phosphor system is described in detail later in Section 7, and its cross section is illustrated in Figure 2.4.4.1 for the purpose of identifying the principal components. Basically, these form a "sandwich."

—— conductor  
—— dielectric  
—— powder phosphor  
—— dielectric  
—— conductor

The phosphor emits light in response to an electric field applied across the two conductors. In this case, the conductor, "the top electrode", is common to all pixels while control of each light emitting element is exercised through the EL contact parts of respective circuit elements. The field is designed to locating a phosphor excitation to the EL panel area and to prevent unwanted optical emission due to fields impressed on the phosphor between the top electrode and various circuit breakers, for example. This configuration permits non-selective application of the powder phosphor material, a distinct advantage from the manufacturing viewpoint. Design requirements of the respective components of the system are the following:

- (1) Top Electrode. The chief requirements of this component concern adequate conductivity for the phosphor excitation current and together with adequate transparency, since the display is viewed through it. Prior experience has indicated that an evaporated gold layer enabled this task.



- (2) Dielectric Layers. These need to be electrically insulating with high dielectric constant, transparent, and thick enough to sustain voltages applied to generate the phosphor excitation field.
- (3) Phosphor Layer. Apart from the intrinsic efficiency of optical emission discussed in Section 7, this layer must be applied uniformly so that all pixel layers exhibit equal brightness within limits invaluable by the observer.

The method of application of the phosphor layer system is described subsequently in Section 3.3 and the history of its development during the period of the contract in Section 7.

## 2.5 Performance Specifications

This section outlines the display performance specifications based on the technical requirements in SCS-501 dated May 2, 1975. Also included are the specifications tentatively established for the TFT's in each elemental cell of a DMD display.

### Summary of SCS-501

Under the terms of this contract, thin film displays must meet the following quality and environmental tests:

- (1) Assemble and package 2 half-panels to produce a 256 character display approximately 3.5 x 7.5 x 0.2 inches. Maximum weight 5 oz.
- (2) The display characters shall be visible and recognizable in an ambient of 2000 foot candle (fc). The contrast ratio at 50 fc should be greater than 20.
- (3) Power dissipation shall not exceed 2 watts with all elements on and 1 watt with all elements off.
- (4) Operating temperature range shall be -45 to 72°C without degradation. The displays must be operated at these temperature extremes and not exceed the power dissipation limits.
- (5) Humidity - Displays shall be maintained at 40°C and a relative humidity of 90-95% for 96 hours and not exceed the power dissipation limits after exposure.
- (6) Altitude - The displays shall operate (not exceed power dissipation limits) at a pressure equivalent to 30,000 and 50,000 feet.
- (7) Shock/Vibration - No visible damage following test method 516.2, Procedure XI of Mil-Std-810B.
- (8) Steady State Life - Displays shall operate at 72°C for 600 hours. Power dissipation should be measured each day and after 600 hours the display must pass the Viewability Test.

(9) Viewability Test

(a) Recognition in an ambient light of 2000 fc. All 256 characters shall be checked for at least 2 of the complete set of ASCII characters. Recognition shall be measured by presenting the characters on the display to 6 objective subjects. A minimum error rate of 3% is acceptable.

(b) One of the 256 character positions shall be checked for all ASCII characters.

(c) At 50 fc the contrast ratio shall be measured at 9 positions.

(d) The displays must pass the viewability test after the operating temperature, humidity and altitude tests as well as steady state life.

The contract requires the delivery of two confirmatory samples tested as follows:

2 displays (2 half-panels, 256 characters)

- visual and mechanical
- viewability
- power dissipation
- 600 hour life test

1 display (2 half-panels, 256 characters)

- operating temperature
- humidity
- altitude
- shock/vibration

TFT Specifications (DMD)

Experimentally it has been established that if the elemental TFT's meet or exceed these specifications on a sampling basis (10 TFT's per half-panel) packaged displays should perform satisfactorily.

Perform tests on a Tektronix 576 curve tracer (or equivalent) in order listed.

### Power Transistor

- (1) Source-Drain leakage current @  $V_g = 0$ ,  $V_d = 15$  volts  
Objective: 50 nanoamperes  
Maximum: 1000 nanoamperes
- (2) Off Ratio (Figure of Merit) - ratio of source-drain leakage current (@  $V_g = 0$ ) before and after application of negative gate bias  
Step 1 - record leakage @  $V_g = 0$ ,  $V_d = 15$  volts  
Step 2 - apply  $V_g = -10$  volts for 10 seconds  
Step 3 - switch to  $V_g = 0$  and record source-drain current after 10 seconds  
Objective ratio: 1.0  
Maximum ratio: 10.0
- (3) ON Current @  $V_g = 20$  volts,  $V_d = 15$  volts  
Minimum ( $I_d$ ) = 50  $\mu$ a
- (4) ON Ratio (Figure of Merit) - ratio of initial source-drain current to source-drain current after 10 seconds with constant positive gate bias (following application of a negative gate bias)  
Step 1 - apply  $V_g = -20$  volts,  $V_d = 15$  volts for 10 seconds  
Step 2 - apply  $V_g = +20$  volts,  $V_d = 15$  volts  
read initial current and current after 10 seconds  
Objective ratio: 1.0  
Maximum ratio: 1.5
- (5) Drain voltage standoff @  $V_g = 2$  volts/step, 5 steps, approximately 1.5 megohm series resistance  
Pass/Fail - TFT should withstand  $V_d = 300$  volts for at least 1 (one) minute without "collapse", runaway or breakdown

### Logic Transistor

- (1) Source-Drain leakage current @  $V_g = 0$ ,  $V_d = 15$  volts  
Maximum: 1 nanoampere

(2) Off Ratio (Figure of Merit)

Same procedure used for power TFT

Objective ratio: 1.0

Maximum ratio: 2.5

(3) ON current @  $V_g = 20$  volts,  $V_d = 15$  volts

Minimum ( $I_d$ ) =  $10 \mu a$

### 3. MANUFACTURING APPROACH

#### 3.1 Manufacturing Process Overview

As in the case of typical solid state device pilot production, tasks associated with fabrication of the display can be segregated into two broad classes:

Class I: Those which are now recurring

Class II: Those which are repeated each time a batch of displays is manufactured

The tasks in each class are identified in flow chart fashion in Figures 3.1 and 3.2 to indicate sequence. The figures also indicate where more detailed description of each task may be found elsewhere in this report.

The implied sequence of tasks in Figure 3.1 is characterized by relatively strong and weak dependences portrayed by the solid and broken arrows respectively. For example, the key pivotal task of component design has a major bearing on the artwork and test instrumentation design. It affects the phosphor technology, the drive electronics and to a lesser extent the vacuum system design and construction. On the other hand, we see weak reverse dependences of component design on artwork. Certain display geometries, for example, are constrained by the features of available computer driven graphics systems. Likewise, certain structural features are incorporated into device design simply for the purposes of test and evaluation.

In Figure 3.1, "circuit fabrication and process verification" means confirming that the electronic integrity of the layout generated on the one hand by the stencil mask hardware and on the other by the vacuum system run recipe. Complete "Pilot System Verification" is not achieved, however, until phosphor application methodology has been developed and minimally adequate test gear constructed. Finally, only after a prototype drive electronics package has been designed and constructed do we have verification of the display manufacturing system.

Various tasks and process steps undertaken during routine fabrication are shown in Figure 3.2. With reference to Figure 3.2, broken

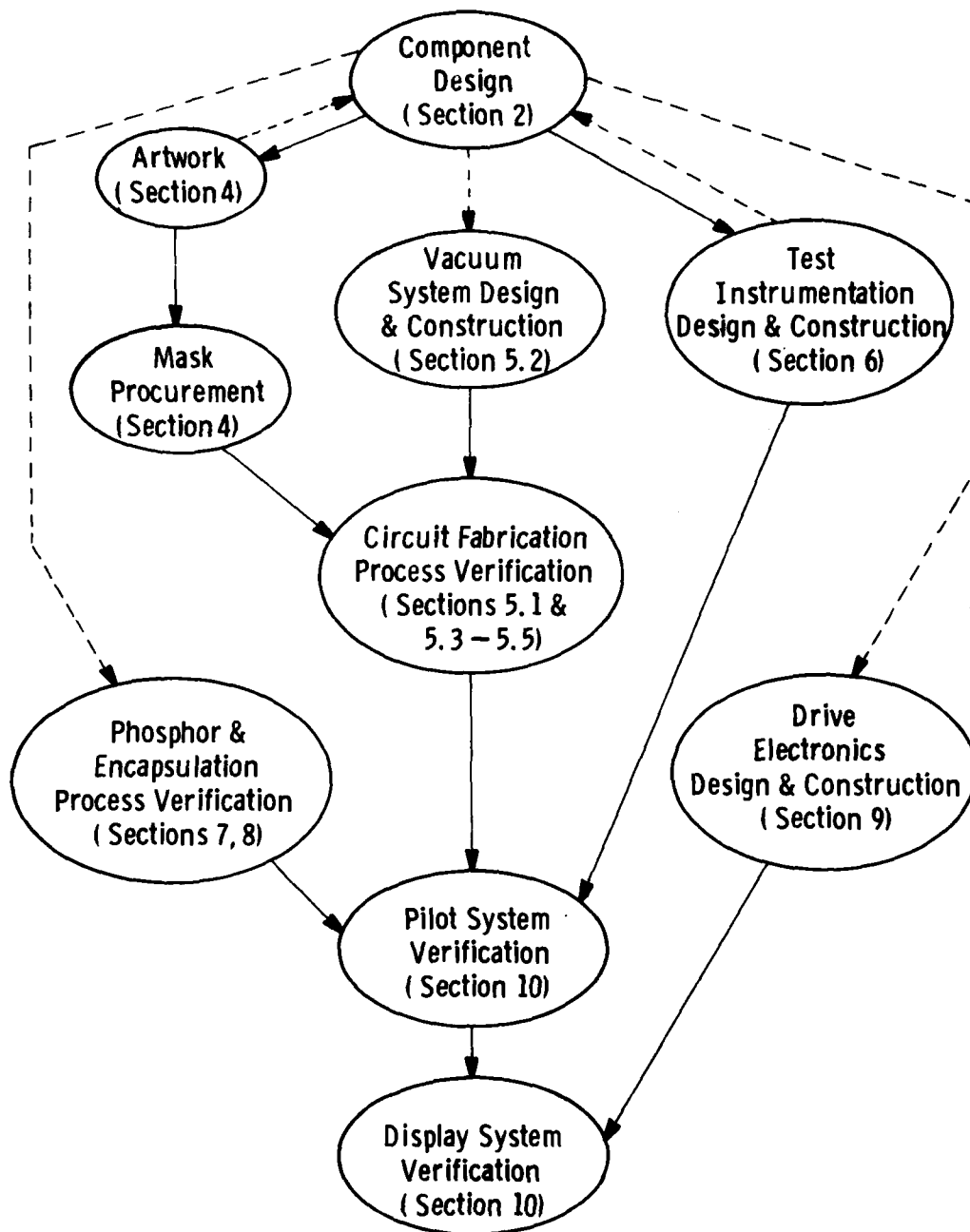
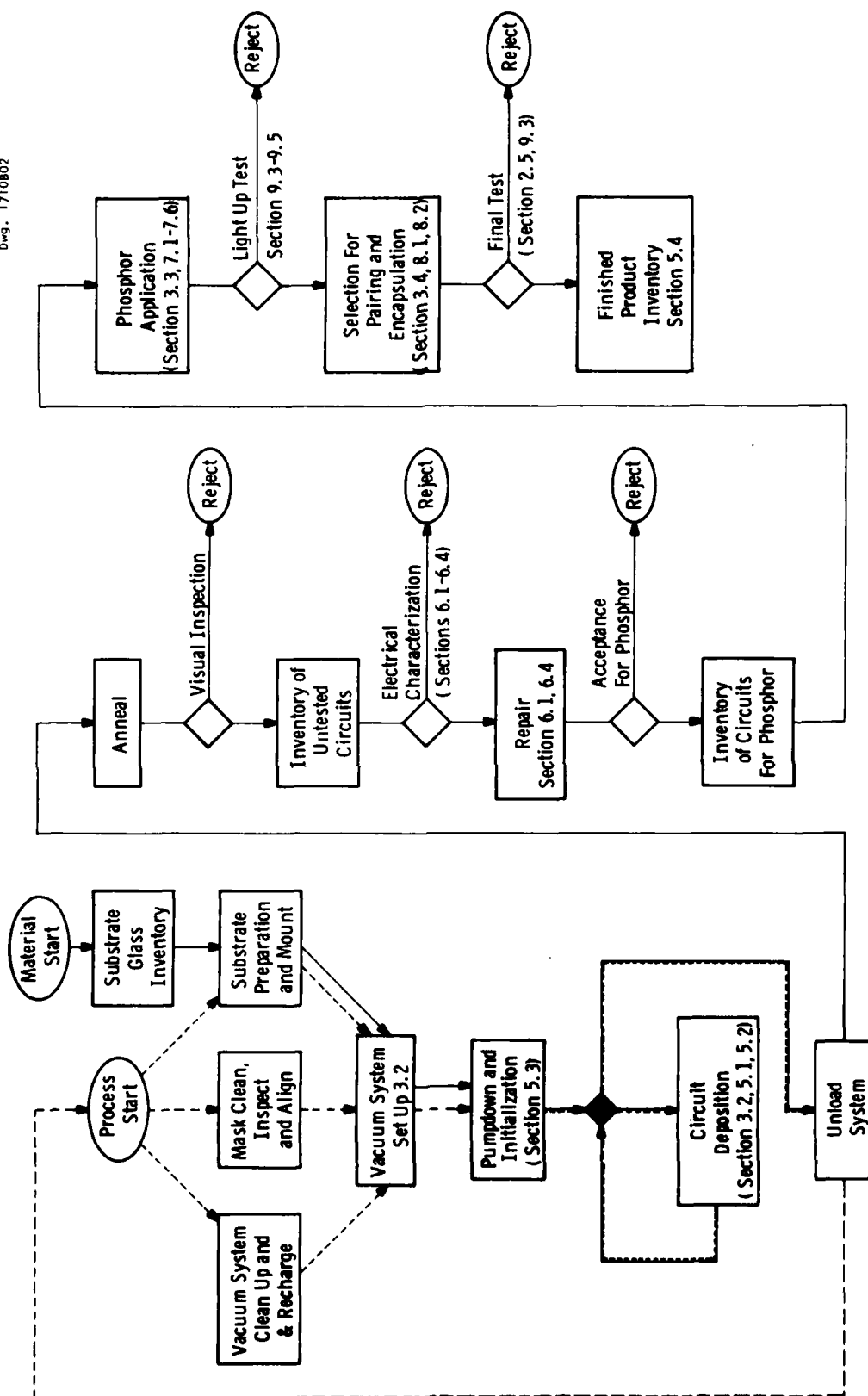


Figure 3.1 Class I, Non-recurring, Tasks Associated with Pilot Production of the Display



**Figure 3.2 Class II Recurring Tasks Associated with the Fabrication Cycle.**



arrows indicate the task sequence during the fabrication of the thin film circuit. The actual path of raw material as it is processed from a glass substrate to a working electroluminescent display is indicated by solid arrows. Each process step or work station description in Figure 3.2 is supplemented by reference to other sections of this report where technical and operational detail is provided. Where no such reference is made, the topic will be described in this section.

Firstly, with reference to the vacuum deposition system cycle, three separate operations are conducted in parallel, and require about four to eight elapsed hours with two operators. Each of these operations which are:

- substrate glass preparation and pre-cleaning
- mask clean and inspect
- vacuum system clean up and recharge

will now be described sequentially.

The substrate glass is first bevelled, by grinding its eight major edges to prevent splinters later breaking off and contaminating the circuit. The debris is rinsed off in DI water, with simultaneous brushing. Each piece of glass is then soaked more than twelve hours in Micro<sup>TM</sup>, a detergent solution. Experience indicated this step was critical in the cleaning process. The substrates are then brushed with the Micro solution and rinsed continuously in Super Q water until the rinsing water reaches the 18 M $\Omega$  level. After drying in an oven dedicated to the purpose, they are inspected under UV light. The last two steps are executed under Class 100 clean air conditions. Experience has indicated that circuit defect levels correlate strongly with the UV visual inspection. More explicitly, substrates passing the UV inspection test typically exhibited few or no circuit defects which could subsequently be related to substrate contamination.

Mounting substrates to their holders is accomplished using the guide pin features of the holder for location and Duco<sup>TM</sup> cement, applied through a syringe, for adhesion. Ordinarily eight substrates are mounted for each run, commensurate with the capacity of the vacuum deposition equipment. The substrate holder hardware is described in

further detail in Section 5.2. The actual eight pieces used are selected from a batch of typically twelve pieces of glass entering the cleaning procedure, UV inspection providing the basis for selection. The substrate-holder assemblies are kept under Class 100 flow until ready for mounting in the vacuum system. Experience indicated that this time should be minimized. Typical practice was not to schedule substrate glass preparation until events in the parallel operations indicated precisely when it would be needed.

The principle of the mask cleaning process is to chemically etch with sodium hydroxide a film of aluminum applied to the relief side of each mask during the pre-processing operation described as "Initialization" in Figure 3.2. During the etch, the materials accumulated on the mask during processing are readily lifted off. The explicit mask cleaning process begins with separating the masks from their holders. Both each mask and its holder are then submerged in 10% sodium hydroxide. The mask holder is supported in a pan by side supports to allow clearance for the guide pins, which face down. Sodium hydroxide solution is then poured into the pan until the solution level is higher than the mask holder. The mask itself is placed with the relief side up in a 190 mm evaporating dish with a wire mesh on the bottom. Sodium hydroxide solution is then poured into the dish to a level above the mask surface. After the specified 18 hours, the sodium hydroxide solution is poured off and all parts are rinsed in the following sequence:

1. D.I. tap water
2. 8 $\mu$  filtered D.I. water
3. 3 $\mu$  filtered D.I. water
4. Filtered D.I. water with nitrogen bubbling

Bulk moisture is then removed with a ionized nitrogen gun in horizontal sweeps. The gun is held sufficiently far away to prevent damage from jet pressure to the more fragile masks. After all parts are dried in an oven at 100°C for 2 hours, they are reassembled for alignment.

The principle of dimensionally correct geometrical stenciling of sequential pattern segments onto any one substrate calls for accurate pre-alignment of each mask on its holder and subsequent precise registration of mask holder to substrate holder during the thin film pattern

synthesis. In Section 3.2, the technique of in-process registration is described as part of the vacuum system hardware. Here we are concerned with the alignment of each mask on its holder, considered the final phase of the inter-run mask processing procedure. A prerequisite is a "master plate", which is really nothing more than a substrate, mounted on a holder, with the pattern of the first mask ("GND#1 - HIC#1 - see Figure 3.3) replicated on it in metal. A distinguishing feature of this particular mask is the nature of the "alignment squares pattern" described in Figure 4.28 in Section 4.4.

With reference to Figure 4.28, the master plate alignment square pattern provides all sixteen of the smaller squares, while each mask other than the first has the larger squares as indicated and the sixteenth smaller square.

After each mask has been loosely secured to its holder, alignment is accomplished by using a split-field microscope to determine mask position in relation to a fixed pattern on the master plate. During the operation, the master substrate holder is mated with the respective mask holder. The split-field microscope enables the viewer to inspect two corners of the mask simultaneously. After the two upper corners are checked, an adjustment is made by lateral movement of the mask. Then the bottom two corners are checked and additional mask adjustment is made. This procedure is repeated cyclically until the alignment is correct in all four corners. When correct alignment is achieved, the composite patterns observed simultaneously through the split field microscope, each resemble Figure 3.3 with only one large square located as indicated.

Essential features of the mask alignment hardware are shown in Figure 3.4 which shows how the master plate substrate holder is modified to readily accept a magnet. This holds the mask firmly after adjustment while it is being clamped to its holder.

The third parallel task conducted prior to setup is vacuum system cleanup and recharge. Each E-gun well is opened and the shields removed. These are sand blasted clean. The hearths and filament mounts are scrubbed with emery cloth, and new observation mirrors are installed. The main vacuum chamber is vacuumed and fresh monitoring crystals are installed.

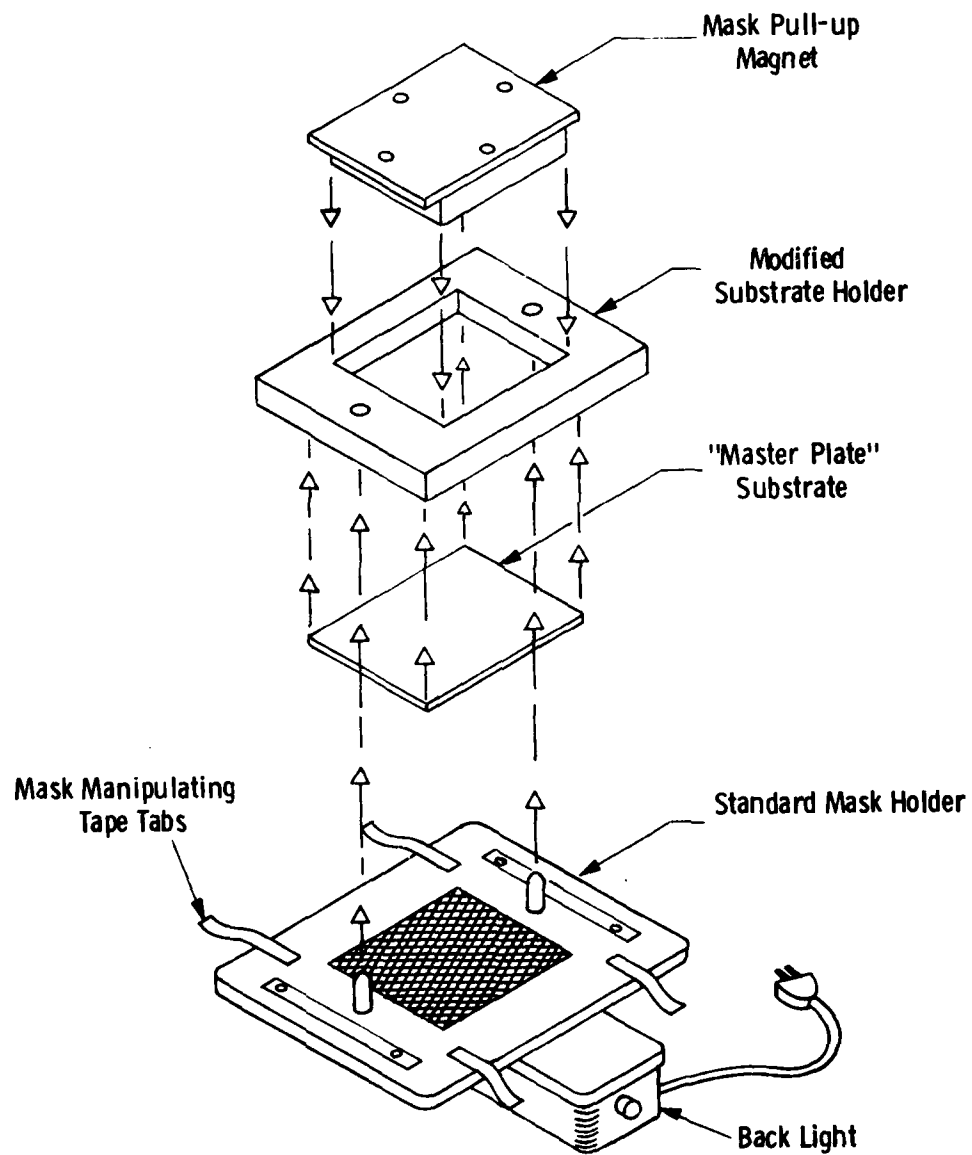


Figure 3.3 Essential features of the Mask Alignment Hardware

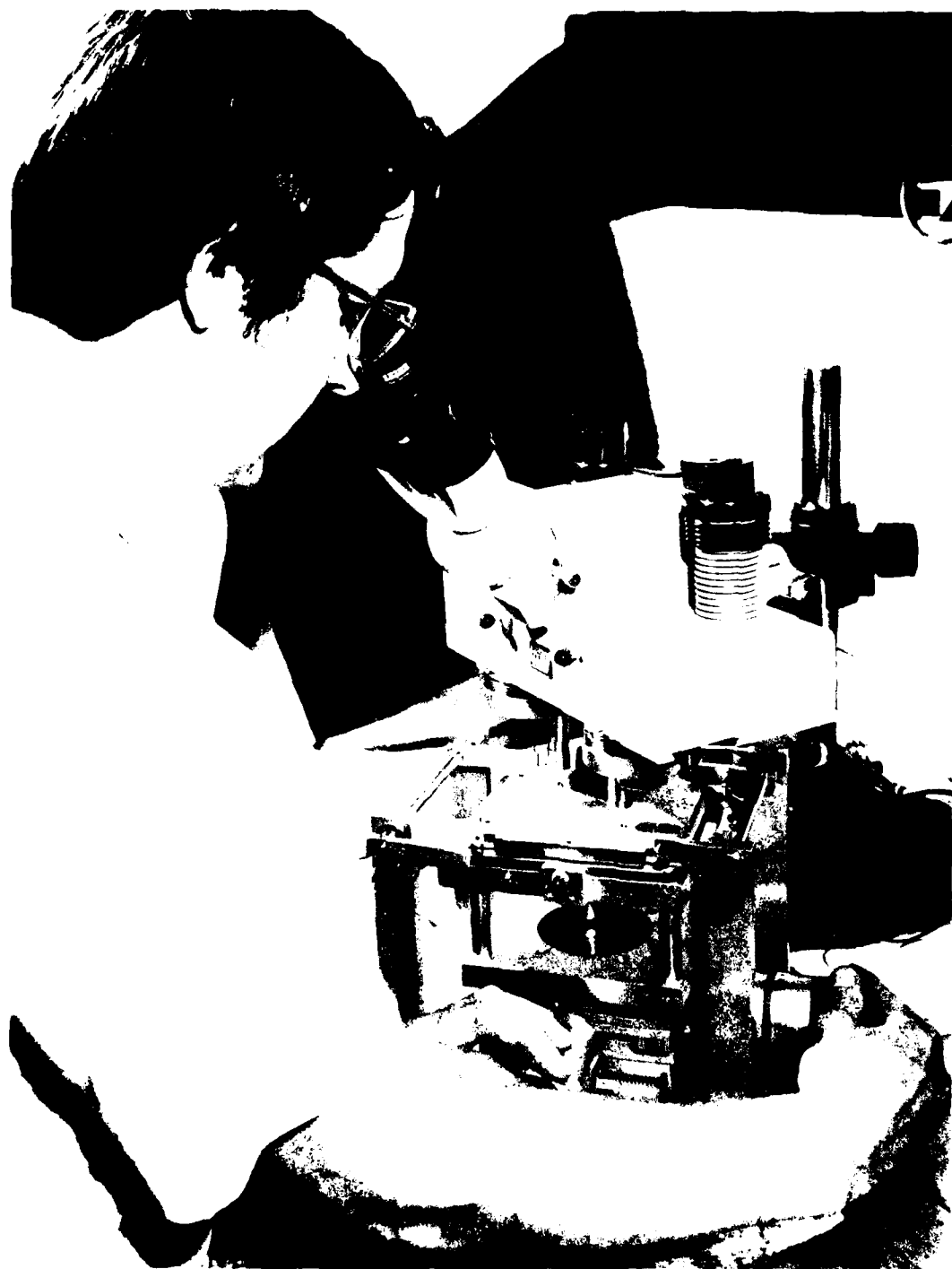


Fig. 3.4 Mask alignment with a split field microscope.

Vacuum system setup in Figure 3.2 refers to replacement of the mask, substrate and actuator wheels described in Section 3.2 and installation of the holder-premounted masks and substrates prepared as described above. First, the mask wheel is replaced from the rack where it was left in the previous unloading. Then the mask holders with pre-aligned masks are mounted on it. After that, the substrate wheel is installed and the substrate holders are attached to it. The next step commences when the actuator wheel is installed and connected up to its air lines. Finally, the lid of the chamber is lowered, the E-beam wells are closed up and pump-down sequence under computer control is initiated. Ordinarily, a starting vacuum of  $2-3 \times 10^{-7}$  torr is reached in about 5-10 hours. However, we consistently observed higher yields when the low vacuum was sustained for twice this time before starting.

Run "initialization" shown in Figure 3.2 refers to three separate operations which experience demanded prior to actual circuit synthesis. These are:

1. Source preheat
2. Mechanical exercise
3. Mask precoat

and are illustrated with process recipes in Figures 3.5 through 3.7 respectively. The format and interpretation of these recipes are described in Section 5.3. For the present, the source preheat implies simply the melt down and clean off the electron beam evaporated materials prior to their actual activation in circuit synthesis. This practice generally provides much "cleaner" patterns in the formation of metal films. In the case of the aluminum oxide insulator film source, we additionally had fairly convincing evidence that pre-heating substantially prevented the deadly cracked insulator syndrome, responsible for multiple bus bar discontinuities. A typical preheat recipe is shown in Figure 3.5.

Mechanical exercise simply refers to a procedure wherein one or more substrates is sequentially mated with each mask holder, automatically, under vacuum. The recipe is shown in Figure 3.6. There are two purposes. The first is removal of residual debris from each mask,

collecting it on the substrate selected for the exercise operation. We have faith in, but no conclusive evidence of its effectiveness in this respect. However, the second purpose was to avoid costly run abortion due to mechanical failure later in a run. Approximately, 50% of theoretical capacity was lost over the 3 1/2 year operating period due to failure at one time or another of the actuator's ability to properly mate the substrate and mask holder by remote, manual or automatic control under vacuum. The exercise operation was performed routinely at the beginning of a run in the hope that malfunctions, presumably originating in both wheel-locating microswitch failures or non-detectable improper mounting of the mask and/or substrate holders would be pre-deleted, thereby lowering the effective cost of run abortion.

The third run initialization operation is mask precoat. Firstly, an aluminum precoat is deposited on each mask being used for the first time after any cleaning. The purpose of this precoat is simply to facilitate later mask cleaning by lift-off etching with sodium hydroxide with the procedure described earlier. Secondly, a copper precoat on top of the aluminum is applied to insulator masks to enhance radiative cooling during evaporation.

Circuit deposition is executed on a substrate-by-substrate basis. That is, each circuit is completely synthesized before a new one is begun. Further details are described in the sections of this report indicated in Figure 3.2.

The vacuum system operating cycle is completed by the unload operation which is essentially the reverse of the setup procedure described previously. The finished circuits are identified with the coding described in Section 6.4 before removal from their substrate holders and annealing, a ten-hour 600°C cycle, with a dry nitrogen ambient.

The remainder of the manufacturing process in overview is readily determined from Figure 3.2 which provides cross-reference to relevant descriptive material elsewhere in this report.

RECIPE ID = RM4039

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	1	11	3100	2.70	22/5.0	25/.5	10	1000	1000	6.0X8	AL	GND-HIC1
2	EB1	1	11	4100	4.00	60/4.0	80/.1	15	1000	1000	6.0X8	AD	GND-HIC1
3	EB2	2	11	3100	8.90	22/2.0	28/.2	10	200	200	6.0X8	NI	GND-HIC1
4	EB1	2	11	4100	4.00	60/4.0	80/.1	15	1000	1000	6.0X8	AD	GND-HIC1
5	EB2	4	11	3100	7.30	20/2.0	22/.1	10	200	200	6.0X8	IN	GND-HIC1
6	EB2	3	11	3100	19.30	22/2.0	28/.3	15	200	200	6.0X8	AU	GND-HIC1
7	EB1	3	11	4100	4.00	60/4.0	80/.1	15	1000	1000	6.0X8	AD	GND-HIC1
8	RES	0	11	3100	5.80	35/1.5	35/.5	5	1000	1000	6.0X8	CS	GND-HIC1
9	EB1	4	11	3100	2.70	22/5.0	25/.5	10	1000	1000	6.0X8	AD	GND-HIC1

Figure 3.5 Typical Preheat Recipe used During Run Initialization to pre-condition E-Beam Evaporated Sources



RECIPE ID = RM4007

LYR	STA	H	M	CHTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	GND-HIC1
2	EB2	2	2	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	HIC2VIC1
3	EB2	2	3	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	GATECAPG
4	EB1	2	4	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	AO	INSULATR
5	EB2	2	5	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	SO/DRAIN
6	EB2	2	6	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	VIC2TFIC
7	EB2	2	7	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	ELMIDCAP
8	RES	0	8	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	CS	LGPWSEMI
9	RES	0	9	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	CS	POWRSEMI
10	EB2	2	10	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	EDGECONS
11	EB2	2	11	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	GND-HIC1
12	EB2	2	12	3100	2.70	2/1.0	2/.2	2	10	12	6.0X8	NI	HIC2VIC1

Figure 3.6. Typical Exercise Recipe used in the Run Initialization Task

### 3.2 The Sequential Pattern Deposition Approach

In Section 3.1, the overall approach to the fabrication of the display was reviewed. An essential step in the process is the synthesis of the thin film transistor circuit matrix from a set of stencil masks. These circuits are unique in this sense and so, as a prelude to the detailed description of layout, design and mask fabrication in Section 4, we are presenting pictorially an example of how the circuit is formed.

Figures 3.7 and 3.8, respectively, indicate the state of the circuit at about the 50% and 100% levels of fabrication, respectively. Each diagram shows three complete elemental circuits and the test transistor pair.

Figure 3.7 shows the result of the first level metal formation synthesized from Masks 1, 2, 3 and the first insulator from Mask 4 with the following legend:

Mask 1	right crosshatch (metal)
Mask 2	left crosshatch (metal)
Mask 3	right & left crosshatch (metal)
Mask 4	no crosshatch (insulator)

The details of the individual mask patterns are shown later in Section 4.4. The result of their combination in this fashion is the formation of segmented but continuous "horizontal" busbars, the "bottom" gates of the double gated logic and power transistors, and one of two ground plates of the capacitor. The strategically located insulator segments prepare for the vertical busbar crossovers and proper isolation of the transistor semiconductor elements. Up to this point, the circuit is electrically passive.

Figure 3.8 shows how the segmented pattern approach completes the circuit. In addition to the four components patterns of Figure 3.7 with no shading, Figure 3.8 identifies the other components as follows:

Mask 5	right crosshatch (metal)
Mask 6	left crosshatch (metal)
Mask 8	double crosshatch (semiconductor)

At this point, the circuit and test transistors have been completely formed and the segments of the vertical busbars rendered continuous. The precision hardware used for this operation is described later in Subsection 5.2 and, as mentioned before, the task of mask design and procurement is documented fully in Section 4.

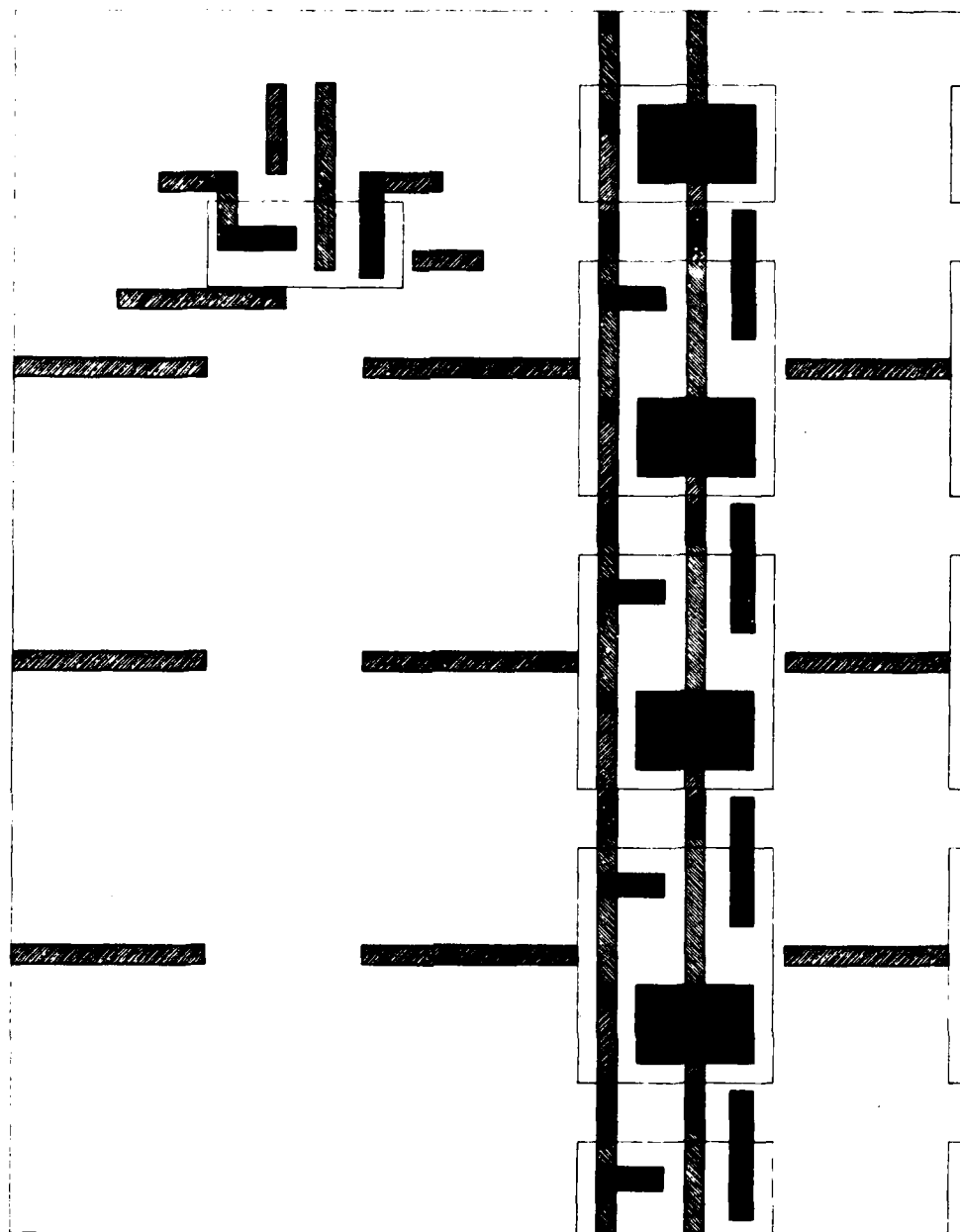


Fig. 3.7 Active layer, lower insulator and lower interconnect/gate layer.

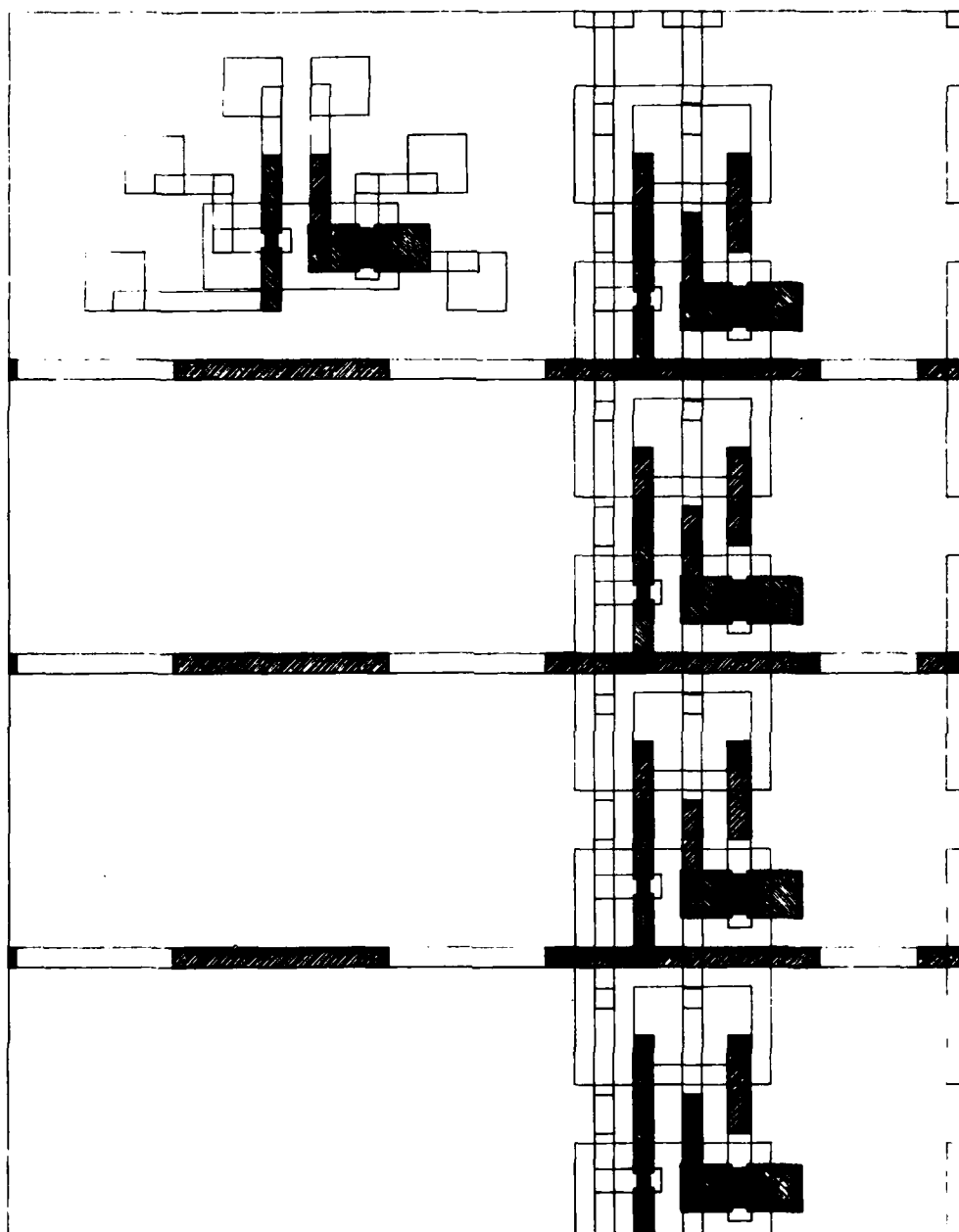


Fig. 3.8 All five major layers.

### 3.3 Powder Phosphor Application

#### Solid State Radiographic Image Amplifiers

The process of applying phosphor originates with Dr. Zoltan Szepesi's work on Solid State Radiographic Image Amplifiers. The solid state image amplifiers were intended as equivalent or improved replacements for fluoroscopic screens and x-ray film used in radiographic evaluations of space vehicle components and structures. Dr. Szepesi's report under NASA contract CR-61328, November 1969, Final Report, illustrates the use of powder phosphor in a plastic medium. The phosphor spray mixture at this time was:

27 g Westinghouse VB-241P EL phosphor  
90 ml 5% solution of cyanoethyl starch (CS)\*  
90 ml 5% solution of cyanoethyl sucrose (CES)\*

The plastic solutions (5%) above were:

40 g plastic: cyanoethyl starch (CS)\*  
or  
40 g plastic: cyanoethyl sucrose (CES)\*  
and  
220 ml dimethyl formamide (DMF)  
580 ml acetonitrile (AN)

\*Sold by Eastman Chemical Corporation.

Powder phosphor was mixed in the plastic solution and sprayed on the solid state radiographic image amplifiers by a "DeVilbiss" type spray gun. Four to five layers of phosphor mixture were sprayed with a 135°C bake for ten minutes at each layer. Following the appropriate number of phosphor layers, three to four layers of clear coat:

1:1 mixture of 5% CS and 5% CES were applied and a final bake at 135°C for 30 minutes.

The solid state radiographic image amplifier was then placed in high vacuum and a semi-transparent conductive lead-oxide, gold film was evaporated on the phosphor-plastic surface. With a surface-to-source distance of 18 inches, 64 mg of P60 was evaporated, followed by a Au evaporation until the sheet resistance measured 50 ohms/square.

The result was a "sandwiching" effect of a photoconductor layer, semiconductor layer, phosphor-plastic layer, and conductive, semi-transparent P60-Au layer.

#### 6 x 6 inch, 20-lpi Electroluminescent Display Panel

The next phase in the development of a phosphor process was the application of phosphor in relation to a 6 x 6 inch, 20 lpi Electroluminescent Display Panel as reported in IEEE Transactions on Electron Devices, Vol. ED-22, No. 9, September 1975. The authors of this paper, viz, T. P. Brody, Fang C. Luo, Zoltan P. Szepesi and David H. Davies relate the design, construction, and performance of a 12,000 element EL panel. Each element consisted of a x-y addressed logic transistor, power transistor, and storage capacitor. The completed thin-film circuit was covered with a sprayed EL phosphor and a Au/P60 layer formed a continuous top electrode.

The phosphor process for the Electroluminescent Display Panel was identical to that of the process developed for the Solid State Radiographic Image Amplifier. A phosphor-plastic mixture of the same proportions and content was sprayed on the display panel. A semi-transparent conductive layer of P60/Au was then evaporated in the same manner and specifications.

The result was a "sandwich" of a thin film transistor layer, a phosphor-plastic layer and a semi-transparent, conductive layer of P60/Au.

#### Manufacturing Methods and Engineering for TFT Addressed Display

The Manufacturing Methods and Engineering contract DAAB07- is an investigation of manufacturing methods and engineering as related

to the development of a Digital Message Device (DMD). In the early evolution of phosphor application processes, the quantity of substrates requiring phosphor was small on a day-to-day basis. Each substrate underwent an intense, time-consuming procedure to assure proper results. The major component of the DMD process is an automated evaporation system utilizing a dedicated mask approach towards manufacturing displays. This automated system increased greatly the number of substrates that phosphor was to be applied to. Efforts were dedicated to increasing the phosphor application throughput to match this increased output of display panels. In the later stage of the contract when results of testing indicated that the phosphor process would not meet temperature specifications (operation at 72°C), new procedures and processes were developed to meet this requirement. Thus, phosphor development will be referred to as phase I and phase II in relation to this juncture of developing a phosphor process to meet requirements at an operating temperature of 72°C.

#### Phase I

##### Early Development

- A. Through work on radiographic image amplifiers and electroluminescent display panels a phosphor-plastic (CS and CES) EL medium was formulated.
- B. This phosphor-plastic was applied to each substrate by spraying repetitive coats alternated by baking steps.
- C. Each substrate phosphor area was masked using tape in a labor intensive, time-consuming manner.
- D. One substrate was coated with phosphor at a time.
- E. One substrate at a time was loaded into a vacuum system and a layer of P60/Au evaporated to form the top electrode.

##### DMD Development

- A. The phosphor-plastic formulation and spraying process was retained.



B. Metal edge masks were developed and holders designed to allow the masking of multiple half-DMD substrates.

C. Through holders designed to hold multiple half-DMD's and a process of alternately spraying and baking substrates, four half-DMD's could be processed at a given time.

D. Holders were designed and metal edge masks developed to allow the loading of two half-DMD's in the vacuum system for the evaporation of the top electrode. The top electrode formulation was retained.

Half-DMD substrates processed in this fashion allowed the phosphor application process to increase throughput to match the output of the manufacturing facility. Testing of the DMD's at 72°C proved that the phosphor-plastic formulation was incapable of meeting requirements. Efforts were made to find a phosphor medium capable of meeting the 72°C operation requirement. Through the primary efforts of L. Scala and J. X. Przybysz, a new phosphor medium was developed. This medium is a cyanoetholated-PVA in a 30/70 mixture of MEK and cyclohexanone. The "PVA" formulation is sprayed on the substrate and the substrate is heated and phosphor brushed into the "PVA." This process proves capable of operation at 72°C. J. X. Przybysz also discovered that P60 was detrimental to phosphor maintenance; hence, cadmium fluoride was substituted for P60 in the composition of the top electrode.

## Phase II

### DMD Development

A. The new "PVA" formulation is sprayed on the half-DMD substrates in repetitive layers with the same equipment as the phosphor-plastic medium was. Since the entire substrate can be sprayed, no masking is necessary and multiple substrates can be processed. Each layer is alternately sprayed and baked.

B. The substrates are then heated and phosphor is brushed into the "PVA" surface. No masking is necessary, allowing multiple substrates to be brushed.

C. A top layer of "PVA" is then sprayed on the substrates. This top layer is applied in two sprayings with a bake between sprayings and after. No masking is required; thus, multiple substrates can be processed.

D. The edge contacts of each half-DMD are then cleaned off "PVA"-phosphor with acetone.

E. Two half-DMD's are then placed in a holder and metal edge masks positioned to define area of top electrode. The holder is placed in a vacuum system for the deposition of cadmium fluoride-gold.

1. A thickness monitor is utilized to insure consistent thickness of materials in the top electrode.

Since the only labor-intensive steps are masking before evaporation of top-electrode, and the cleaning of "PVA"-phosphor from the half-DMD edge contacts by hand, the process allows throughput to match that of the automated evaporation system, manufacturing the half-DMD's.

### 3.4 Encapsulation

With regard to displays, the structure of the development areas basically consisted of circuit manufacture, phosphor application, and encapsulation. It becomes apparent then that encapsulation efforts paralleled the history of phosphor development. Early radiographic image amplifiers and electroluminescent display panels required encapsulation. These efforts resulted in the selection of Stycast<sup>®</sup> epoxy as the encapsulant. The panels were masked by hand to protect contact areas. Epoxy was poured onto the panel surface in the center of the panel. A cover glass was slowly lowered on the panel to prevent air trapping. The weight of the cover glass forced the epoxy to cover the entire surface of the panel and the excess flowed out over the edges. Continuous monitoring was necessary to ensure that the cover glass remained in the proper location and to wipe the excess epoxy flowing

from under cover glass. The epoxy was allowed to harden partially and then the panel was placed in an oven for curing. After cure, excess epoxy was removed by the use of a razor blade. When the automatic evaporation system for the manufacture of DMDs was put into operation, throughput once again became a problem. The early labor-intensive methods proved unacceptable. Later in the development phase, testing at 72°C proved that epoxy as an encapsulant was unsatisfactory. Thus, the manufacturing approach to encapsulation was divided into what can be called phase I and phase II.

#### Phase I

##### Early Development

A. Radiographic image amplifiers and electroluminescent panels were masked with tape to protect contact areas.

B. Stycast<sup>®</sup> epoxy was mixed and poured on center area of panel.

C. A cover glass was slowly lowered in hinge-like fashion to prevent entrapment of air. The weight of the cover glass forced epoxy in center to flow outward covering entire surface.

D. As excess epoxy flowed from edges of cover glass, cotton swabs were used to remove this excess epoxy.

E. As the epoxy semi-hardened, flow of excess epoxy stopped. The masking tape was then removed from contact areas and the contacts cleaned with acetone.

F. Panel was then baked to effect curing of epoxy.

G. After curing, excess epoxy that was on back of panel and on surface of cover glass was removed with a razor blade.

H. The back and front of panel was then cleaned with acetone and methanol.

### DMD Development

Since all DMD panels are of the same geometry, package size becomes constant. This factor allows the design of a mold to eliminate time intensive steps in the encapsulation process and increase throughput to match that of the manufacturing facility. A DMD is composed of two halves since the output of the manufacturing facility is half panels. This necessitated the fact that the package consist of a back-plate, two half panel displays and a cover glass. Because of the fixed geometry, glass was purchased to dimensions with high accuracy requirements and a high degree of flatness. Two half DMD s are abutted face down, then the back plate is secured to the two halves with double adhesive tape. The double adhesive tape effects the sealing of the back of a panel to the back plate and secures the position of the half panels into the configuration of a DMD. A fixture was designed to permit the alignment of the two halves before the placement of the back-plate. This fixture also ensures the proper placement of the back plate. The encapsulating mold protects the edge contacts from the encapsulant and properly positions the cover glass.

A. A glass back plate is prepared by applying double adhesive tape to one side.

B. Two half-DMD s are placed in an alignment holder and aligned.

C. The paper cover on the double adhesive tape is removed from the back plate exposing the adhesive.

D. The back plate is lowered on the two half-DMD s with the adhesive down. The back plate guides on the alignment fixture properly position the back plate.

E. The back plate is pressed to the two half-DMD s to secure the adhesive.

F. The DMD is then placed face up in the encapsulating mold centered to all sides.

G. Epoxy is poured across center of DMD.

H. The cover glass is lowered hinge-like on top of the epoxy to ensure no entrapment of air. The mold rails ensure proper position of cover glass.

I. Mold is left at room temperature until epoxy is cured.

J. Mold is then broken down and DMD removed. Mold release prevents adhesion of epoxy to mold.

K. Excess "flashing" of epoxy on cover glass is removed with a razor blade.

L. Front and back of DMD is cleaned with acetone and methanol.

#### Phase II

The testing of DMD panels at 72°C and at high humidity proved that the use of epoxy as an encapsulant was unsatisfactory. Data gathered by testing "Postage Stamps" (small substrates that simulated a DMD package) had shown that a silicone rubber compound was superior to epoxy as an encapsulant. Humidity protection was also enhanced by reducing the area of the Riston<sup>®</sup> border to allow greater area of cover glass to substrate glass seal around the perimeter of the cover glass.

The Riston<sup>®</sup> area on all half-DMDs was reduced by the redesign of the Riston<sup>®</sup> phototool. The encapsulation process remains the same with the substitution of silicon rubber instead of epoxy. The utilization of an abutment fixture with its alignment guides for placing the back plate, the use of an encapsulation mold to position top cover and protect contact areas, allow DMDs to be encapsulated without time and labor intensive monitoring and clean-up of the original process. This optimization allows throughput to match the output of the Manufacturing Facility.

## 4. MASK AND PATTERN DESIGN

### 4.1 Historical Review

In Section 3.1, we have described in general terms the approach to the manufacturing process featuring synthesis of the thin film circuit matrix by sequential selective vacuum depositions through metallic stencil masks. During the first two phases of the contract, we developed in conjunction with an outside mask supplier, a design for the stencil masks embodying nickel plating of a beryllium-copper core. The nickel plating was first patterned onto the core material using conventional optical lithography and then plated up. Apertures were then etched in the core using the plated nickel as a resist and finally the entire structure was flashed with nickel.

In subsequent subsections herein we describe how and why an alternative approach was adopted during the final third phase of the program. The detailed description of the new approach to mask fabrication contains much material relevant to the earlier one. However, it focuses on the second approach because of its advantages which become evident during the discussion.

### 4.2 Mask Fabrication Approach and Method

In this context, mask design means the materials used in, and the physical construction of, the stencil masks themselves. It includes geometric specifications other than those which pertain exclusively to the thin-film pattern. In other words, it concerns dimensions such as mask thickness and area which generally apply in common to all masks of a set, a set being the combination responsible for generating the required thin film pattern. Consequently, the overall geometry of any particular stencil mask embodies two designs: the mask design and the pattern design. The former is usually the same for all masks of a set and the latter varies from mask to mask within a set. We are concerned in this section only with the mask design.

In principle, the mask design and the pattern design can be changed independently or together. The strategy discussed in Section 1.5.6 for Phase III disclosed the intention to do both. The existing mask construction was originally a nickel plated beryllium-copper core with a total thickness of .003" to .005". The specific reasons a change to nickel plated Kovar are:

1. The Be-Cu cored structure has inferior temperature resistance characteristics. The temperature of the masks rises severely, particularly during  $Al_2O_3$  evaporation. The induced mechanical distortion produces inadequately defined thin film patterns. This can be satisfactorily prevented by the cumbersome expedient of mounting a patterned Kovar shield between the evaporant source and the BeCu mask defining the pattern as described in the second Quarterly Report. However, it imposes an unneeded additional burden on vacuum system operation.
2. Due to their metallurgy, the Kovar masks respond much better than the nickel plated Be-Cu versions to the magnetic pull-up used to ensure mask to substrate contact.

The details of the mechanics of the process whereby the masks are fabricated are known only to the mask supplier. Basically, Westinghouse provides a pair of master photoplates from which the supplier generates copies to be used in so-called phototooling, which is then stored for any future use in the supplier's vault. Considerations involving our preparation of the photoplates are discussed later in Section 4.5 herein. Whereas details of the phototooling itself and the mask etching and plating procedures are retained by the supplier as proprietary information, we can disclose here the general approach to the fabrication of these particular masks. Both the supplier and Westinghouse have agreed that sharing the technology at this level was necessary for successful completion of the overall operation.

The process is most readily described by examining the gestation and birth of a particular aperture, starting from a plain sheet of Kovar. However, as a prelude, essential features of the cross-section of a finished aperture, for this new type of mask, in contact with a substrate in a vacuum system, are illustrated in Figure 4.1.

Referring to Figure 4.1, which introduces extensively used mask-related jargon, we observe a roughly conically shaped mask aperture defining a pattern required on the substrate. This configuration prevents "shadowing" which might otherwise occur at the geometrical extremities of the substrate due to the finite substrate-source separation, known as the "throw distance". Consequently, the stencil mask is said to have a "defining side" and a "relief side" as indicated in the figure. Mechanical integrity of the mask derives largely from the Kovar core. Pattern definition is provided by the "nickel top plate". The supplier chooses to apply the "nickel flash" layer over the composite structure. The "gold plating base" is essential for the fabrication procedure but not for mask performance. As indicated in the caption for Figure 4.1, the relative physical geometry of the various features of the mask are highly distorted. Dimensions in the formation of a conical aperture with a section of  $W = 100 \mu$  are shown more to scale in Figure 4.2. Here the gold plating base has been omitted, but a new feature, the "undercut", is specified. Ideally, this should be zero. Due to anomalies in the mask fabrication process, it typically registers 40 to  $100\mu$  as shown.

Gross features of the mask fabrication can be understood by reference to the formation of a particular aperture are illustrated in Figure 4.3 A through I.

Figure 4.3A shows the basic  $75\mu$  Kovar core, gold-plated on the future defining side of the mask. Both sides are then covered with photoresist as shown in Figure 4.3B and the composite assembly is mounted in the phototooling. The photoplates from which it is made have previously been supplied by Westinghouse and feature special so-called "target squares" (described in Section 4.5) to aid in the prealignment of the phototooling. Whereas the photoplate pattern on the relief side matches



Dwg. 7698A89

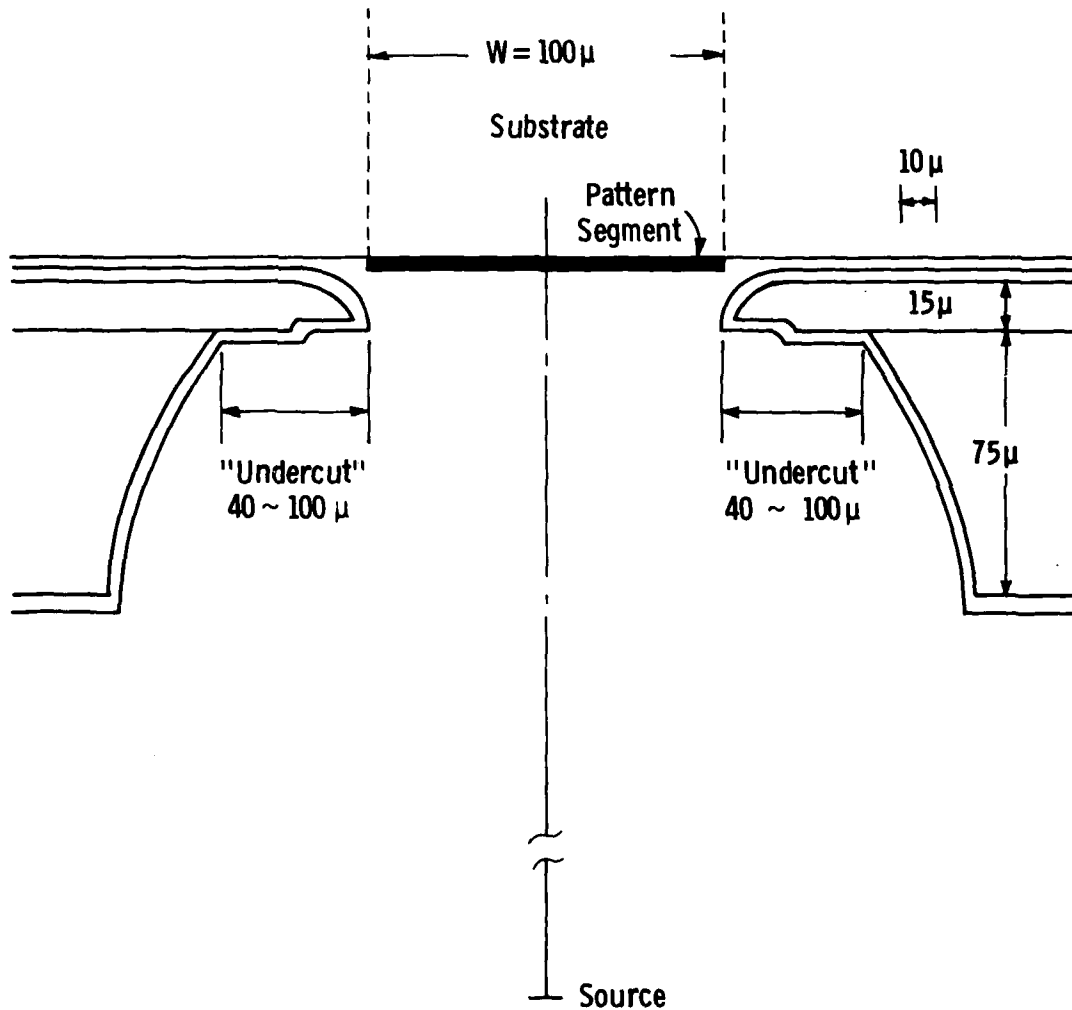


Figure 4.1 Essential features of the cross-section of a typical aperture of a Kovar cored mask in contact with the substrate receiving a thin film pattern component. (Dimensions are geometrically distorted for purposes of exposition ).

Dwg. 7698A90

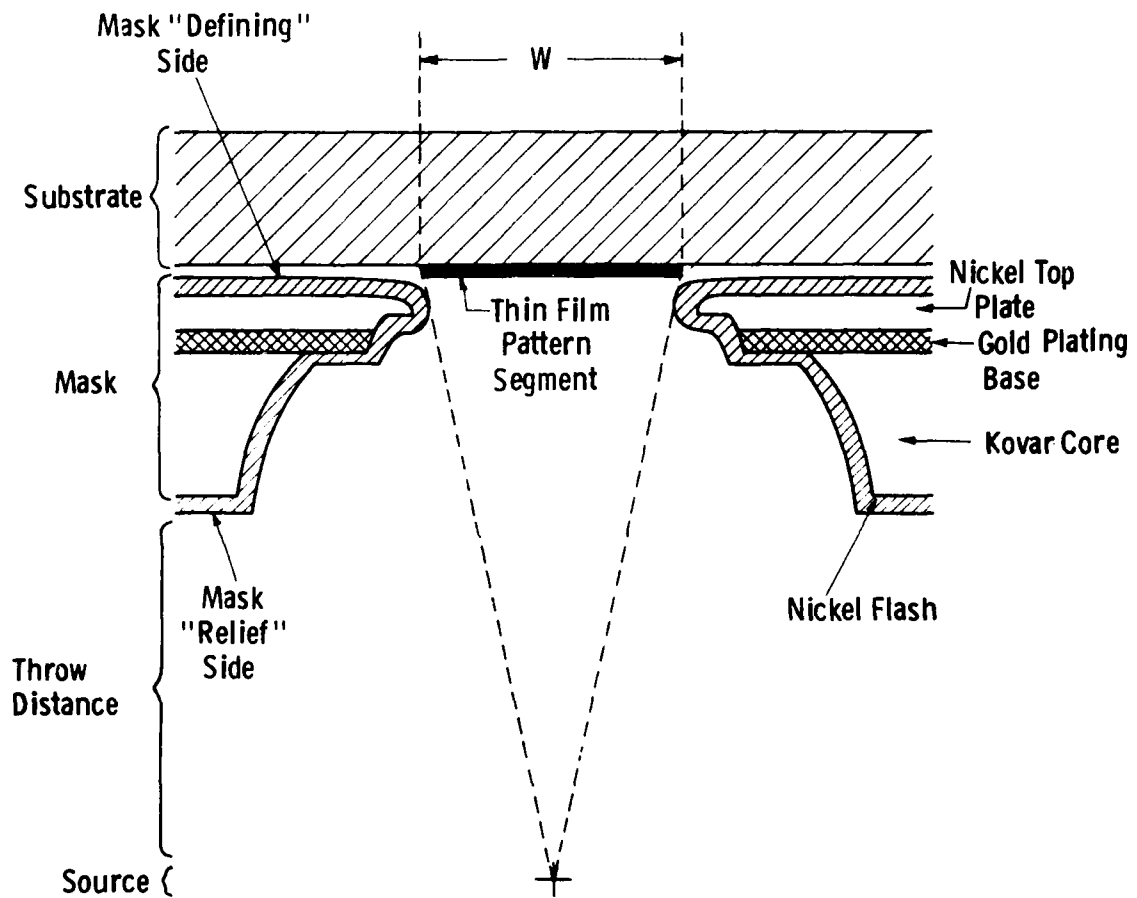


Figure 4.2 Typical dimensions of a mask aperture generating a 100 $\mu$  pattern segment.

that of the eventual aperture pattern, the defining side photoplate aperture images have been "opened up" by  $10\mu$  on an edge by prior post-processing of the digitized artwork.

The phototooling then provides for simultaneous exposure of the resist layers on the two sides. After development, the resist has the configuration shown in Figure 4.3D. After the assembly is removed from the phototooling, the patterned relief side is coated with wax to permit selective nickel plating of the defining side as shown in Figure 4.3E. This is the point where the nickel plating "overhangs" the resist to the extent of the  $10\mu$  per edge compensation of the photoplate artwork, thereby defining the required aperture dimension. The wax is then removed from the relief side and a new layer is applied to the resist-patterned nickel plating on the defining side as shown in Figure 4.3F. The structure is then ready for the selective etching of the Kovar, limited by the defining side gold plate and the relief side photoresist generating the configuration shown in Figure 4.3G. After removal of the wax from the defining side, and photoresist from both sides, only the thin membrane of gold plating remains blocking the aperture. This is selectively etched away and the resulting aperture pattern is finally flashed with a thin layer of nickel plating as indicated in Figure 4.3I.

The geometrical precision of masks made by the above process is excellent--certainly more than adequate to meet mask-to-mask registration requirements. Typically, we observed  $\pm 5\mu$  mask-to-mask registration over a 10 cm dimension. This is far superior to the very irregular and marginal  $\pm 20\mu$  mask-to-mask registration we formerly observed with the Be-Cu cored structure. These were made by a somewhat simpler process than that illustrated in Figures 4.3A through 4.3I. The Kovar maske have also better temperature excursion resistance. For example, it was mandatory during the evaporation of the  $Al_2O_3$  insulator through Be-Cu cored structures to shield the relief side with a so-called "back up" mask which featured matching apertures on a much coarser scale to prevent shadowing. Whereas the backup masks also served to promote magnetic adhesion of the defining side of the pattern mask to the

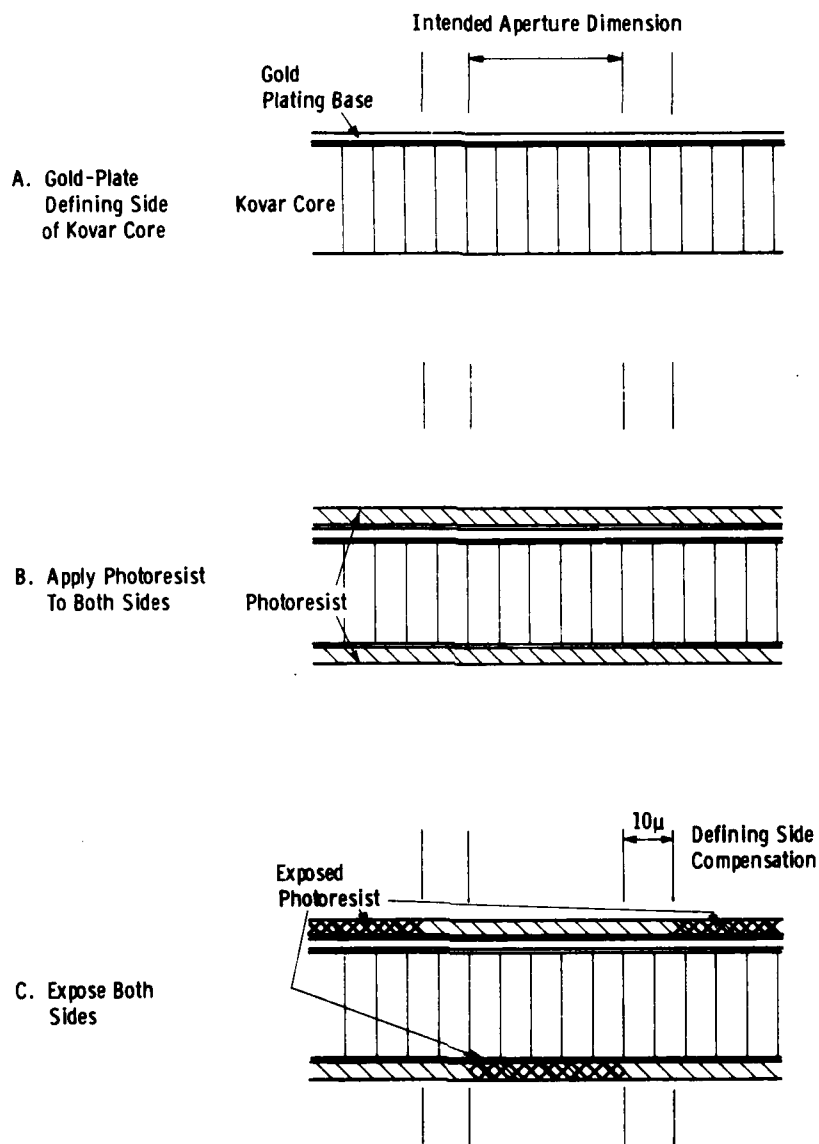
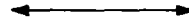
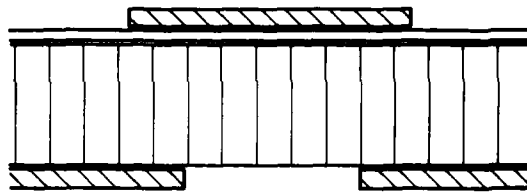


Figure 4.3 Fabrication of an aperture in a Kovar-cored mask—first three steps.

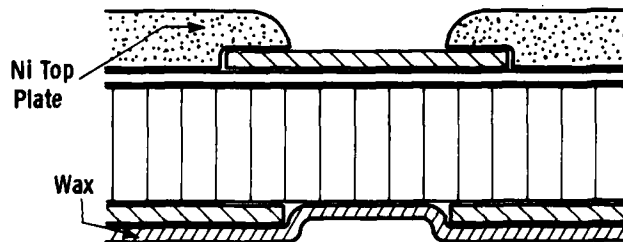
Intended Aperture Dimension



D. Develop Photoresist



E. Wax Seal Relief Side and Plate Defining Side



F. Shop Wax From Relief Side & Wax Defining Side.

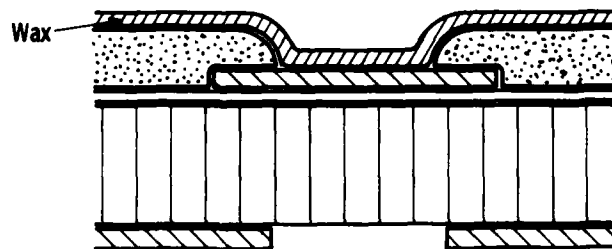
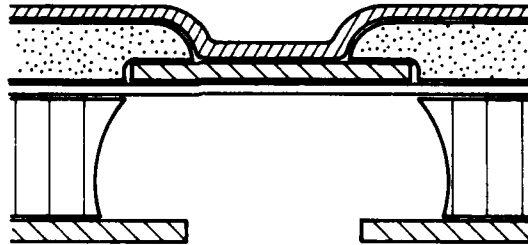


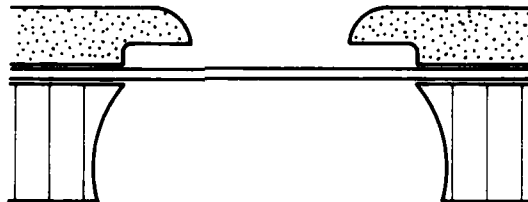
Figure 4.3 (continued) Fabrication of an aperture in a Kovar-cored mask-- second three steps.

Curve 1706884

G. Etch Kovar Core  
From Relief  
Side



H. Remove Wax  
& Resist



I. Etch Gold Membrane  
& Nickel Flash.

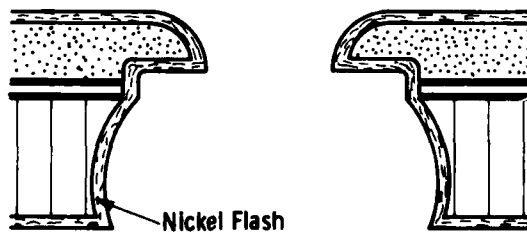


Figure 4.3 (continued) Fabrication of an aperture in a Kovar-cored mask--last three steps.

substrate, they also shielded the pattern mask from excessive heat of condensation. However, we have found even with the new Kovar masks, a copper precoat of the  $\text{Al}_2\text{O}_3$  mask is necessary to prevent temperature induced distortion during evaporation. We believe the copper precoat promotes radiant cooling. Without the copper precoat, mask distortion and accompanying loss of pattern definition ensues.

One problem unique to the Kovar construction is the appearance of pinholes through non-reinforced areas of the nickel top plate as illustrated in Figure 4.4. They originate through flaws in the first step of the mask fabrication, namely, the gold plating of the defining side of the raw Kovar stock. As a result, the nickel fails to plate these pinhole areas. As long as such potential pinholes are not located in regions where the Kovar core is subsequently etched out to provide the desired aperture pattern, such as on the right in Figure 4.4, local flaws in the gold plating are inconsequential. However, if they occur in locations such as on the left in Figure 4.4, the defect may destroy the resulting pattern electrical integrity for obvious reasons. One could, of course, insist on delivery of flaw-free masks. However, whereas the mask supplier has worked diligently to eliminate this problem as far as possible, we compromised in the tentative acceptance of masks with pinhole defects pending our later determination of the criticality of the defects. This is largely because of the very tight schedule under which the entire mask redesign and procurement task was knowingly undertaken. For similar reasons, we chose to be forgiving concerning another facet of the mask fabrication process. In Figure 4.4, for example, one could argue that if the Kovar etching were properly controlled, the undercut region would not exist. The Kovar would be etched only to the extent necessary to define the aperture. Besides eliminating the pinhole defects, the mask could have better overall mechanical integrity. However, we have no reason to disbelieve the supplier when he says etching to perfection is an extremely difficult process. We, therefore, took the route of tentative acceptance, again pending configuration of usability of each piece delivered. In retrospect, what we probably should have done was to have compensated the relief side photoplate in

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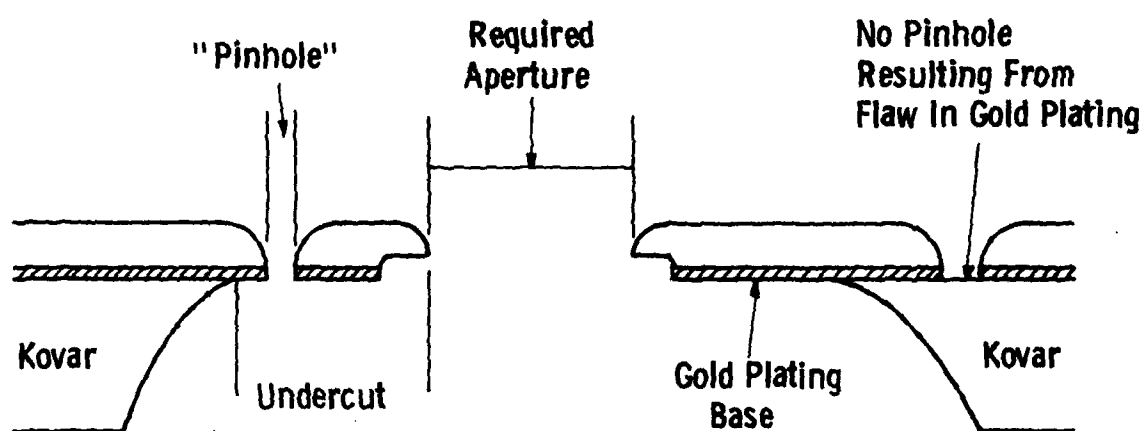


Figure 4.4 Pinhole formation in a Kovar-cored structure fabricated by the process illustrated in Figure 4.3.



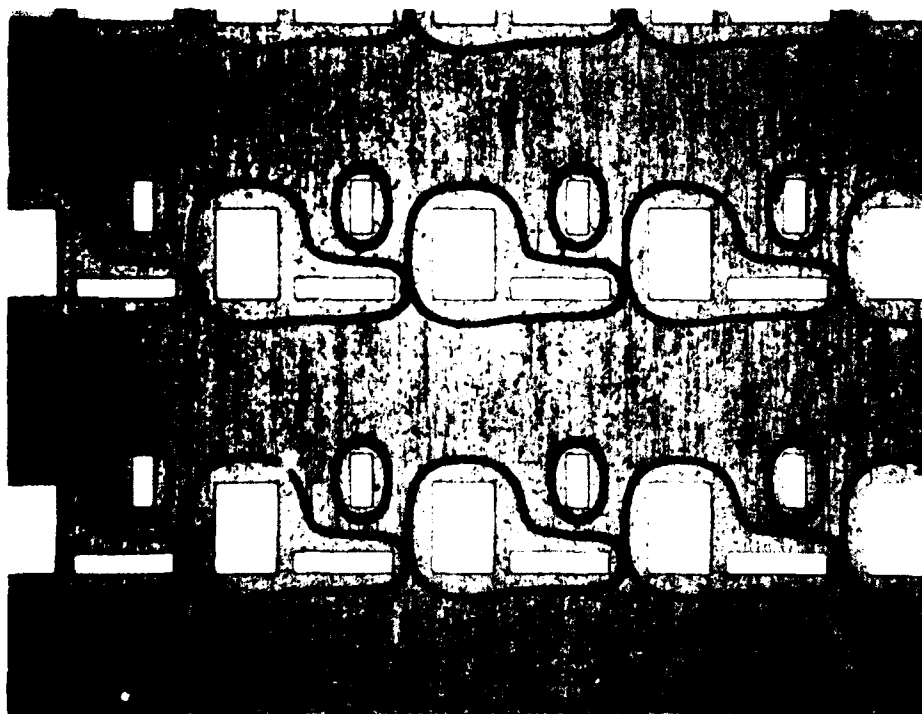


Fig. 4.5    Excellent mechanical integrity generated by Kovar etching to specification in the semiconductor pattern mask. The view is from the relief side.

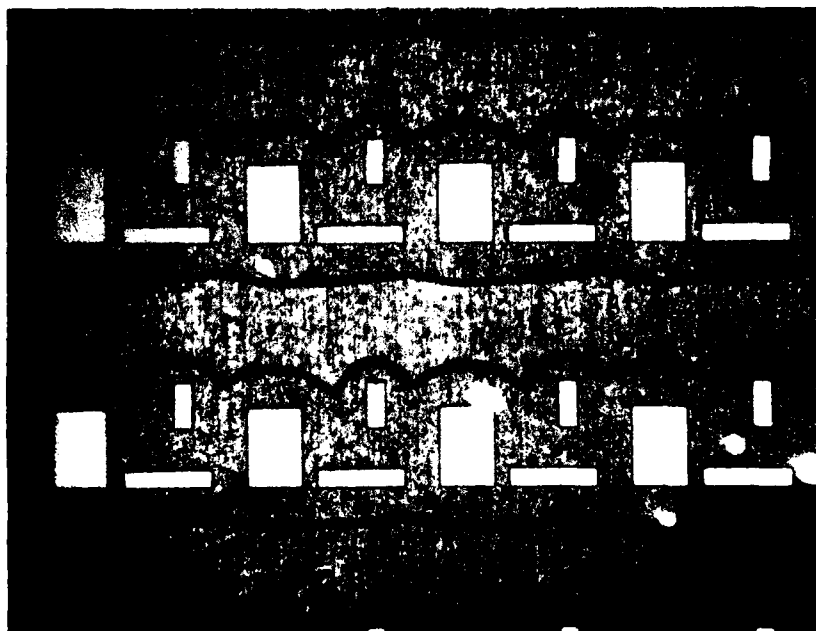


Figure 4.6 Pinholes generated by a combination of defective gold plating and over-etching of the Kovar core.

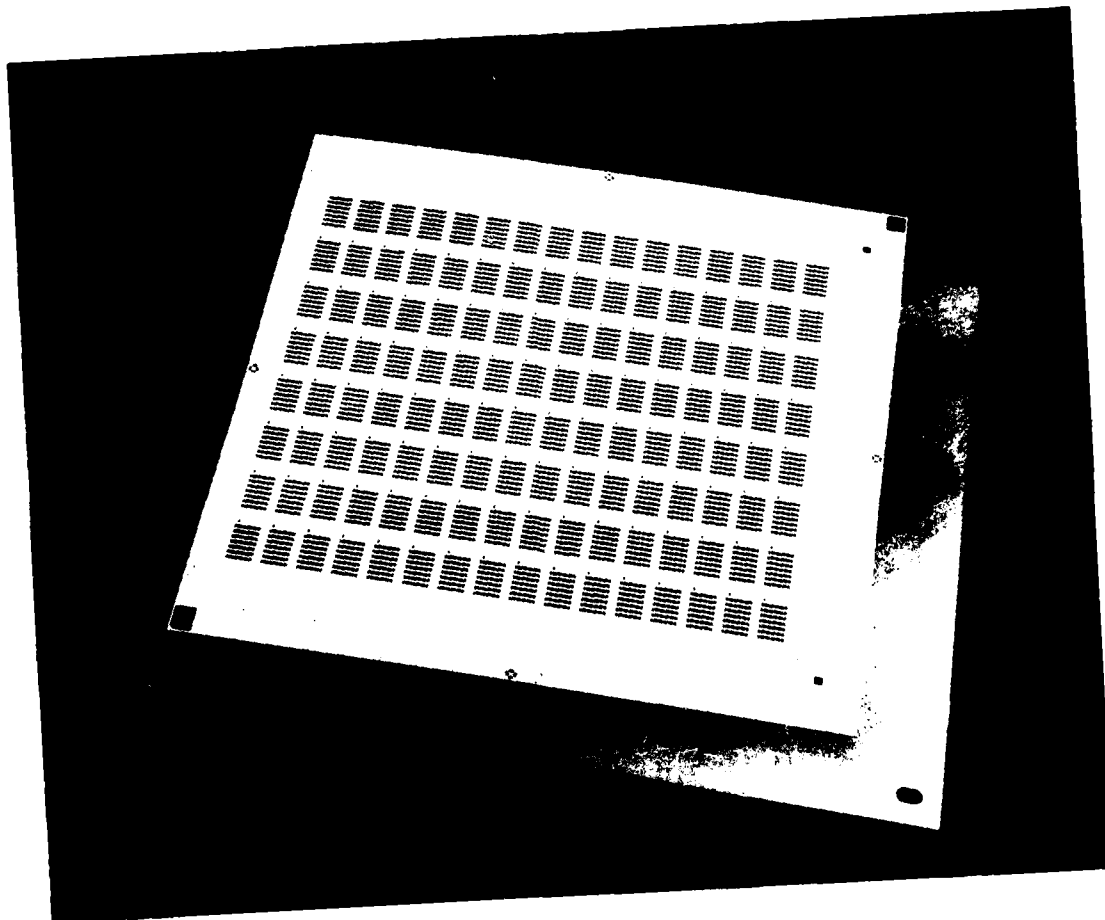


Figure 4.7 Artwork of moat lines exposing Kovar core to minimize impact of temperature induced bi-metallic bending.

the opposite direction, i.e. "closed-up" the artwork in the post-processing activity described later in Section 2.4.5.

Photographs of the relief sides of two masks are shown in Figures 4.5 and 4.6 which demonstrate respectively near-perfect and over-etching situations. Both masks, however, have been successfully used in the vaccum system.

One final and novel feature of the new mask design is the provision of so-called 'moat' lines on the defining side surface of the mask. The idea here was to minimize temperature-induced bimetallic bending of the masks by isolating, as far as possible, various regions of the nickel top plate. The moats simply exposed lines of bare Kovar core between the defining side aperture pattern. An example of this is shown in Figure 4.7.

#### 4.3 Pattern Design Considerations

The distinction between the concepts of mask design and pattern design was described previously. In review, mask design concerns itself with the physical constitution of the vaccum system stencil masks, the materials used in their construction, and their features otherwise common to all masks of a particular set. Pattern design, the subject of the present section, deals with the aperture patterns which generally differ from one mask to another within a set.

The object of pattern design is initially to provide a digitized data base from which pattern generator instructions can be readily derived to flash photoplates for use in mask construction as described in the previous section, e.g., as shown in Figure 4.3C. The ultimate object is to ensure that sequential depositions through the masks so constructed synthesize correctly a thin-film pattern previously determined adequate to drive a phosphor dot matrix constituting the display.

Basically, there are six inputs which impact the pattern design process. These are:

- 1) the mask fabrication process
- 2) mask handling/usage procedures

- 3) equipment to be used for digitization and pattern generation
- 4) electrical and electronic integrity ("layout") of the thin-film pattern
- 5) testability of the thin-film pattern so fabricated
- 6) repairability of the thin-film pattern.

The ultimate objective of the exercise is to integrate all the considerations in a way that the eventual thin-film pattern can be synthesized with as few different masks and as few process steps with as few materials as possible. Although each item listed above cannot be considered exclusive of the others, the following discussion adheres to the classification listed for the purpose of clarity of exposition.

Constraints imposed by the mask design fall into five categories:

- Minimum aperture size
- Aperture shape
- Aperture aspect ratio
- Minimum aperture separation
- Aperture density

First of all, factors limiting any aperture section to values above  $20\mu$  may be understood with reference back to Figure 4.3E. Here we observe the nickel plating encroaching over the defining side patterned photoresist. Though, in principle, it should be possible to separate approaching edges of the plating to an arbitrarily small distance, in practice, the plating becomes difficult to control when the specified aperture is  $20\mu$  or less.

Secondly, the only aperture shape we have been able to operate with successfully, is the rectangle. L-shaped apertures, for example, provide very unreliable masking at the inside projecting corners due to mechanical weakness and present special problems during mask cleaning operations. It is possible that trinagular-shaped apertures or other geometrical oddities might behave as well as rectangles, but there are

two main reasons why they are not used. First, we have never developed any artwork in which they would offer significant advantage, and secondly, they present special digitization and pattern generation problems.

The third mask design constraint concerns aspect ratio. Whereas there certainly exists some upper limit on the size of an aperture which can be made, we have never had cause to consider situations in which any aperture is both high and wide.\* On the other hand, in the deposition of bus-bars, for example, one needs pattern segments that are long and narrow. For reasons not entirely well understood, it is generally found that the wider the narrower side, the longer one can make the longer side; hence, the upper size limitation is usually described in terms of aspect ratio. In the present pattern the narrowest apertures are  $50\mu$  wide. An aspect ratio of about 10:1 is considered the maximum allowable, although we typically work within a 7:1 limit.

The minimum aperture separation limit is a direct consequence of the mask fabrication technique described in Figure 4.3E and applies, in this case, to the source-drain gap. Here one would ideally like to have the gap as narrow as possible from the point of view of optimizing the transistor electronic operating characteristics. In practice, one is again limited by requirements imposed by the generation of the defining side pattern definition, shown again in Figure 4.8. Here we have the cross section of the source and drain apertures separated by the so-called source-drain "bridge". The real limiting factor is the minimum dimension of gold plating exposed between the respective photoresist islands which can provide a sufficiently reliable geometry for the initiation and growth of the nickel plating. If the gap between the photoresist islands is much less than  $10\mu$ , the nickel plating sometimes fails to "take". Since the nickel typically encroaches over the photoresist extremities to the extent of about  $15\mu$ , one cannot meaningfully specify final bridge widths and hence source-drain gaps less than  $40\mu$ .

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\*The largest apertures we use generate the contact fingers and phosphor pads and these are well within the limits of the technology.

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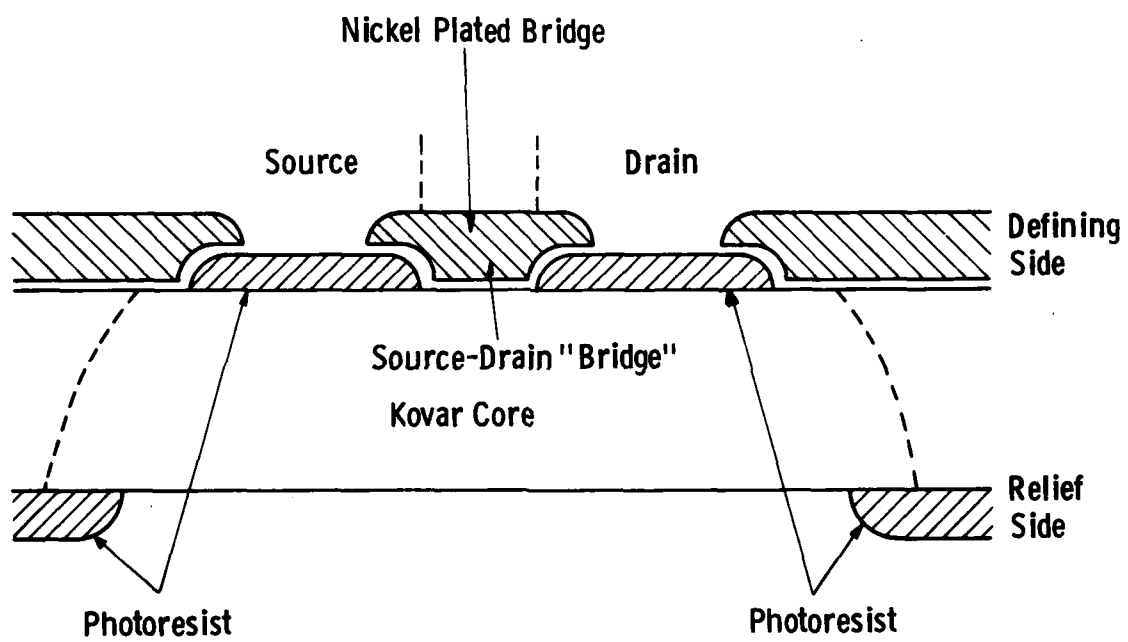


Figure 4.8 Factors limiting minimum aperture separation.  
(Refer also to Figure 4.3E).

An additional feature of interest in Figure 4.8 is the non-matching of the defining and relief side photoplates. What would be the relief side source and drain apertures have been merged to provide a single opening for etching of the entire core between the broken lines in Figure 4.8. The bridge is said to be "without reinforcement". This technique has been applied extensively to certain masks of the new set, wherein groups of apertures, typically those responsible for generating a particular character location in the display, are entirely defined by a so-called defining side nickel "skin".

The final constraint on pattern design imposed by mask design concerns aperture density. Here one must consider the issue of "mask mechanical integrity", that is, a situation in which masks are either locally or universally so "lacy" that they cannot be handled without physical damage or geometric distortion. There exist no numerical specifications to nail down the "do's" and "don'ts" of this issue. It is rather a question of intuition and experience. Generally, one tries to avoid situations in which Kovar core reinforcements are discontinuous anywhere across the mask. In other words, the Kovar reinforcement should be generally grid-like and in which lateral protrusions and indentations are permissible. Figure 4.9 illustrates the extremes of acceptable and non-acceptable designs.

Mask handling and usage procedures constitute another broad class of considerations entering into pattern design. From the circuit fabrication viewpoint, the mask count within a set should be minimized and the masks should be as thin and flexible as possible. This calls for very fragile structures with very dense aperture packing. However, the masks have to be handled for cleaning, inspection, and installation. In the tradeoff, pattern segments which could, in principle, be deposited through a single mask have, therefore, to be often distributed across two or more separate masks.

Next, the equipment used for digitization and pattern generation must be considered. There are basically two reasons why the DMD device being made in this program is assembled from two half-panels instead



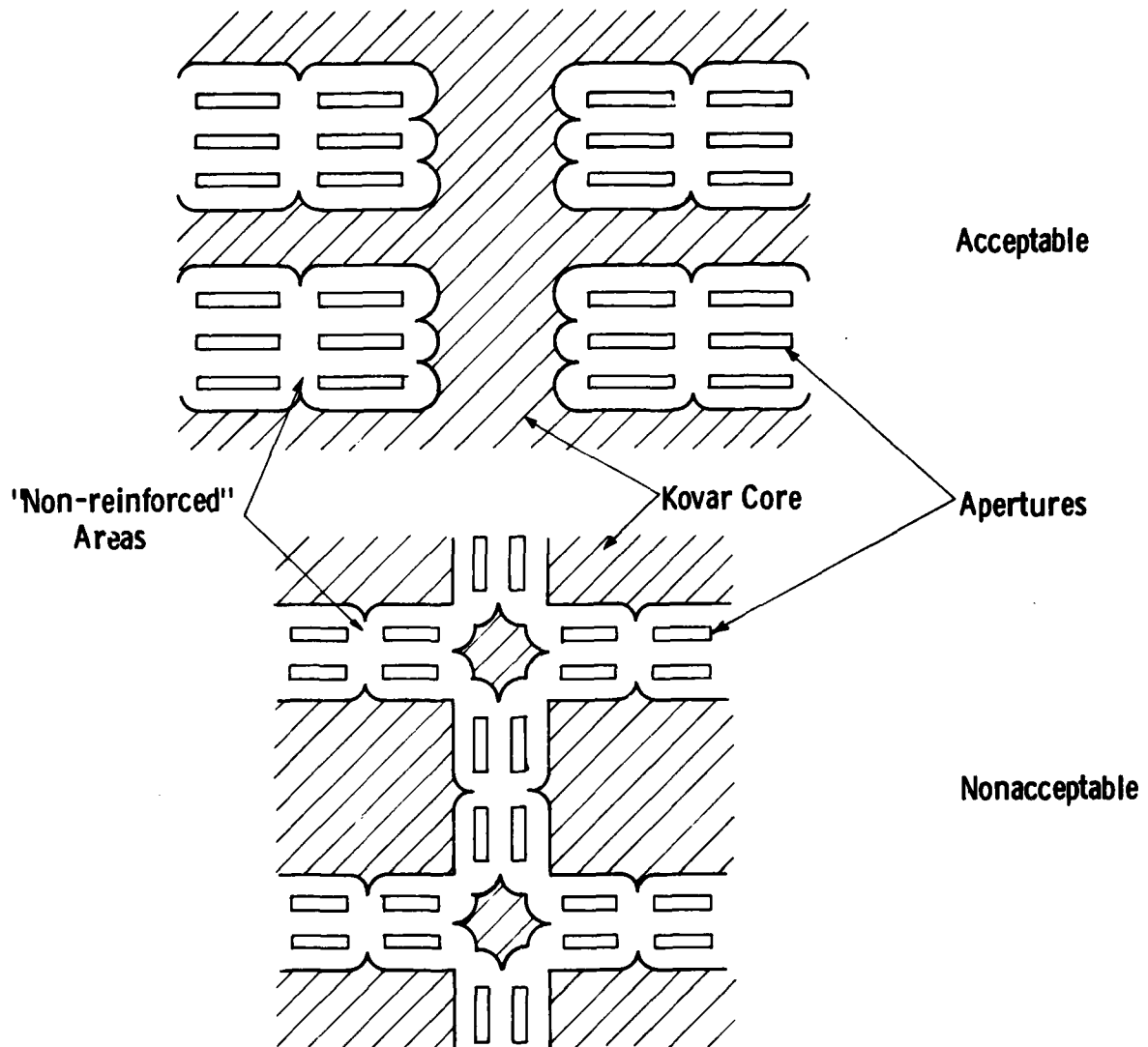


Figure 4.9 Extremes of acceptable and non-acceptable Kovar core reinforcement patterns. In both cases, certain groups of apertures are defined entirely on a defining side nickel "skin".

of a single composite structure. One relates to the vacuum system hardware being used, which itself was not designed to accommodate the full 4" x 7" substrate. Equally important, however, is the equipment available for digitization and pattern generation. The Applicon system which was used for pattern digitization could only accommodate 10 cm x 10 cm drawings at the required level of 5 $\mu$  pattern definition. Likewise, the only readily available pattern generator, when this work began, was a Mann 1600 unit which further limited the pattern area to a 10 cm x 10 cm.

The major traditional consideration concerning pattern design is transposing the electronic schematic to an artwork layout. Since the electrical and electronic properties of the circuit have been discussed extensively in previous quarterly reports, only those features related directly to the change from the "old" design to the "new" design will be considered here.

In Section 1, we disclosed five general purposes of the mask and pattern redesign task. Two of those bear strongly on the pattern itself; for the sake of review, these two are listed below:

- Reduce mask count from 12 to 9 or less;
- Relieve the mask inspection burden through a geometrically less complex pattern.

These purposes were not served by unilateral consideration of the mask and pattern designs alone. The vacuum deposition process itself had to be reformulated. Nonetheless, the essence of what we were really looking for here was replacement of the old two-mask, five-aperture-per-pixel insulator mask subsystem by a single mask, single-aperture-per-pixel alternative. This would offer advantages not only in circuit fabrication but in mask inspection and cleaning. A single large aperture, for example, is mechanically more sturdy and easy to clean and inspect than five smaller ones on two different masks. For much the same sort of reason we sought to reduce pattern complexity by changing it from a graphics to an alphanumeric format. This was to reduce the pixel count from 8547 to 4480

per half-panel. Together with the simplification of the insulator pattern, the resulting total insulator aperture count was reducible from approximately 43,000 to less than 5000 per mask set! Although not all apertures of the former graphics format were actually functional in the resulting thin-film pattern, they all had to be cleaned and inspected since there was no readily available way of distinguishing functional apertures from non-functional ones.

In summary, considerations of circuit layout focusses on insulator mask aperture simplification and reformatting the display. The purpose was to reduce the mask count not only by eliminating one of the previously used pair of insulator masks but by the circuit pattern redesign, which was to embody any other geometrical simplifications which might be realized by fabricating the circuits with fewer than the five different metals which had historically been used in circuit fabrication.

As indicated at the beginning of this section, the pattern was to encompass a feature entirely absent from the old design. This was related to circuit testability. The whole issue of circuit testing and testability has become somewhat complex and is covered extensively in section 5. Meanwhile, suffice it to say that the "old" design embodied no special provisions to facilitate circuit evaluation prior to phosphor application and encapsulation. A gallant attempt to comprehensively appraise multiple properties of the circuit with a sophisticated automatic tester had not produced anticipated results because to a certain extent the layout could not expeditiously accomodate it. In the redesign effort we recognized we needed special features in the circuit to facilitate testing, whether it was done automatically or otherwise. Major consideration was therefore given to providing such features. These and all other aspects of the thin-film layout are discussed in the next section.

#### 4.4 Circuit and Mask Layout

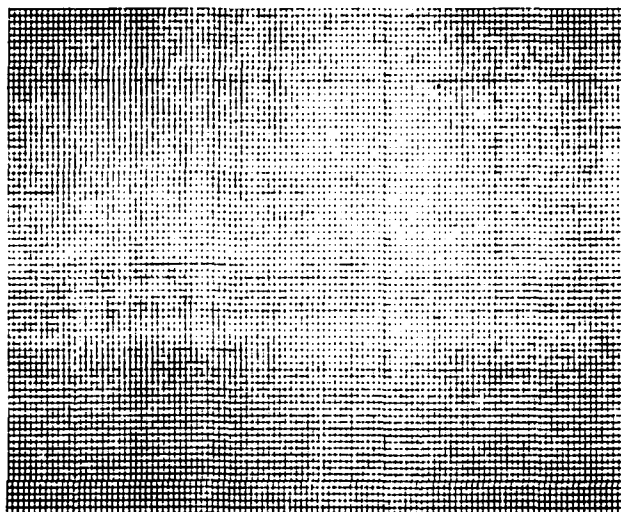
The actual artwork layout and digitization subtask began after the mask design and fabrication technique, described here in Section 4.3 had been firmed up and a variety of other considerations, such as those discussed in Section 4.3, had been weighed. In operations such as this, the dimensional constraints imposed by device requirements such as the geometry of the pixel array are compiled. A decision is then made on the graphics system to be used and the gross features of the data base representing the drawing. Next, the general approach to the circuit deposition sequence is determined. Artwork digitization begins with laying out a basic cell corresponding to the pixel and the circuit element driving each phosphor dot. Finally, the complete drawing is assembled in the data base, including supplementary features such as contact pad arrangement, test device distribution and so on. The discussion which now follows describes how the new layout evolved through these five phases respectively.

Essential geometric features of each half panel as called for by the original contract language are shown in Figure 4.10.

One of the consequences of selecting the graphics computer-- a readily available Applicon System here at Westinghouse R&D Center-- was that all pattern dimensioning had to be approximated in metric units. Table 4.1 compares the pertinent display geometry specified by contract with the matrix approximations we have actually used with the old and new designs. In all cases, the "actually used" numbers conform to the ranges permitted.

The data in Table 4.1 describing the 11t dot size indicates that we have been able to increase this by about 20% in area. Both versions conveniently feature "round number" dimensions in metric units. Other gross dimensions of the artwork pertaining directly to mask construction are shown in Figure 4.11.

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Required:  
77 rows over  
2.9"  
(37.7 mil  
or 957.8  $\mu$ /line)

Required:  
111 columns over  
3.3"  
(29.7 mil or  
755  $\mu$  per column)

Figure 4.10 Nominal display format specified by contract requirements.

Table 4.1 COMPARISON OF CONTRACT SPECIFIED SIZE REQUIREMENTS OF  
HALF-DISPLAY WITH METRIC APPROXIMATIONS ACTUALLY USED  
IN THE OLD AND NEW DESIGNS.

	<u>Horizontally</u>	<u>Vertically</u>
Number pixels accommodated	111 columns	77 rows
Display Dimensions:		
Contract	3.3 ± .03"	2.9 ± .05"
Actual	~ 3.28"	~ 2.88"
Lit Dot Size:		
Contract	>21 mil	>15 mil
Actual (Old)	21.6 mil (550μ)	15.7 mil (400μ)
Actual (New)	23.6 mil (600μ)	17.7 mil (450μ)
Overall Cell Size:		
Contract	29.7 mil	37.7 mil
Actual (Old & New)	29.5 mil (750μ)	37.4 mil (950μ)

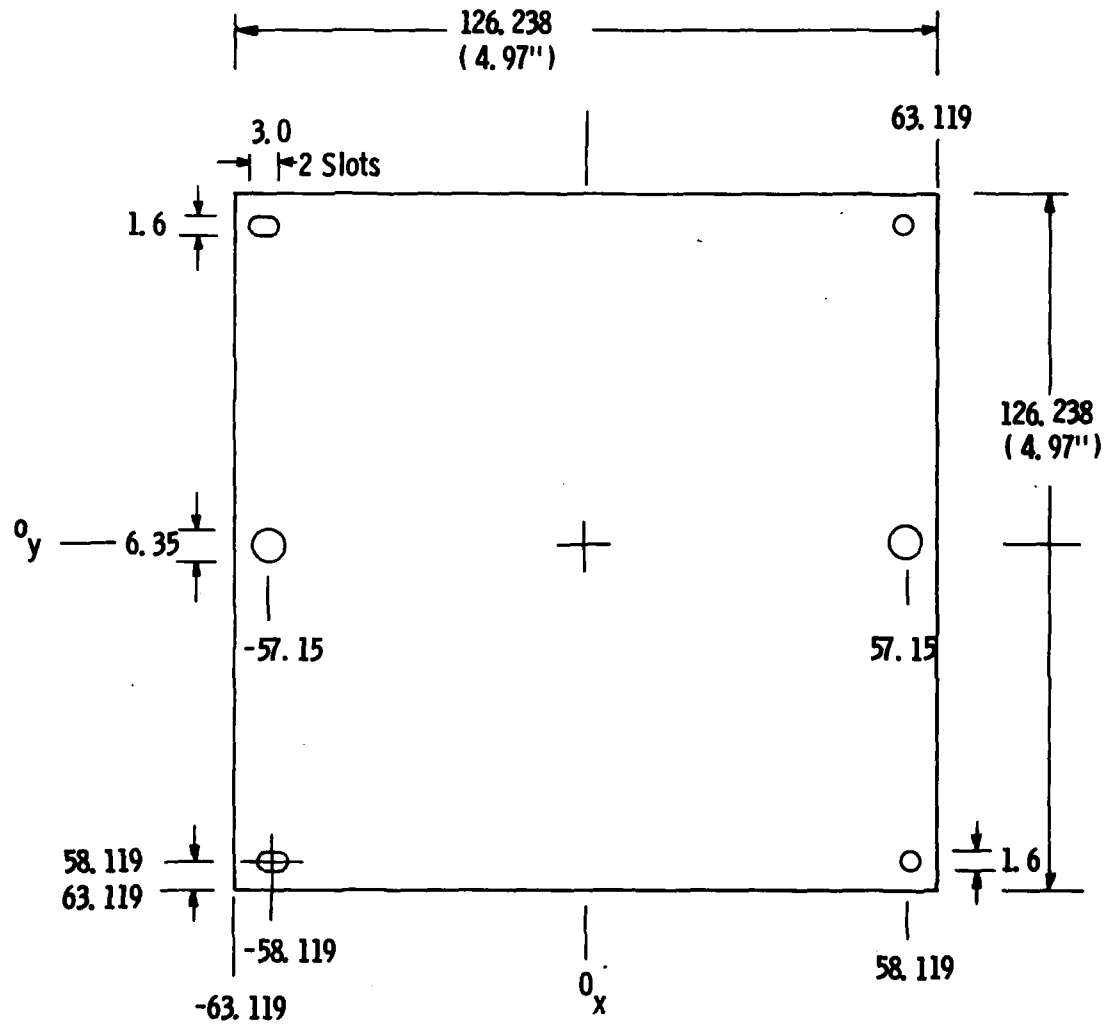


Figure 4.11 Dimensions relative to mask construction and vacuum system installation.

The overall size of each mask is  $126.238 \times 126.238 \text{ mm}^2$ . The holes in each corner are designed specifically to later facilitate re-alignment on the mask holder. The two larger circular holes on the X-axis accomodate the locating pins of the mask holder.

The dimensional data so far assembled are next transferred to the Applicon Graphics System. Subsequent discussion necessarily uses certain jargon associated with the software.

In principle, the Applicon "drawing table" measures approximately  $32,000 \times 32,000$  units. Assigning each basic grid unit a scale of  $5\mu$  uses about  $20,000 \times 20,000$  of these for the mask artwork and meshes nicely with the requirements for generation of metric Mann tapes from the data base. As far as the drawing is concerned, it means the operator can specify any dimension to an integral multiple of  $5\mu$ , although the Mann 1600 can only flash apertures in  $5\mu$  increments starting from  $10\mu$ . These mask design features are transferred to all of the twelve Applicon drawing levels, each of which is reserved exclusively for a particular pattern level.

At this point, a new conceptual approach to the synthesis of the thin film pattern was developed. After much discussion, we envisaged the deposited circuit films in cross section as the five-layer grouping shown in Figure 4.12. The outermost layers contain a complete set of horizontal bus-bars and the respective gates of the double-gated transistors. They also contain the vertical bus-bar segments not overlapping any of the horizontal bus-bar segments and the upper and lower (grounded) plates of the elemental three-layer capacitors. The segments of the vertical bus-bars forming crossovers with the horizontal bus bars are deposited in the central (active) layer group. The latter includes the transistor source, drain and semiconductor film segments and the central (active) layer group. The latter includes the transistor source, drain and semiconductor film segments and the central "hot" plate of the elemental capacitors. Since the insulator layers electrically isolate the active layers from the interconnect and gate layers, one must also "bridge" the insulator layers in certain places, for example, the point



\* Vapor Sources

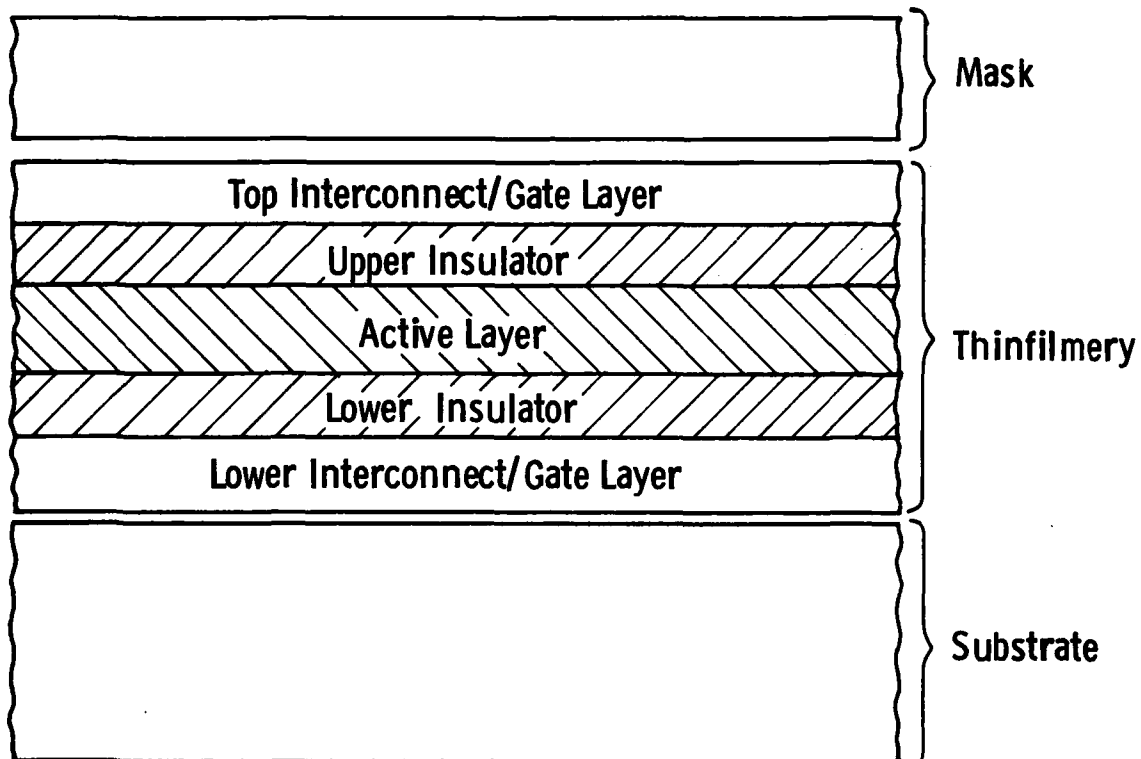


Figure 4.12 General conceptualization of thin film pattern cross section as five separate layer grouping.

of contact of the top and bottom gates of the power transistor (on the outer layers) to the center plate of the capacitor (on the active layer). For visualization, the elemental circuit roughly corresponding to the "old" pattern is shown in Figure 4.13. The outcome of considering several other factors, including a commitment to fabricate circuits with a single metal replacing the former aluminum and copper segments in the interconnect system, suggested that the total mask count could be reduced to 10 or 9 from 12 within the scope of the five layer concept if the previously vertical ground bus bars shown in Figure 4.13 could be run horizontally. This altered the bus bar visualization from that shown in Figure 4.13 to the one in Figure 4.14. Although this approach increased the bus bar crossover count per pixel by 33%, as indicated in Table 4.2, it was accepted because it offered the opportunity to reduce the mask count from 12 to 10 at most. Most importantly, it presented a way of eliminating one of the two bothersome insulator masks altogether and rendering the remaining one mechanically sturdy, cleanable, and readily inspectable. This was determined to be a major purpose of the entire task as explained previously in Section 4.2. The potential disadvantage of increasing the bus bar short defect yield was also offset partially by the fact that source-to-ground voltage stress is typically about half that of the gate-to-ground figure in typical panel operation

Table 4.2      COMPARISON OF BUS BAR CROSSOVER COUNTS PER PIXEL BETWEEN  
THE NEW AND OLD PATTERN DESIGNS (DERIVED FROM FIGURES  
4.13 and 4.14)

	<u>Source-Gate</u>	<u>Source-Ground</u>	<u>Gate-Ground</u>
Old Design	1	0	.5
New Design	1	1	0

When all the foregoing considerations and analyses had been completed, work started on the detailed segmentation of the thin-film pattern of the basic elemental pixel drive circuit. The only additional constraint was that the pattern should fit into the space allocated between the bus-bars with no less misregistration tolerance than the old pattern which

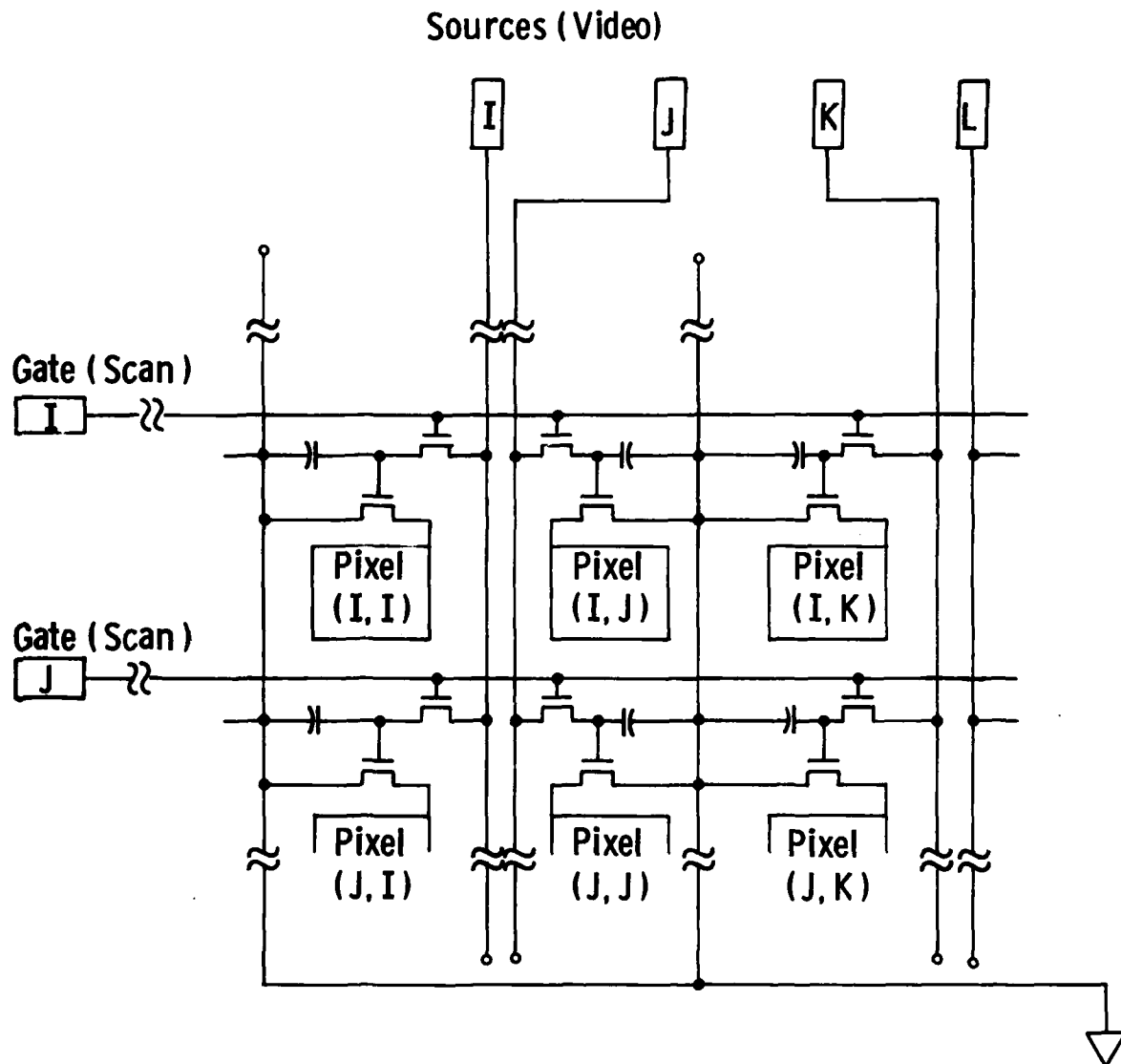


Figure 4.13 Bus-bar visualization for old layout.

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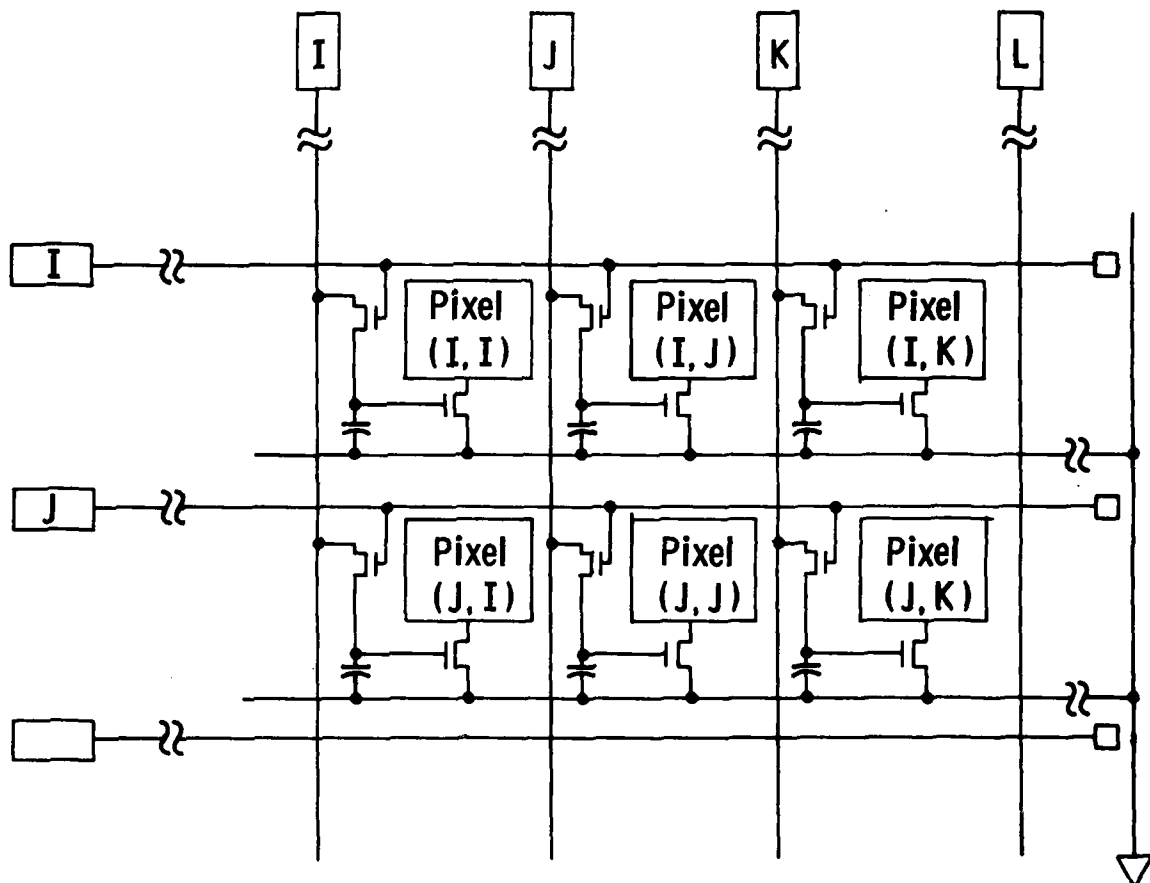


Figure 4.14 Bus-bar visualization for new layout.  
(See also Figure 7.1)

had been determined misregistration-proof as far as the capability the vacuum system hardware was concerned. We also sought to maintain the geometries of the two transistors and the materials used, since those made by the old pattern seemed quite capable of doing the task required of them.

After about forty hours work on the Applicon, the elemental circuit pattern was frozen in the form shown in Figure 4.15. Although this has since been reduced to a nine-mask pattern, its original ten component levels are shown in Figures 4.16 through 4.25. This series of diagrams portrays a 35-dot single character region to provide the reader with a clearer concept of how mask integrity considerations were honored. Essential information relating to the pattern components of the new design is given in the respective captions of Figures 4.16 through 4.25. All relative geometries in these figures describe the actual thin-film pattern and generally do not relate to the dimensions of flashes later to be made on the photoplate. These are described later in Section 4.5. A composite picture of all ten levels on a larger scale is shown in Figure 4.26 which also shows some very desirable features of the new design entirely absent from the old one. The principal ones are the location of a pair of test transistors at each character with easily accessible, oversize test pads. Their incorporation in the design was made possible by the commitment to fabricate only the required alpha-numeric features of the display. This was in no way a withdrawal from the previous position, because even the old artwork itself was incomplete as far as making a graphic display was concerned. Also shown in Figure 4.26 are strategically located test pads on the bus-bars. These later facilitated enormously the onerous task of locating critical bus-bar defects prior to repair, and were, likewise, made possible by taking full advantage of the commitment to a strictly alpha-numeric format.

Whereas the phosphor dot matrix driving circuit pattern is fairly well described by Figures 4.12 through 4.26, the artwork layout chore is not complete without additional features related to mask fabrication and alignment. The present section concludes with a description of four remaining facets of drawing digitization known as

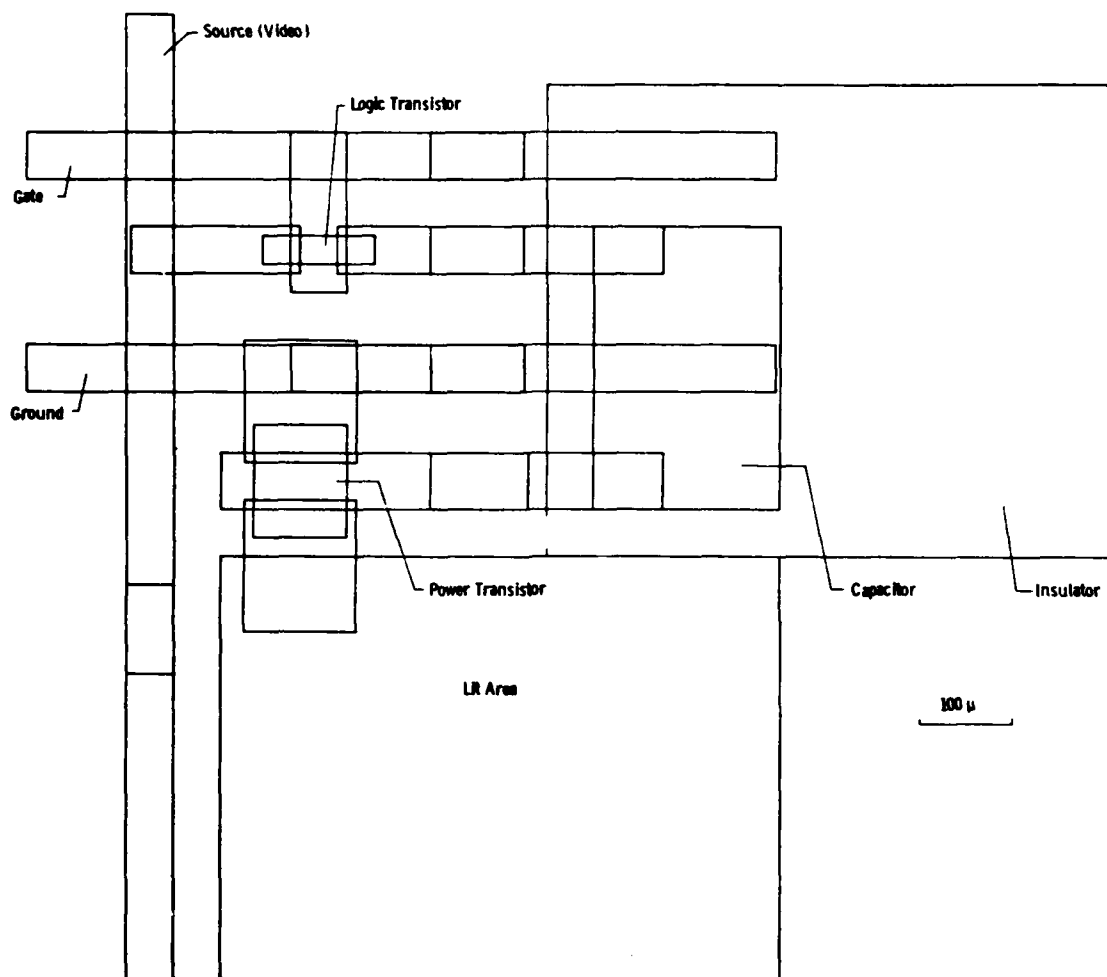


Figure 4.15 Artwork of the elemental circuit of the new design.

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MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY--ETC(U)

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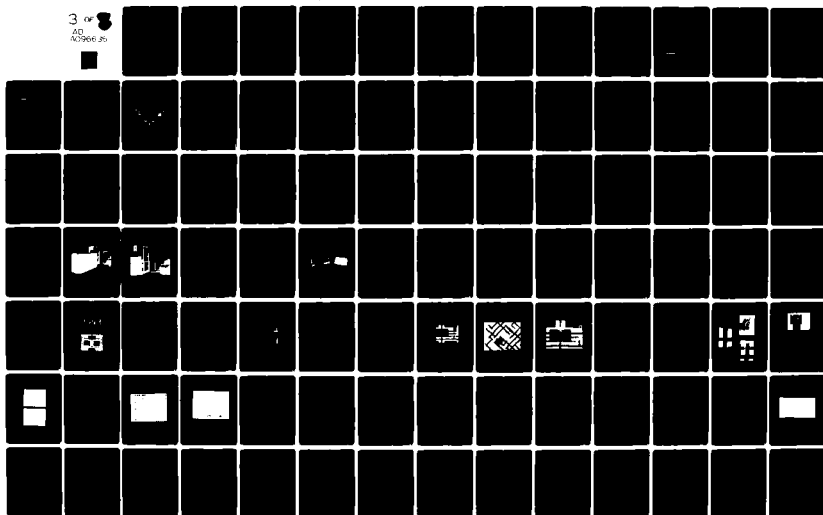
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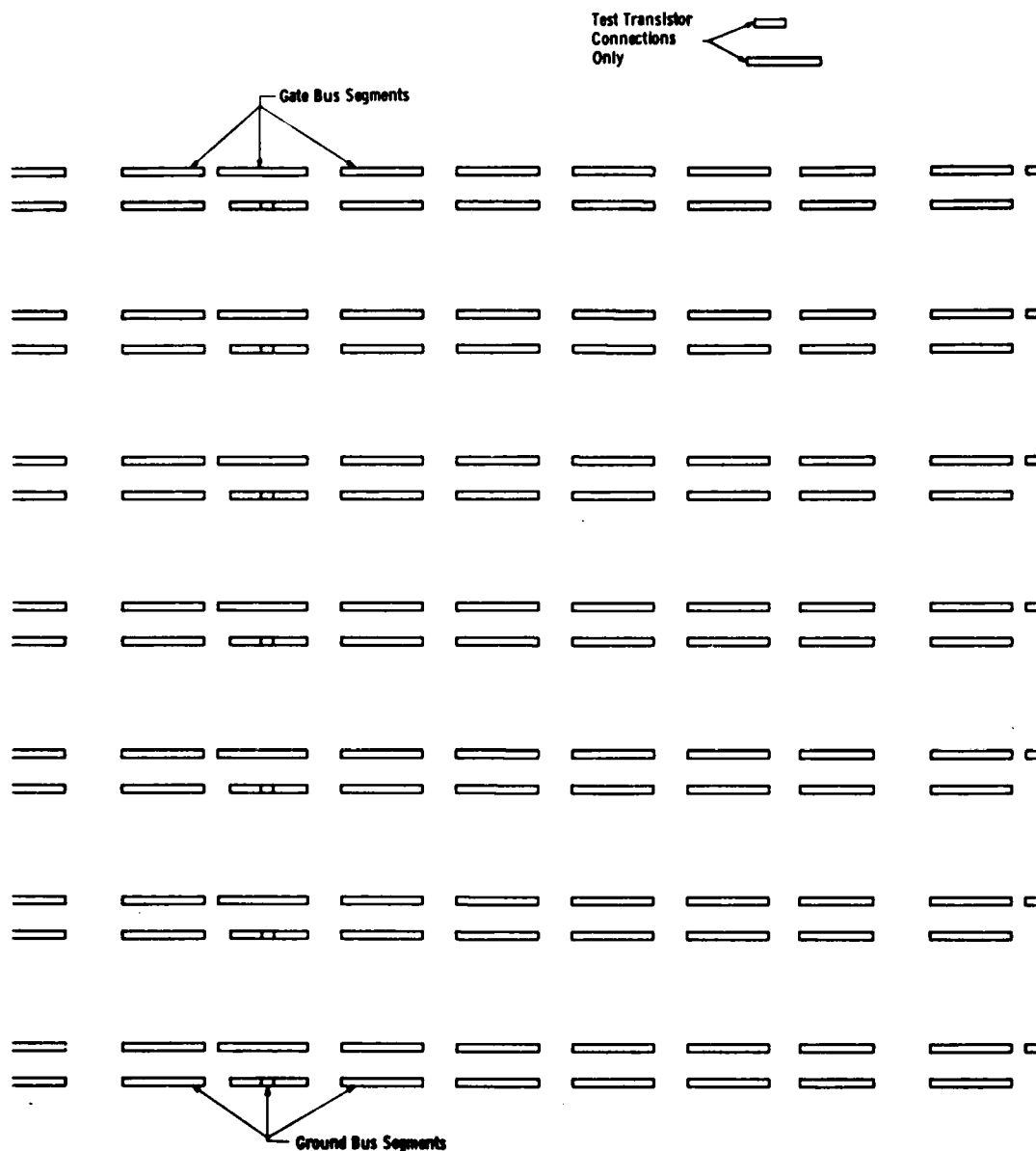


Figure 4.16 Level 1 of the new pattern; horizontal bus bar (gate & ground interconnect segments). Together with levels 2 and 3 (Figures 4.17 and 4.18), this constitutes each of the outermost gate and interconnect layers of the scheme shown in Figure 4.12.



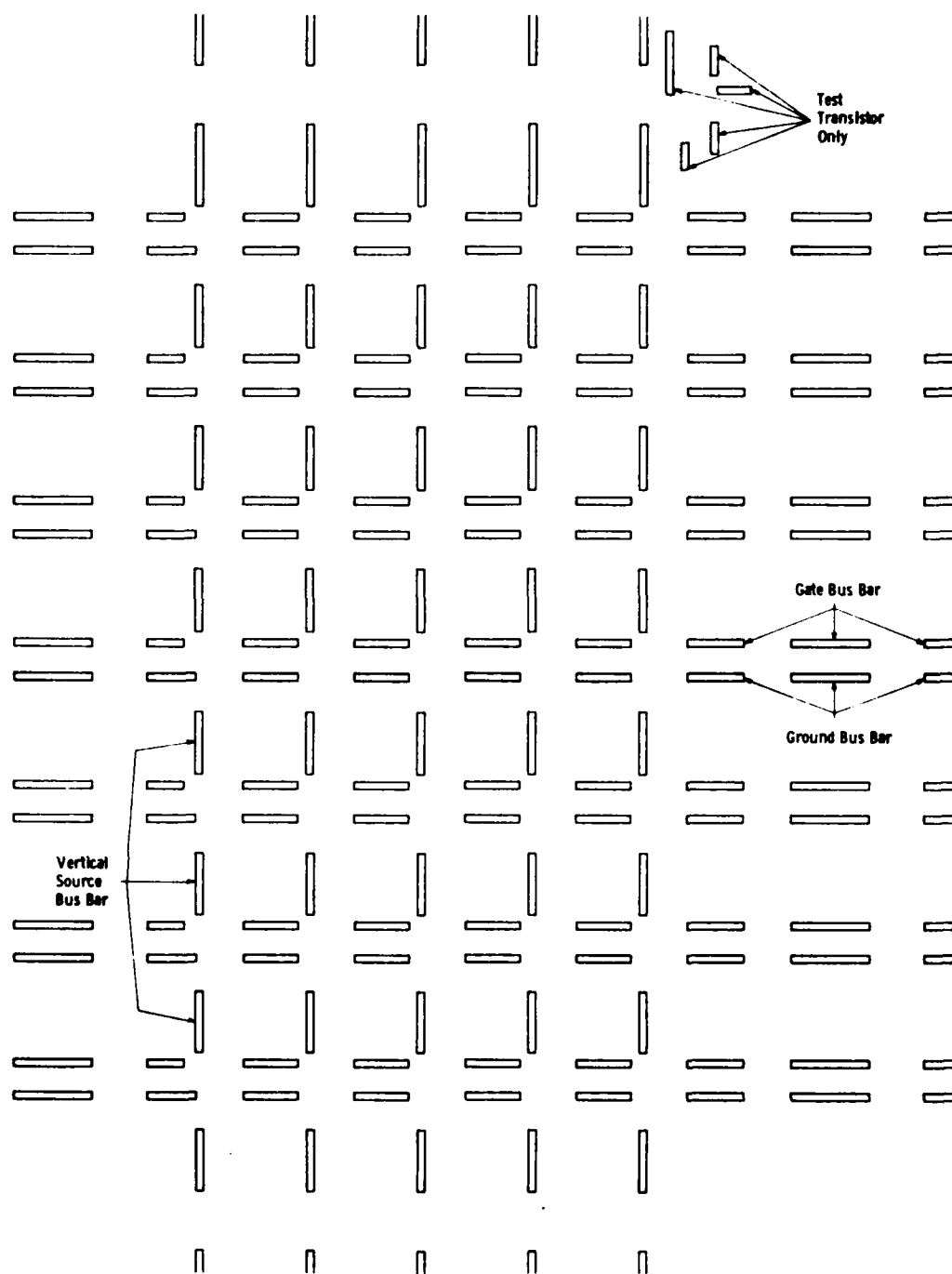


Figure 4.17 Level 2 of the new pattern; completes horizontal bus bar pattern and provides non-crossover segments of vertical bus bar pattern. Together with levels 1 and 3 forms the outermost layers shown in Figure 4.12.

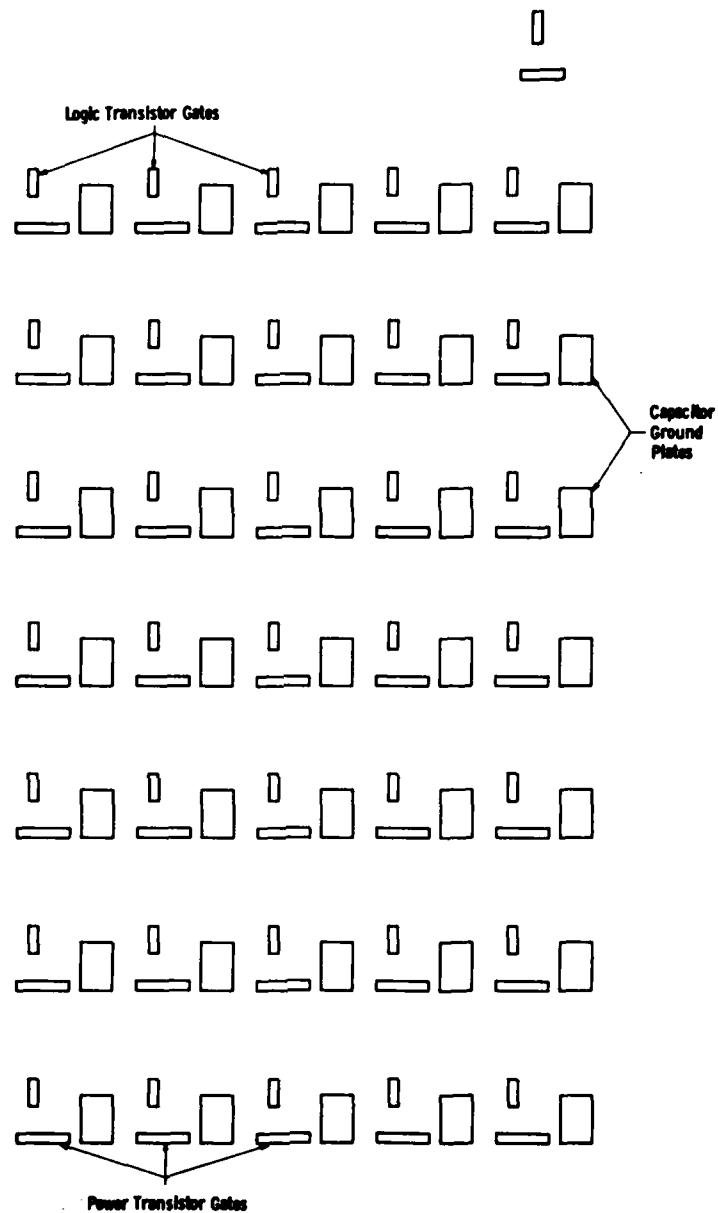


Figure 4.18 Level 3 of the new pattern; adds transistor gates and capacitor ground plates to levels 1 and 2 to complete outermost layers of scheme shown in Figure 4.12.

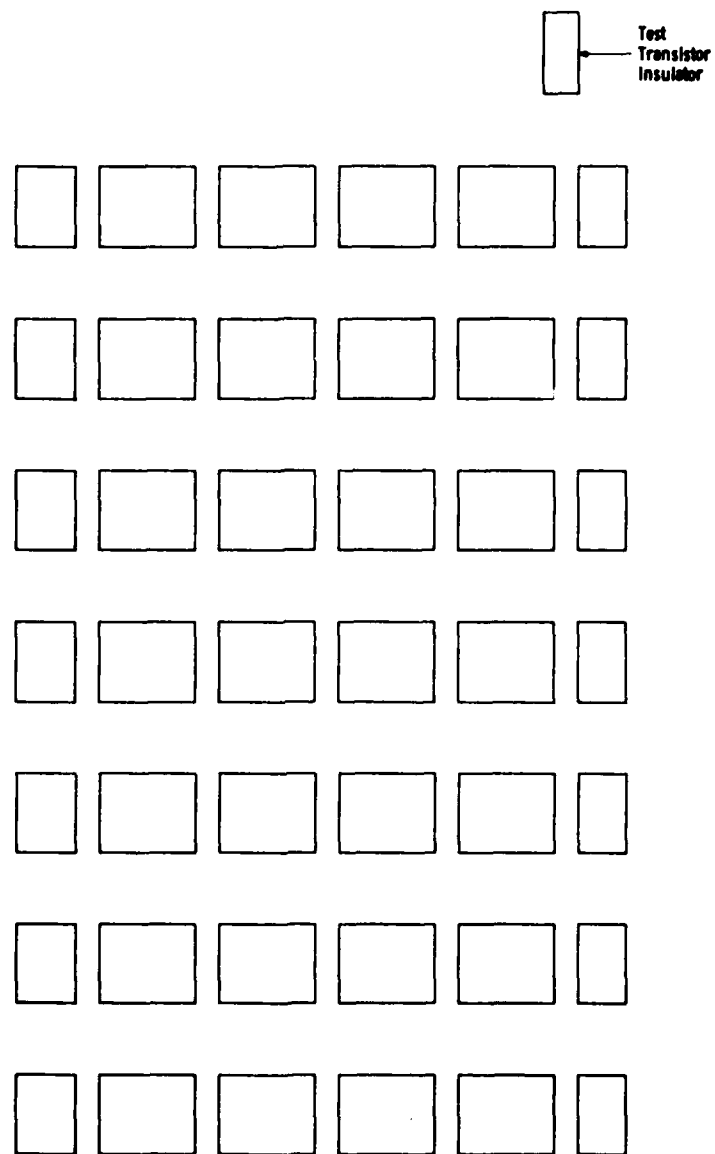


Figure 4.19 Insulator pattern on Level 4.

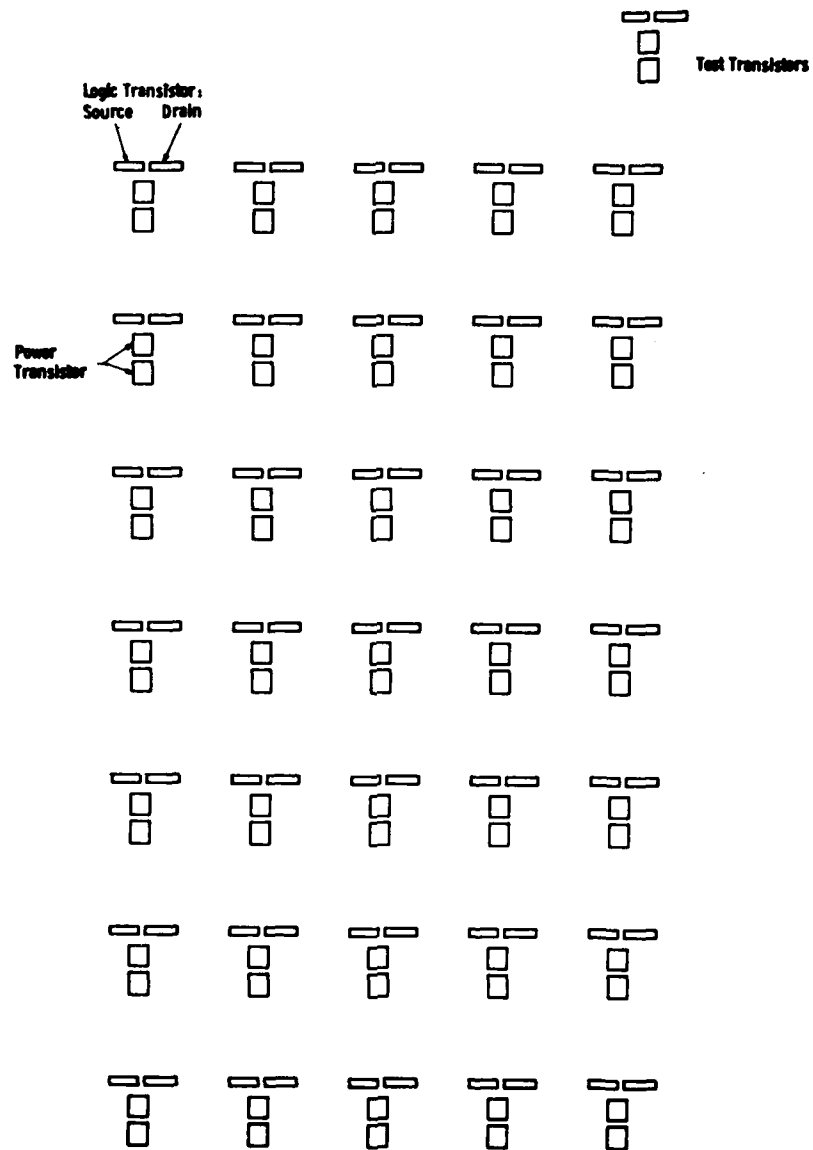


Figure 4.20 Gold source drain pattern on Level 5 of the new design; the first component of the "active layer" in Figure 4.12.

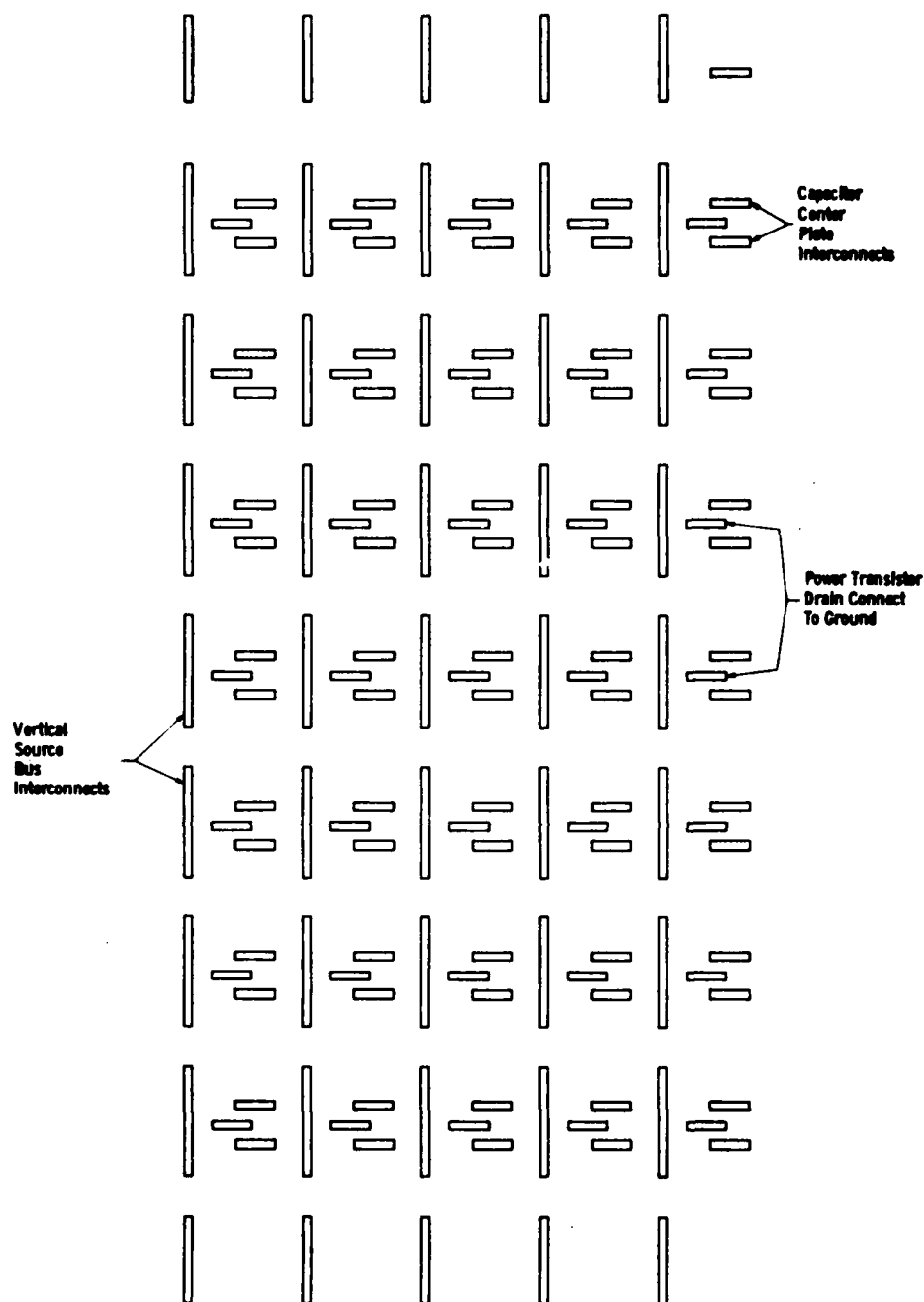


Figure 4.21 Level 6 of the new design; second component of the active layer in Figure 4.12. We had originally hoped, and later found it possible, to make these transistor and capacitor interconnects and vertical bus segments from nickel instead of copper as in the old design.

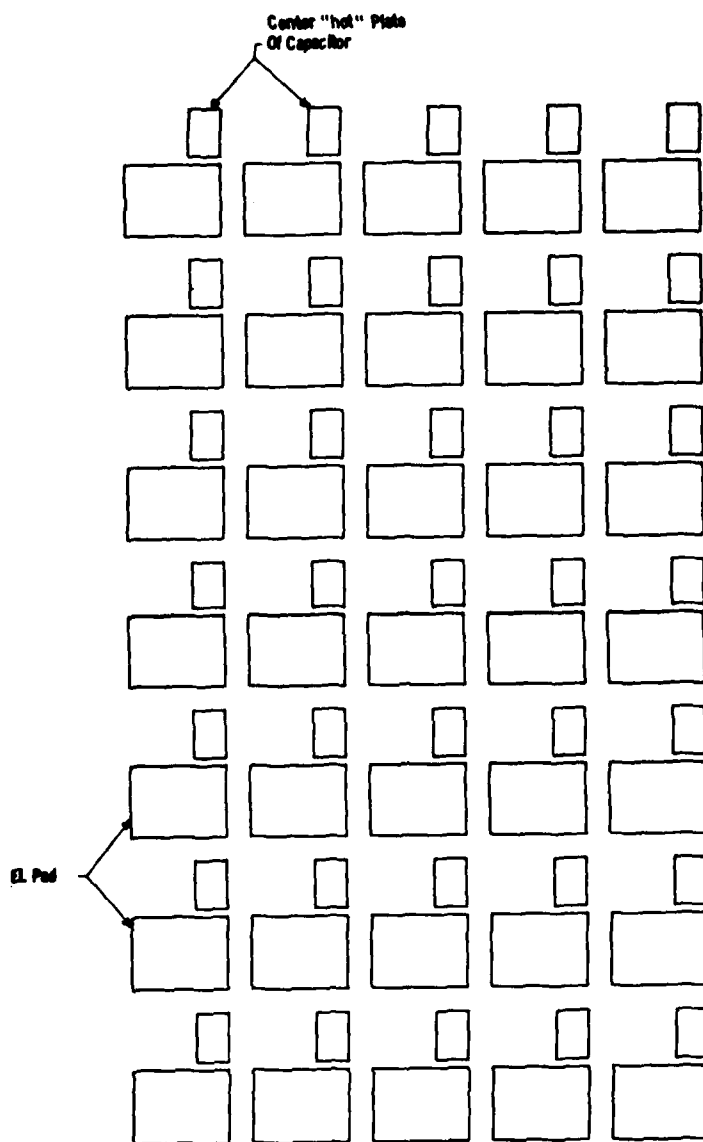


Figure 4.22 Level 7 of the new design; third component of the active layer of Figure 4.12 contributing the capacitor center "hot" plate providing essential electrical continuity from the logic transistor drain to the power transistor gate.

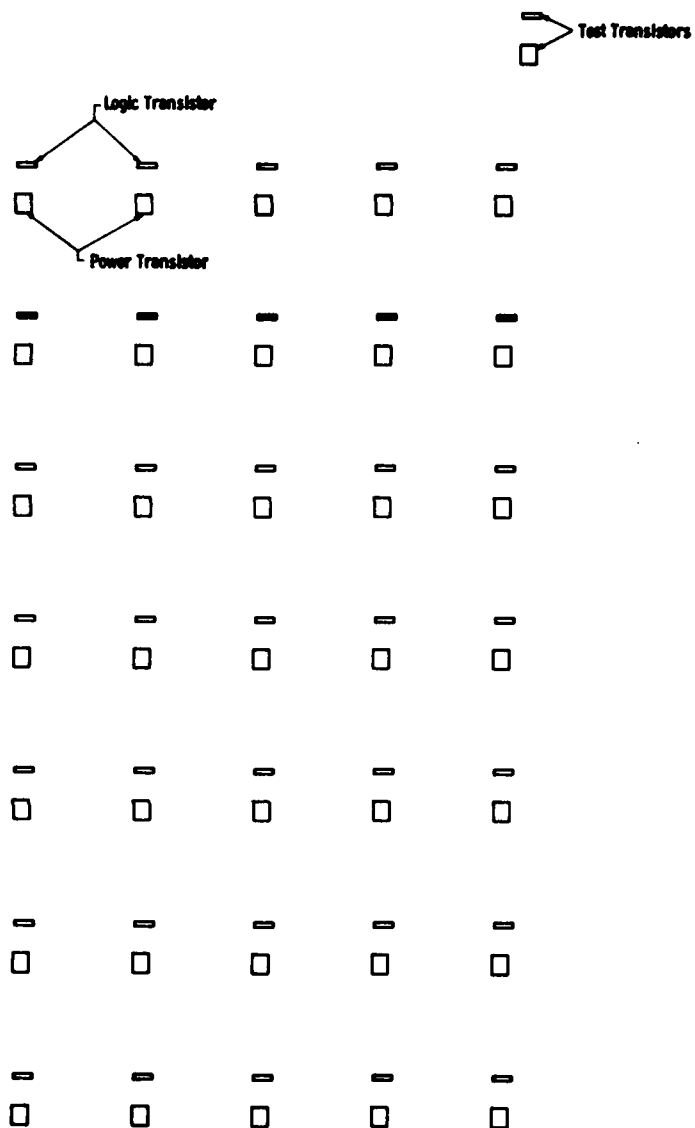


Figure 4.23 Level 8 of the new design; CdSe semiconductor for the logic and power transistors.

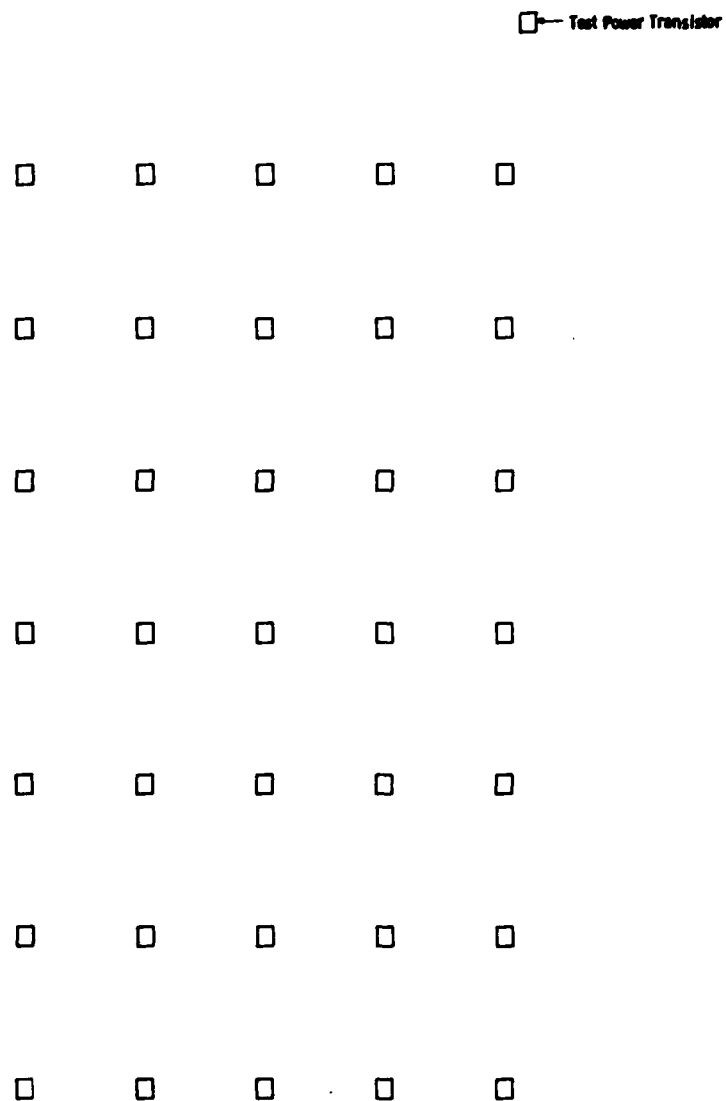


Figure 4.24 Level 9 of the new pattern design for differential doping of the power transistor. With Levels 5 through 8, this completes the active layer of Figure 4.12. (This was the mask we were later able to discard).



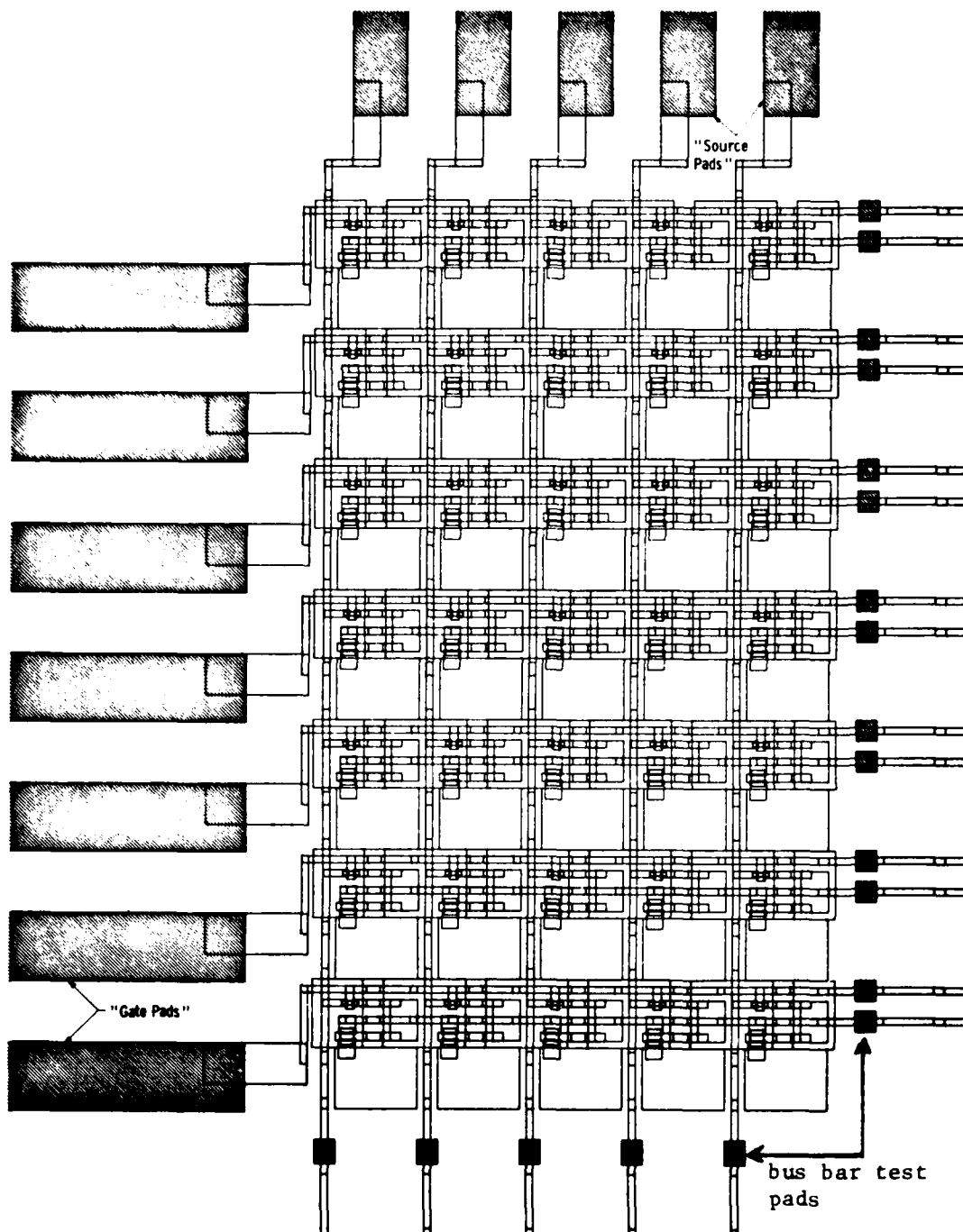


Figure 4.25 Level 10 of the new pattern on a larger scale contributing circuit contact pads only. This mask does not contribute to any of the layers shown in Figure 4.12.

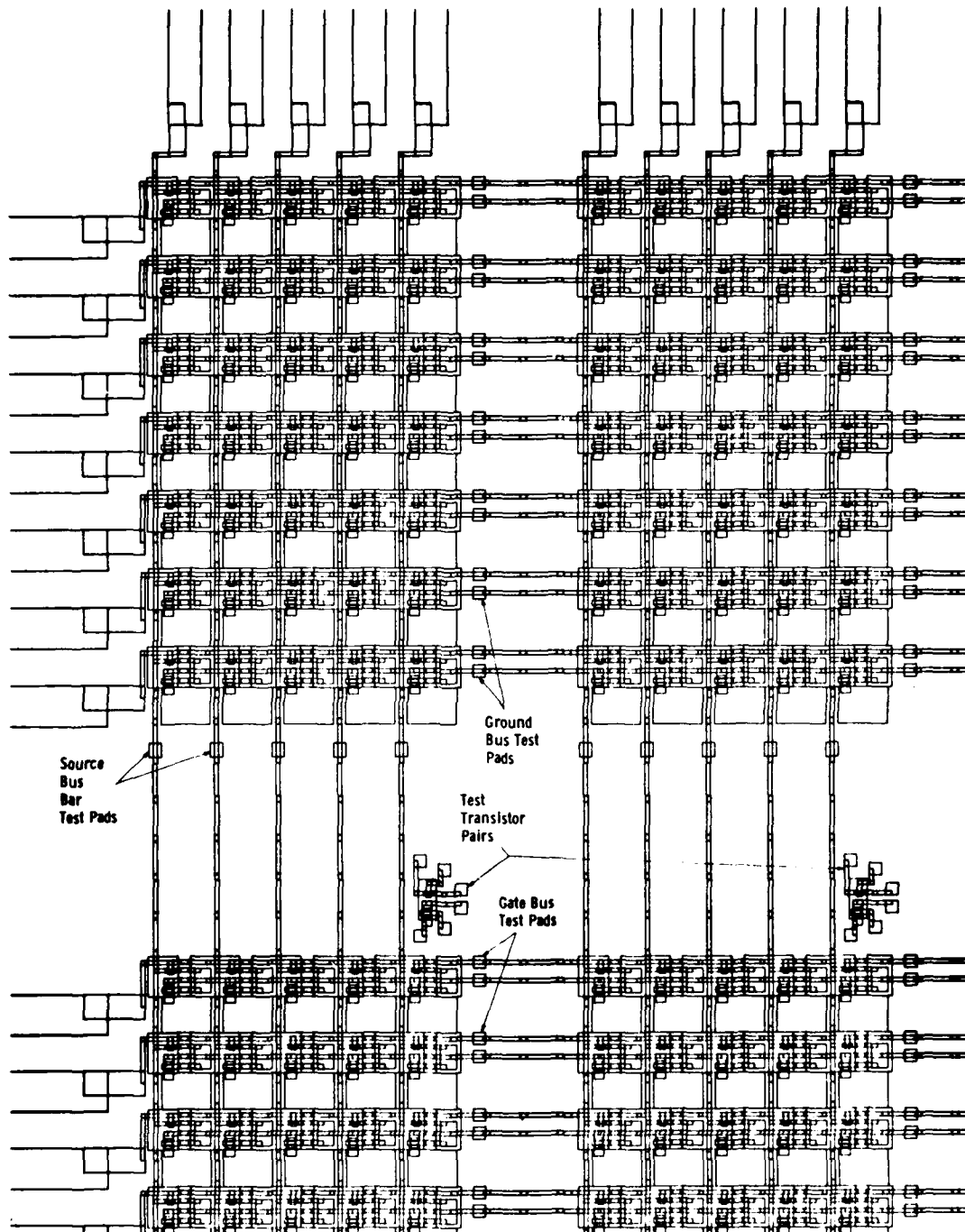


Figure 4.26 Composite pattern generated by superposition of levels 1 through 10 in Figures 4.16 through 4.25 illustrating strategically located test transistors and bus bar test pads.

- alignment squares
- targets
- nomenclature
- check squares

The purpose of the alignment squares is two-fold. They facilitate the alignment of each mask correctly on its respective mask holder and, in addition, provide a readily interpretable means of decoding any misregistration errors which might occur during the vacuum deposition of the thin film circuit. At each alignment square location indicated in Figure 4.27, an array of sixteen squares is incorporated into the data base as illustrated in Figure 4.26. Mask 1 (Figure 4.16) is fabricated with a set of apertures corresponding to all sixteen smaller squares illustrated in Figure 4.28. Thereafter, each mask has only one of the offset larger squares and the "keying" square. The use of this artifact is explained in later documentation.

The purpose of the targets is to facilitate assembly of the phototooling (Section 4.2) and are photoplate features not transformed into mask apertures. In Section 4.2 previously, we explained and phototooling requirements for defining side and relief side photoplates. These plates are carefully aligned face-to-face during phototool assembly. The purpose of the targets, illustrated in Figure 4.21, are to facilitate the operation. As indicated in the figure, the shaded areas are flashed on to the defining side photoplate and the clear areas on to the relief side plate.

For the important purpose of finished mask identification, each different one is assigned alphanumeric artwork disclosing essential information. This results in inscriptions indented on the finished mask (by absence of nickel plating) as listed in Figure 4.30.

Finally, a so-called "check square" pattern is inscribed on all photoplates as indicated in the lower right portion of Figure 4.27. The format of the sub-pattern is shown in Figure 4.28. Its purpose relates to photoplate preparation and is described in the next section.

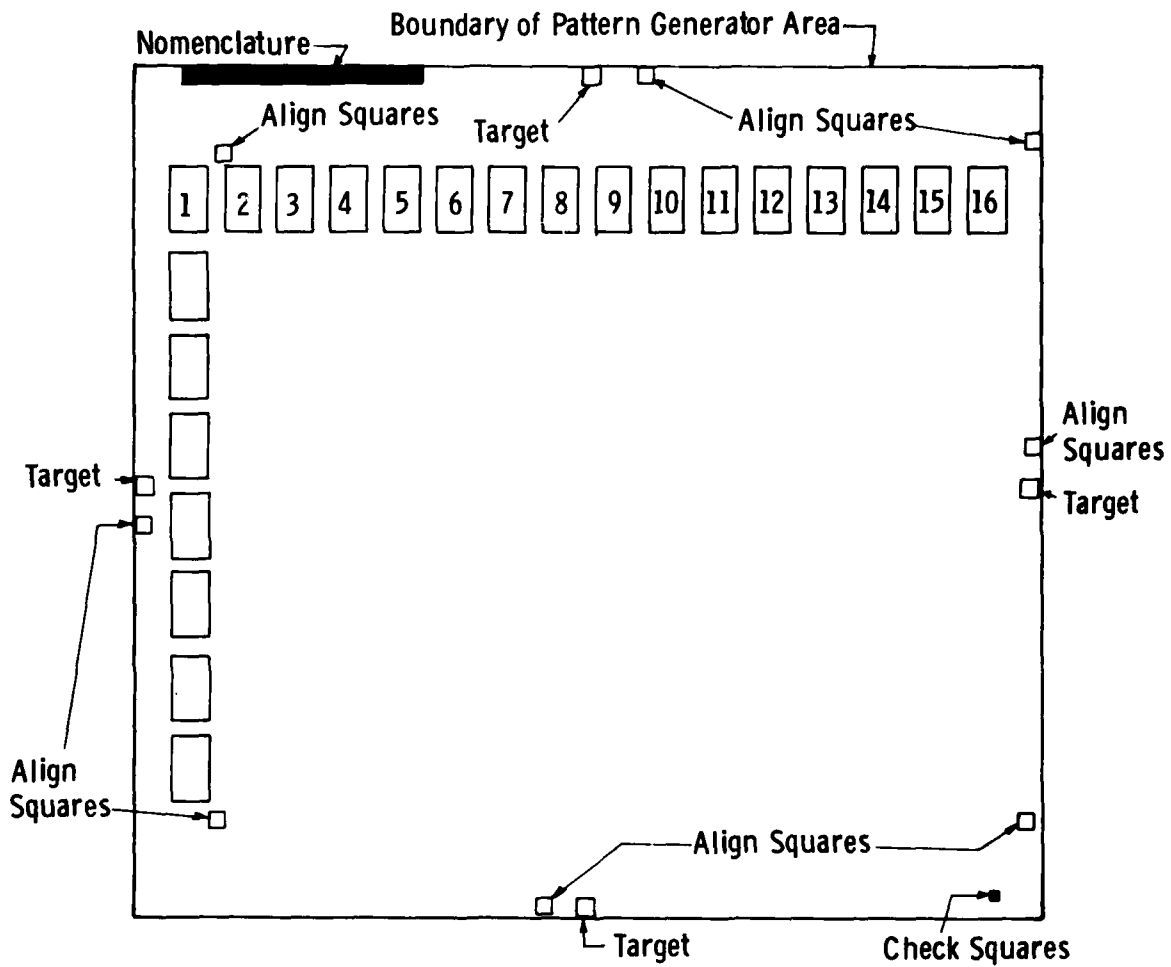


Figure 4.27 Location of targets, alignment squares, check squares and nomenclature relative to thin film circuit artwork of the drawing.

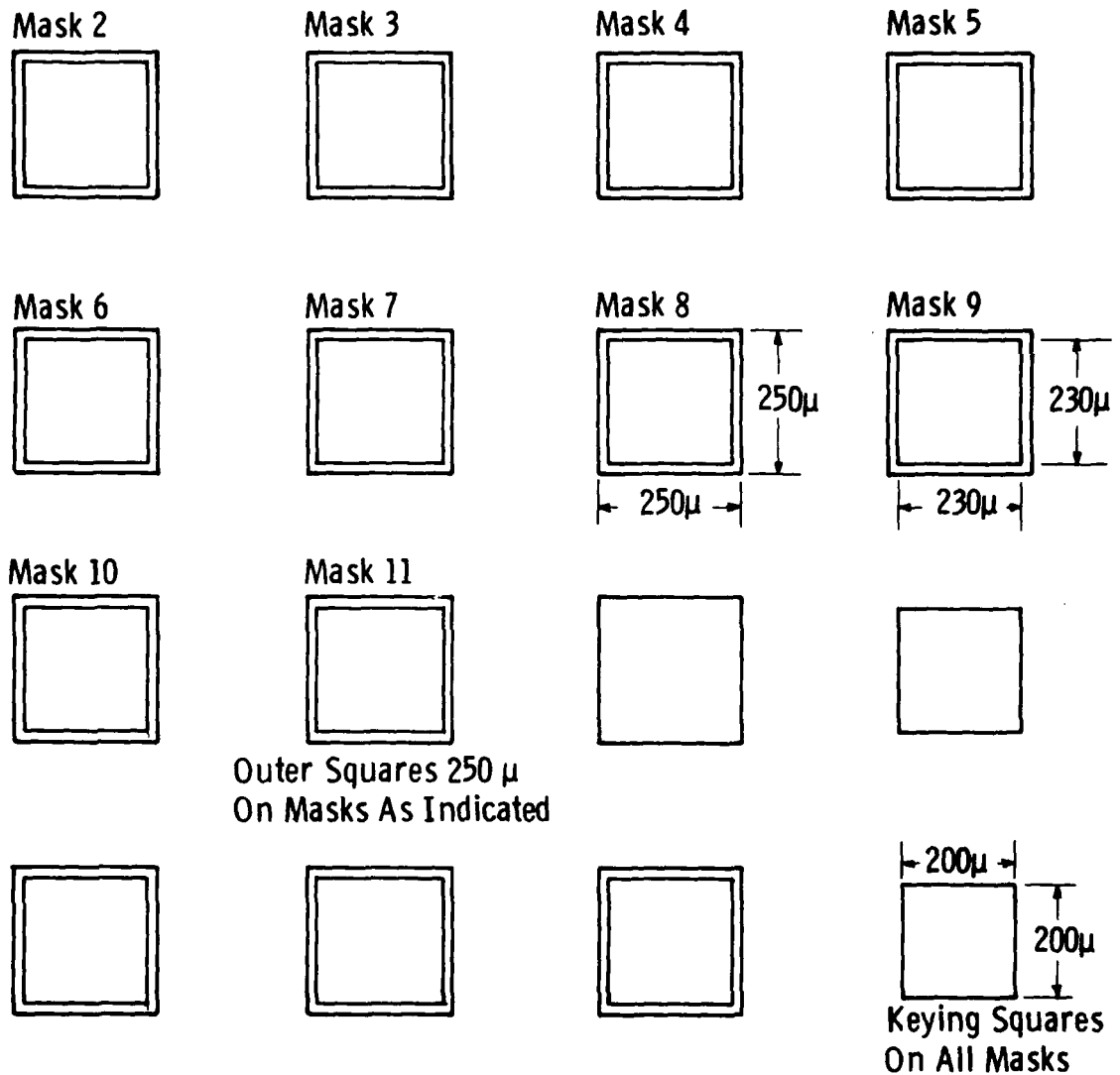


Figure 4.28 The alignment square array incorporated into the artwork at locations shown in Figure 4.18 for the purpose of expediting mask alignment and later for checking in-process mask-to-substrate registration.

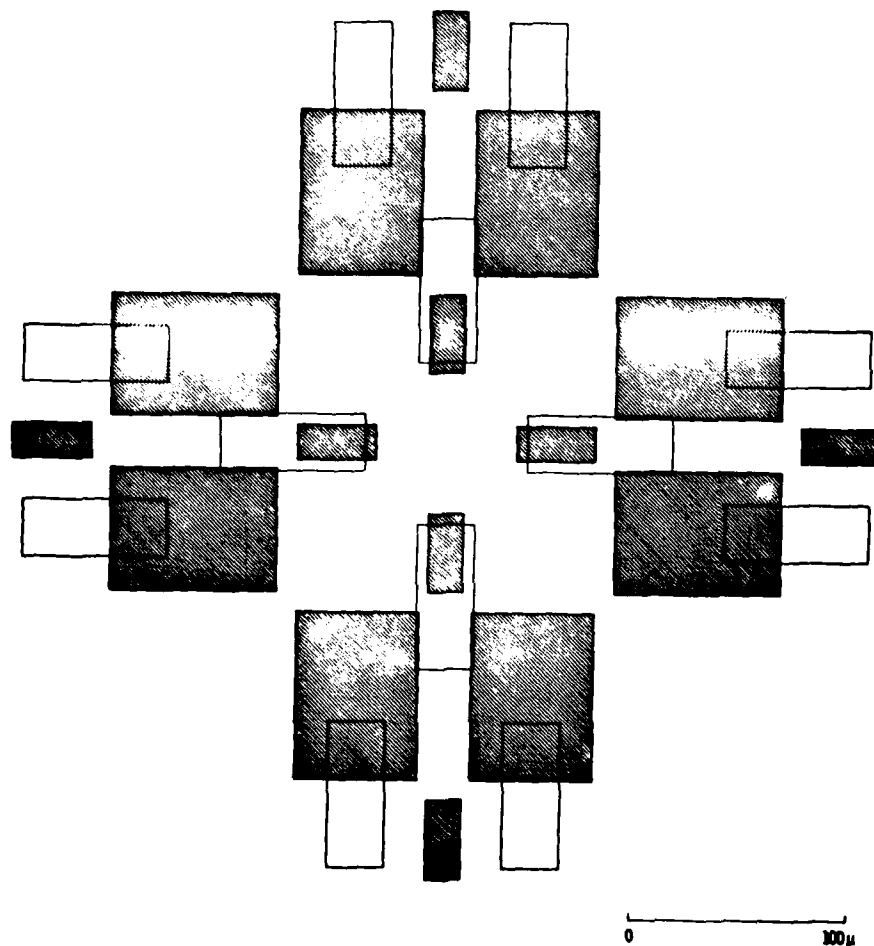


Figure 4.29 The target patterns used to facilitate photoplate alignment during assembly of the tooling. Locations on artwork are specified in Figure 4.18.

- ☐ MASK 1 GND#1-HIC#1  
DMD DISPLAY-2 VER 1
- ☐ MASK 2 HIC#2-VIC#1-GND#2  
DMD DISPLAY-2 VER 1
- ☐ MASK 3 LOGIC GATE-POWER GATE-GND#2  
DMD DISPLAY-2 VER 1
- ☐ MASK 4 INSULATOR  
DMD DISPLAY-2 VER 1
- ☐ MASK 5 SOURCE DRAIN  
DMD DISPLAY-2 VER 1
- ☐ MASK 6 VIC#2-TFT IC  
DMD DISPLAY-2 VER 1
- ☐ MASK 7 EL CONTACT-CAP PLATE  
DMD DISPLAY-2 VER 1
- ☐ MASK 8 LOGIC-POWER SEMI  
DMD DISPLAY-2 VER 1
- ☐ MASK 9 POWER SEMI  
DMD DISPLAY-2 VER 1
- ☐ MASK 10 EDGE CONTACTS  
DMD DISPLAY-2 VER 1

Figure 4.30 Mask identification inscriptions-"nomenclature". (Refer also to Figure 4.18).

Dwg. 7698A91

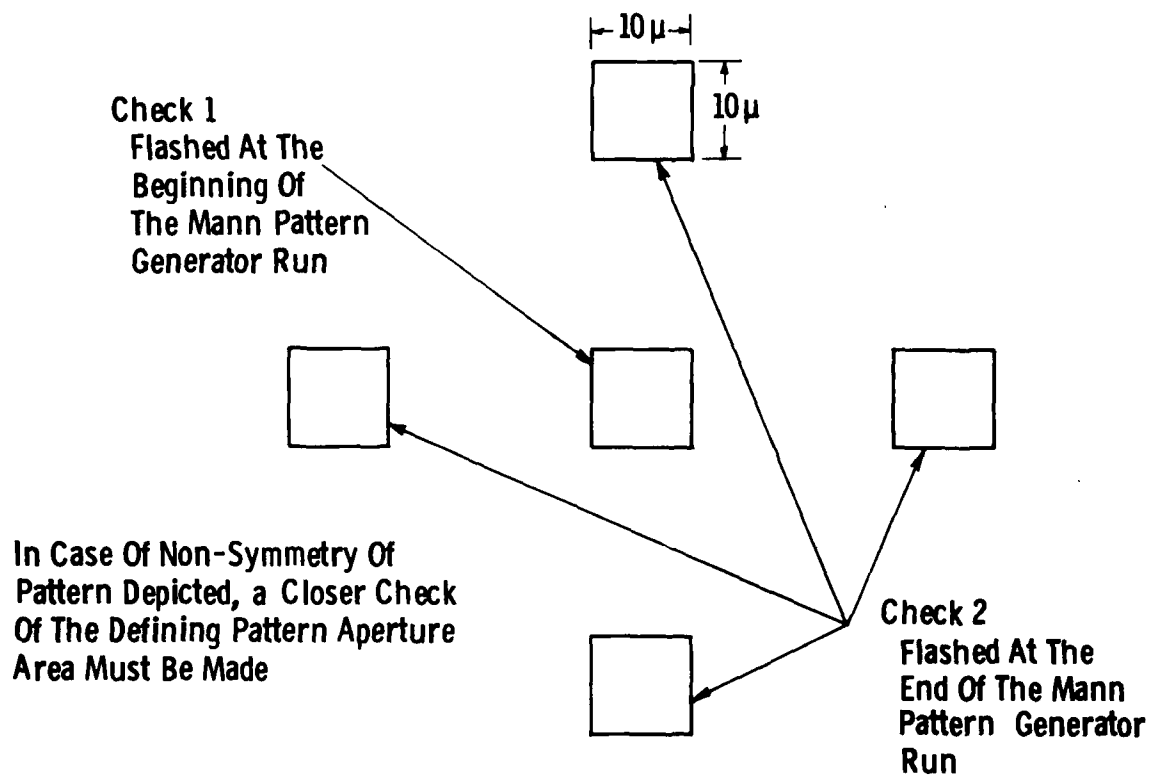


Figure 4.31 The check square pattern used to provide early detection of the most common mode of pattern generator malfunction. (Refer also to Figure 4.27).



#### 4.5 Photoplate Preparation

Over the years both before and during the current program, we have developed highly specialized techniques for dealing with the interface between the Applicon Graphics System and the Mann 1600 pattern generator, particularly for the purpose of fabricating thin film circuit masks. While it is not appropriate here to go into all the highly detailed procedures designed specially for this equipment, there are gross features of the process of generating photoplates whose description should be useful to anyone embarking on this type of work for the first time.

The essentials of photoplate generation begins with the compilation of the drawing data base as explained in Section 4.4, and ends with the act of inspecting the photoplates prior to their assembly into stencil mask phototooling as described in Section 4.2. The purpose of the present section is to provide useful information concerning steps between these two subtasks. A breakdown of these is illustrated in Figure 4.32. As indicated in Figure 4.22, we chose to render the drawing on the graphics system as a replica of the intended thin film pattern when viewed on the substrate with films "near." While this is not absolutely necessary, it is most convenient for rapid determination of whether predetermined design rules are properly observed. However, the nature of stencil mask fabrication as described in Section 4.2 generally requires photoplate flashes to be larger or smaller than their corresponding apertures and, furthermore, larger or smaller to a different extent for the relief side and defining side photoplates. The term "post-Processing" means appropriate manipulation of dimensions to ensure correctly compensated photoplate flashes. Attention must also be given to the mask identification nomenclature if it is to be properly inscribed on both sides of the mask with the proper polarity. The initial drawing must also be scanned to ensure that features beyond the capability of the pattern generator, such as acute angles, are not present. Finally, one also seeks to minimize, as far as possible, the run-time of the pattern generator. One does this by presorting the drawing or otherwise restructuring it in

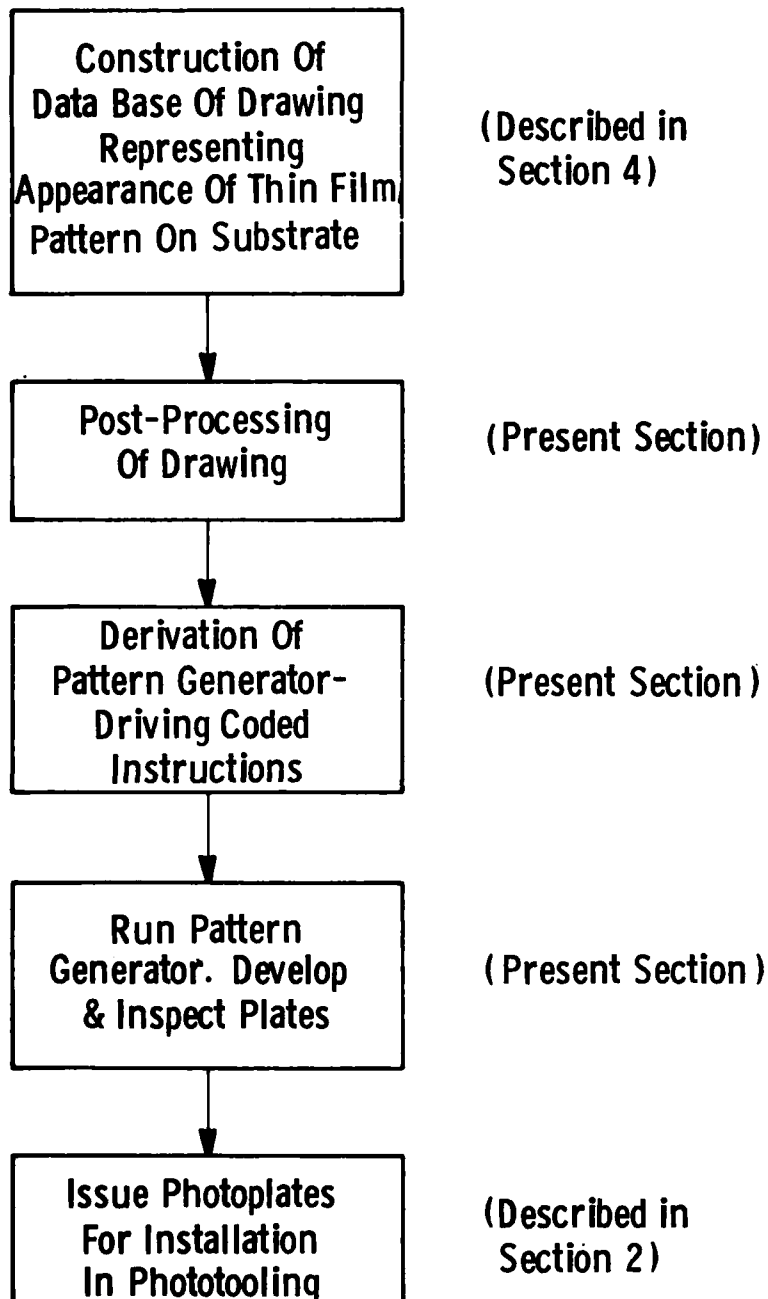


Figure 4.32 Gross breakdown of tasks involved in photoplate generation.

Dwg. 7698A94

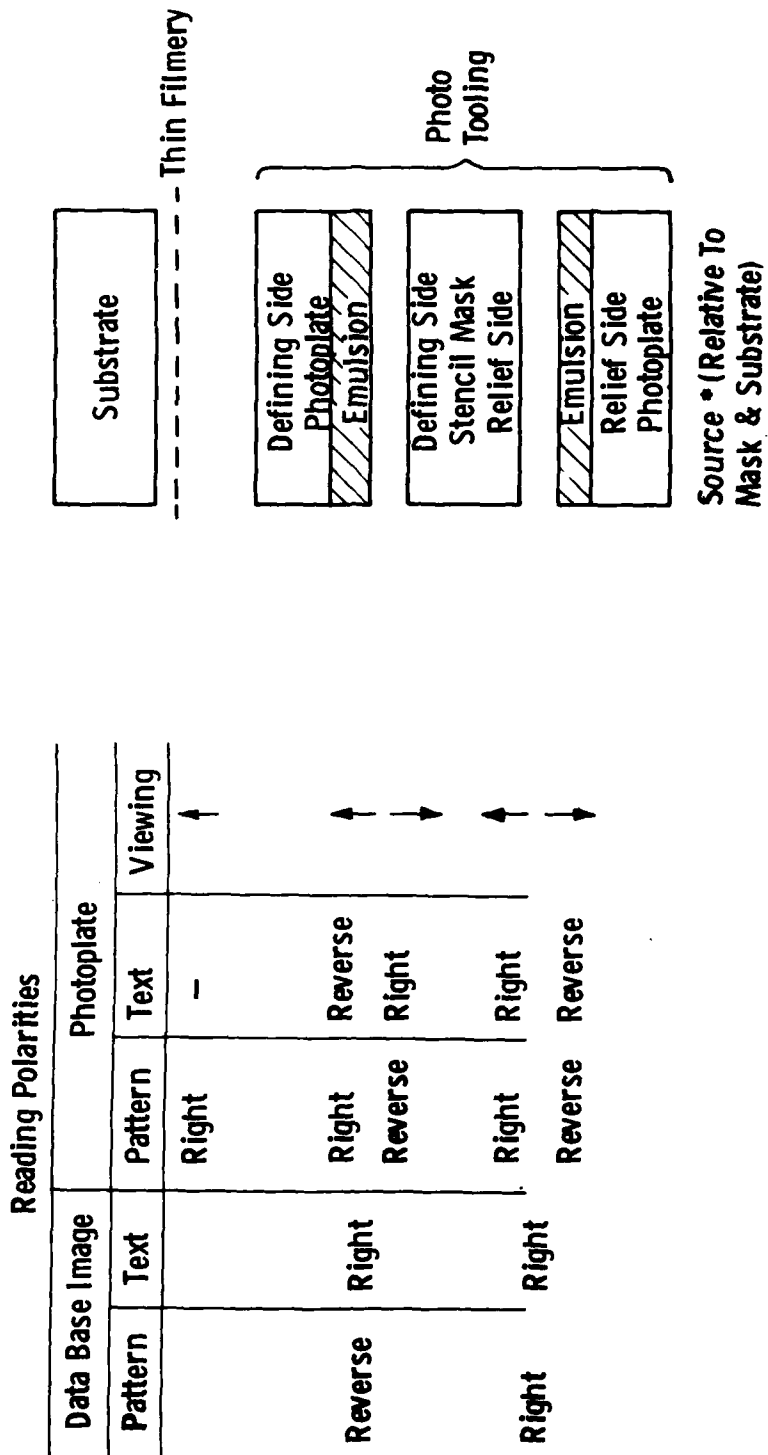


Figure 4.33 Right and reverse reading polarities of the defining side and relief side drawings and text.

order that the flash instructions so derived do not conflict substantially with the pattern generator's most efficient operating mode.

Depending on the hardware and software systems actually used, certain facets of the post-processing activity can be handled automatically. However, for our purpose, the drawing in Figure 4.33 indicates the kind of considerations which should be made prior to developing the Applicon/Mann interface. In essence, one derives conceptually two different drawings from the original. Because of the nature of the phototooling, with plate-emulsion in contact with the mask surface on either side, one drawing (corresponding to the relief side) is right reading relative to the substrate pattern and the other is reverse reading. However, the nomenclature text must be right reading on both drawings as shown. This scheme provides correct matching of the relief side and defining side flashes of any particular aperture.

With the type of thin-film pattern discussed in the previous section, pattern generator run times can easily exceed 40 hours per photoplate on the 1600 model if the drawing is not properly presorted. Besides scheduling difficulties, technical considerations demand that this run time be reduced to something less than 16 hours for smooth, fault-free operation. This is done by ordering the flash instructions to correspond as far as possible to the equipment manufacturer's recommendations, so that the travel path across the substrate is, for example, a continuous roster scan or some simple variation of such. Usually, flash instructions are transferred from the graphics system to the pattern generator via conventional magnetic tape. We tried three different ways of ordering the flashing instructions:

- (1) Using the optional sort of graphics system post-processing software itself
- (2) Through an off-line computer used ordinarily to transform the 9-track graphics system output to the 7-track code compatible with the Mann
- (3) Manual manipulation of the basic drawing data base

We were unable to make any one of these approaches perform really well. However, run times close to an average of sixteen hours per photoplate were finally obtained by a judicious combination of the first and third.

Even after a properly ordered 7-track tape had been written we ran into the next difficulty, which is mentioned here in the hope it may help anyone following this path in the future avoid unnecessary grief. The pattern area for this kind of work is somewhat more extensive than that encountered in LSI. Whereas conventional 4"x5" photoplates are acceptable for the latter, we found (the hard way) that specially ordered center-cut photoplates should be used to help eliminate any adverse effects resulting from deterioration or other quality problems sometimes observed near the edges of the pre-cut 4"x5" photoplates as delivered by the manufacturer.

Ordinarily, the actual running of the pattern generator presented no special problems. However, on an earlier program, we had determined that the failure of a particular thin-film circuit to operate properly was the absence of a particular flash on one of the master plates. (The phototooling naturally failed subsequently to provide the corresponding aperture on the stencil mask). This very rare failure mode can be detected as far as our existing resources are concerned only by visual inspection, which is not too difficult with an optical comparator. However, we soon learned how to detect a second and more common failure mode more rapidly. For reasons unknown at this time, the pattern generator flash head would randomly "get lost" by as little as 5 or 10 $\mu$  while flashing a plate. This resulted in the location of all flashes made after the fault occurred being displaced by the same amount, usually undetectable to the naked eye (and sometimes even with exhaustive microscope scanning), to those made before the fault occurred. To ensure detection of this most common (but still rather rare) failure mode, we used the so-called check pattern shown previously in Figure 4.22. As indicated there, the flash instructions are ordered by one way or another so that the square at the center of the check square complex is flashed prior to any other in the pattern. The four peripheral squares

are flashed last of all. With the sub-pattern arrangement shown, this most common failure mode of the pattern generator was most readily detectable. Although this occurred only once during the present pattern redesign for the DMD display, the check square pattern itself was responsible in this case for saving many weeks, and possibly months, of delay in obtaining a 100% "correct" set of new masks.

The last act prior to receiving finished stencil masks from the supplier was to arrange transmittal to all twenty photoplates to him. Whereas we did receive complaints of the lack of pattern edge definition, he immediately made high contrast photocopies of the master by contact printing for use in the phototooling.

At this point we have come full circle in the pattern redesign and mask procurement task of our program. The interested reader is referred back to Section 2 for a review of how the stencil masks are derived from the photoplates.

#### 4.6 Impact of the Revised Mode and Pattern Design

The execution of the mask redesign and procurement task of the final eight-month phase of the program (begun in November 1978) more than fulfilled our expectations of its complexity and its demands on time, labor and patience. After all, whereas the technical desirability of the operation had been firmly established over a year earlier, no commitment to it had been made because of trepidation experienced in earlier mask design activity. However, in spite of its cost--about \$10,000--the money seems to have been well spent. Prior to the final phase of the program, we could produce circuits at the rate of about 20 to 24 pieces per month. Over the preceding four-month period, using the old masks, only two complete DMD displays with viewability approaching the contract-required level had been made. The spending level often exceeded \$100,000 per month.

During the final few weeks of the program, which was the only time that the full complement of new masks had been available, circuits were made at an effective rate of more than 40 per month. We routinely converted these into readable displays with about 50% yield. This does not mean that the displays were blemish-free but that they were at least as good as those made with the old masks. This is done with a comparative spending level of less than \$35,000 per month. Whereas numerous processing, test, and evaluation improvements were also made during the same time period, it is our judgment that the mask redesign task was the key element in the success of the overall strategy formulated in November 1978 for the final eight months of the program.

On the negative side, one disturbing aspect of the mask redesign has emerged. It is simply that our redesign was not revolutionary enough. During the later days of the mask redesign and procurement effort, several excellent ideas came to light which, had they been incorporated into the redesign, would, undoubtedly, in the light of subsequent experience, have enormously contributed to yield if not to throughput. Although circumstances did not permit a second redesign cycle, these concepts are sufficiently important to justify the discussion provided in the next and final section.

#### 4.7 New Design Concepts for Further Yield Improvements

Subsequent discussion in this section acknowledges a certain philosophy which has emerged concerning the viability of the manufacturing process to which the current program is committed. The discussion is limited within the framework of the all-stencil mask process.

The technical strategy formulated for this final phase of the program implicitly hypothesized that the marginal visible success of prior work was largely attributable to difficulty of fabricating a fault-free bus-bar complex. This is one of two components of the phosphor dot matrix-driving circuit. The other component is the assembly of identical active circuit elements located at the bus bar intersections, previously illustrated schematically in Figures 4.13 and 4.14. The

basis of the hypothesis is that a defect originating during the fabrication of our elemental circuit generally affects that pixel element only. We had earlier demonstrated that a 8 x 16 character half-display could accomodate up to 100 such defects and still meet contract viewability requirements. Furhtermore, extensive experience had convinced us that over the long haul, the relative rate of appearance of such defects was typically less than fifty (out of 4480 pixels) and averaged more like twenty five. In addition, even during varied process experimentation over a course of thirty batch runs, we had never failed to make transistors capable of at least initially perfomring their required function.

On the other hand, a single bus bar defect can "destroy" as many as 24 characters. A typical post-vacuum bus bar defect count of as few as ten can render an otherwise "perfect" display totally unreadable. Thus, the essence of the stated hypothesis; visible success in the current program as evidenced by a copious flow of displays exceeding the 97% viewability requirement, has been limited only by the difficulty of making a vacuum-deposited fault-free bus bar complex. Next to this problem, transistor problems (including "stability"), real or otherwise, are minimal.

We had only a precious few weeks to work with the new masks. Their redesign was highly directed at "bus bar yield". Neither the new process "recipe" nor the mask redesign made any change to the transistor structure. Our modest success in routinely fabricating viewable displays, (within limits permitted by our unprecedented and extended series of mechanical and electrical failures of the automatic vacuum system!) we consider vindication of the hypothesis. That is, if our success has, in any way, been less than resounding, the reasons are:

1. The impact of defects on viewability is the major limiting factor of the manufacturing concept.
2. By far, the most serious defect occurs in the bus-bar complex.
3. Defects in the elemental active circuits affect viewability performance very marginally.



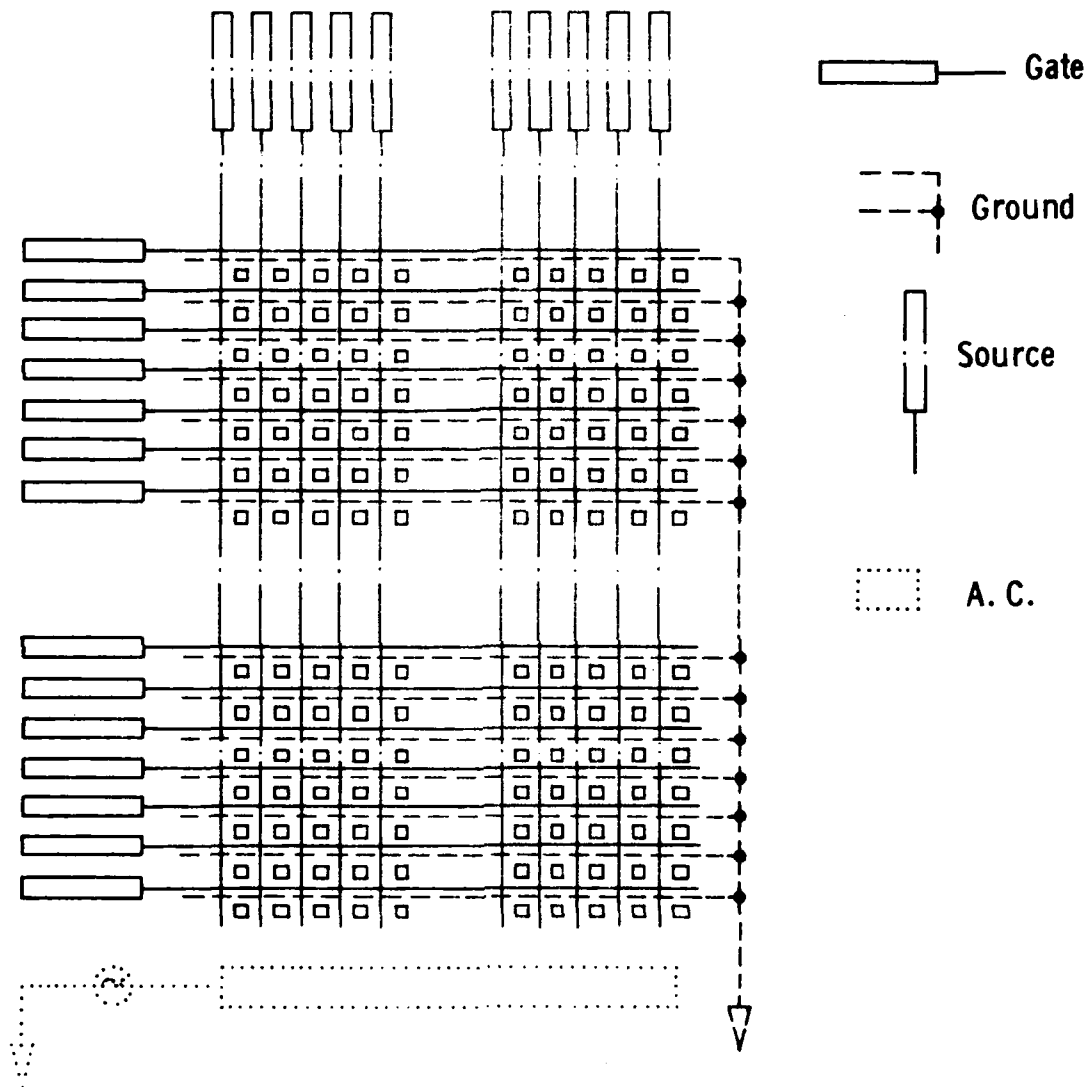


Figure 4.34 Four-character version of existing bus-bar scheme--new pattern design. (Refer also to Figure 4.5).

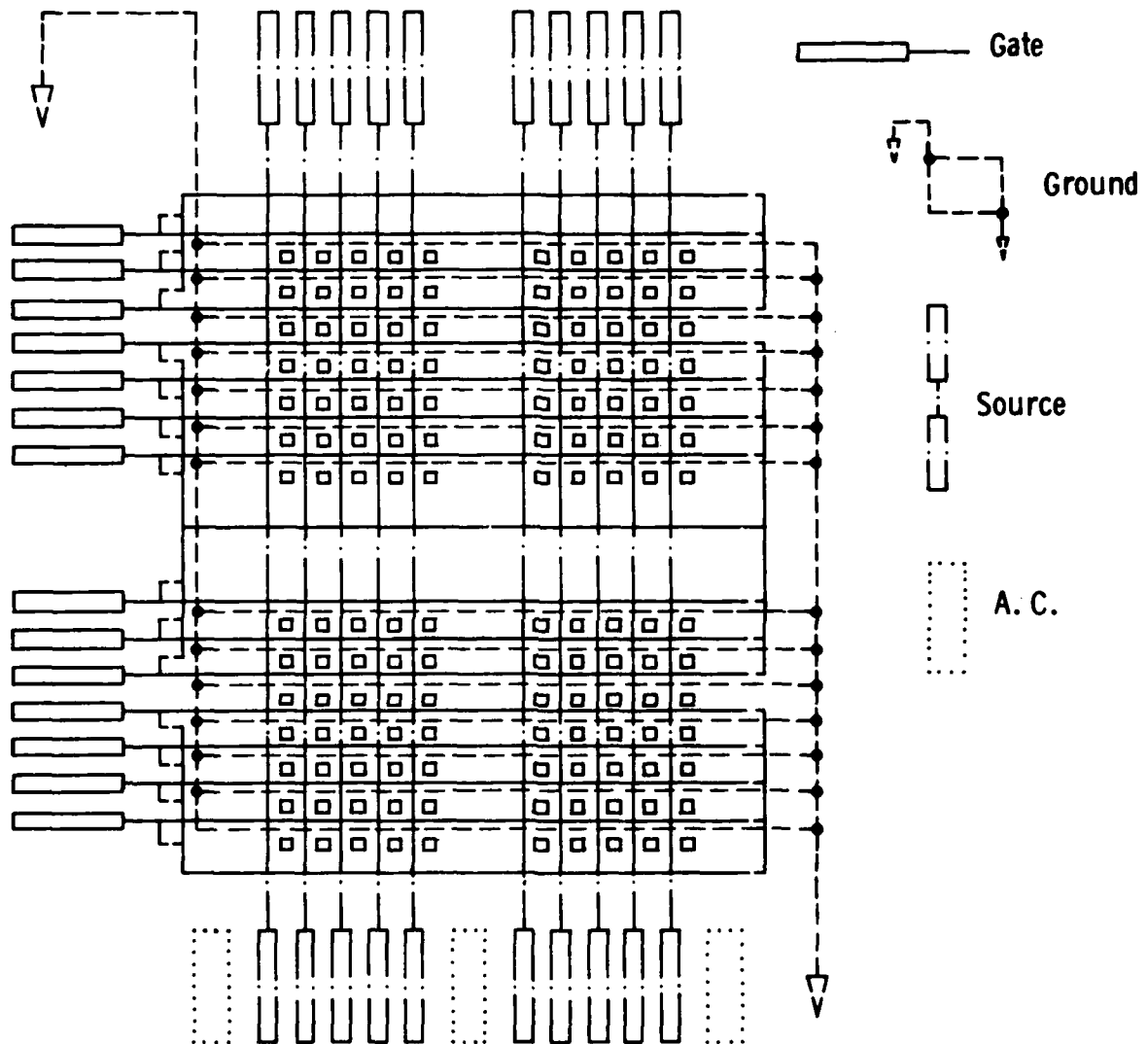


Figure 4.35 An alternative bus-bar scheme derived by additions to the existing pattern. This would render bus-bar defects (opens and shorts) inconsequential if maintained at their recent density.

4. At no time in this last phase of the program have transistor operating characteristics, their uniformity or reproducibility had any negative impact on reaching program goals.

Consequently, this final section of the present report appropriately describes a few further design modifications which future workers in the area should find most beneficial. Consistent with the subjective philosophy disclosed above, they are directed at further eliminating or minimizing the impact of bus bar defects. They alone may not resolve all the bus-bar problems; however, the features to be suggested should substantially clear the air and reveal the identification of the next most serious problem.

The substance of our recommendations can be inferred by comparison of Figures 4.34 and 4.35. The former illustrates the nature of the existing bus-bar scheme as featured by the new pattern design. Whereas the new design contributed the important features of yield and testability as described in Section 4.4, it did not include any special features for repairability. Figure 4.34 indicates one way in which this might be done within the scope of the existing alpha-numeric format. Some alternative trickery would have to be devised, of course, to achieve the same ends for a graphics panel. The claim we make is that with the pattern additions shown in Figure 4.35, the defect density we now typically observe in bus bar patterns would be inconsequential as far as viewability is concerned. We shall illustrate this claim with a few examples of the five bus-bar defect types, namely:

1. Source bus opens
2. Ground bus opens
3. Gate bus opens
4. Source-ground shorts
5. Source-gate shorts

As a prelude however, we should emphasize that in addition to the benefits indirectly accruing from the existing new pattern design described in Section 4.6, we have also demonstrated a dramatic drop in

average open counts. In fact, we have made four circuits with no open bus-bars of any kind. On the average, we now see less than three of each unless some type of malfunction of the vacuum system hardware occurs. Anyway, for the purpose of discussion, we will assume that between zero and three opens of each type will continue to be the norm for 90% of the circuits produced.

By inspection of Figure 4.35, it should be obvious that a single open in any source of ground bus-bar will be totally inconsequential as a result of the supplementary external contacting to the circuit. An open in a gate bus-bar is not so easily compensated for, since the finished display continues to be assembled from two abutted half panels of the type shown in Figure 4.35. (The righthand side must continue to be free for abutment). However, by depositing a floating gate bus-bar between characters, an open in any one of seven successive gate bus-bars can readily be accommodated by a simple post-test manual interconnection of appropriate points "pre-wired" to the defective bus.

The fourth defect type is, in principle, readily resolved by the expedient procedure self-explained in Figure 4.36. For type 5, source-gate shorts, one can do much the same sort of thing provided, of course, that the source bus which is shorted is not somewhere else open. Once again, the defect density we now typically observe suggests that multiple defect complexities have now become relatively rare.

In conclusion, this Section attempts to offer a convincing solution to the only problem which remained an obstacle to highly visible success. It does this by identifying the bus-bar defect as the root of the problem and explains how this could now be rendered manageable as a consequence of the features already incorporated into the new pattern design.

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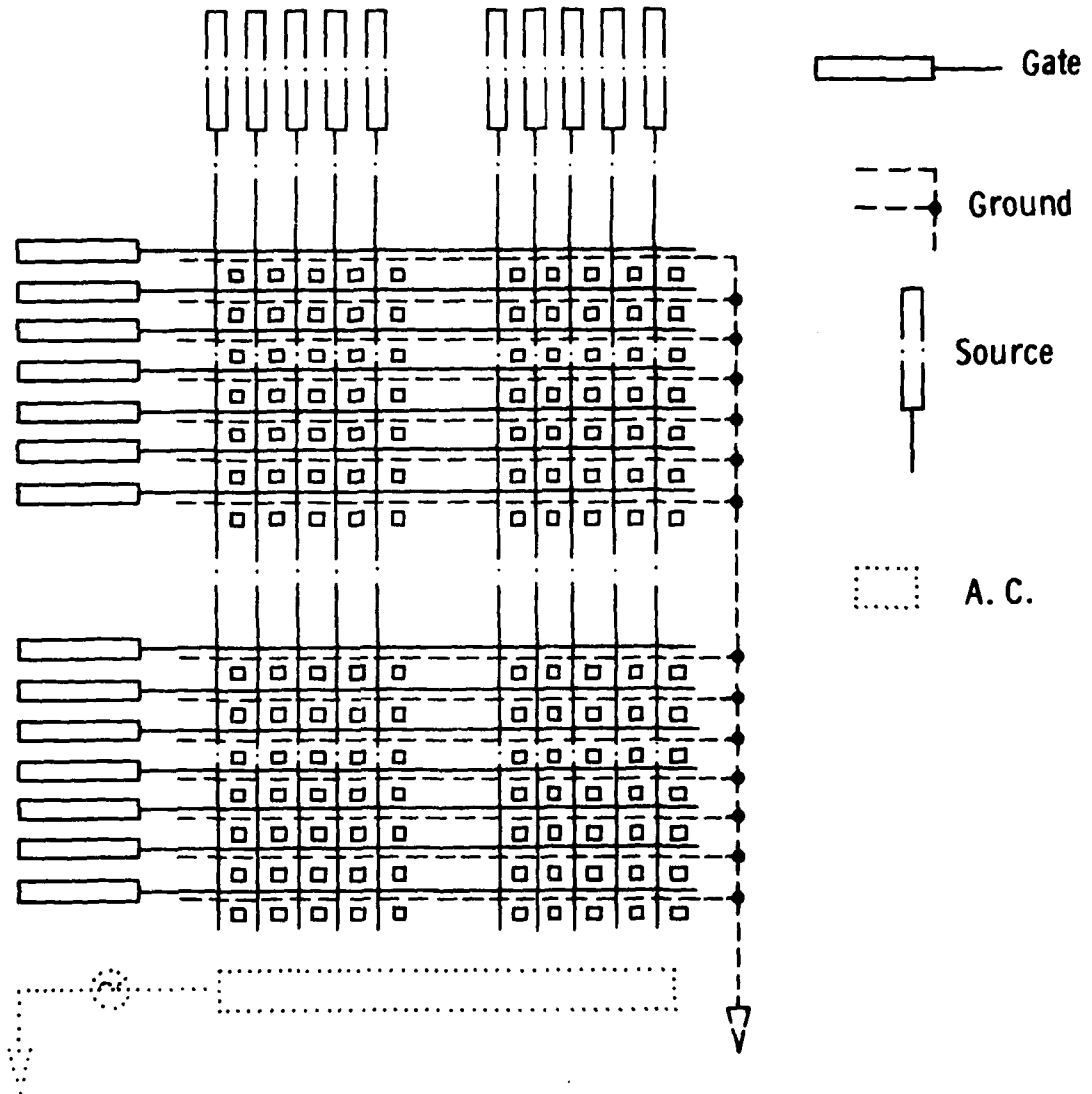


Figure 4.36 Resolution of Type 4 bus-bar defect (source-to-ground short) with the bus bar scheme shown in Figure 7.2.

## 5. CIRCUIT FABRICATION

### 5.1 Materials and Deposition Techniques

#### 5.1.1 The Insulator and the Metal Contacts

Because of their intimate interconnection, the materials used for these components must be treated together. It has been demonstrated that  $\text{Al}_2\text{O}_3$  made by electron beam evaporation is oxygen deficient and that oxygen vacancies act as electron traps. Furthermore, the number of charges that get trapped when an  $\text{Al}_2\text{O}_3$  capacitor is charged up is a strong function of the metal used to make the contact. Eisele showed that by heating the  $\text{Al}_2\text{O}_3$  in oxygen or air at  $400^\circ\text{C}$ , the trapped charge density could be reduced from  $10^{18} \text{ cm}^{-3}$  to  $10^{16} \text{ cm}^{-3}$ .<sup>(14)</sup> That the effect is due to the addition of oxygen and not due to temperature was demonstrated in a similar heating experiment in dry hydrogen with no apparent reduction in charge storage capability.

The metal used is also important since top and bottom aluminum electrodes resulted in two orders of magnitude less charge storage capability than gold-gold, copper-copper or indium-indium electrodes. In all, the effects of insulator fabricating and processing conditions plus those of the electrodes range from  $10^{16}$  -  $10^{14} \frac{\text{charges}}{\text{cm}^3}$ .

$\text{Al}_2\text{O}_3$  with aluminum electrodes has a very high breakdown field strength undoubtedly associated with the foregoing charge phenomenon. For these reasons, the Al -  $\text{Al}_2\text{O}_3$  combination has been used extensively in flat panel display circuitry, although it is not clear that the optimum conditions, (i.e. low charge storage) are always present in the fabrication.

There are, however, a number of disadvantages of aluminum.

They include:

- (a) non-ohmic contact with the CdSe semiconductor requires use of multi-metal depositions.

- (b) high self diffusion rate resulting in dendritic growth during annealing, resulting in defects
- (c) poor scratch resistance

6000 Å of  $\text{Al}_2\text{O}_3$  would break down at about 300 volts so that an EL phosphor operating with less than 150 volts r.m.s. sine wave excitation could be comfortably accommodated. It is found that the gain and leakage current requirements are adequately met using this value; other parameters of equal importance are available to make further adjustments to these quantities.

#### 5.1.2 The Semiconductor and the Source-Drain Contacts

The semiconductor used exclusively on this program was CdSe deposited by electron beam evaporation. The thickness of the film is only 150 Å and the deposition is at 4 Å/sec onto a room temperature substrate. This results in an open network of amorphous CdSe. Films deposited under these conditions tend to be cadmium rich so that the conductivity is quite high.

The electrical characteristics of the TFT's, before they are annealed show a high n-type conductivity with very little modulation, and no saturation, whereas after annealing, saturation of the drain current occurs, the modulation is pronounced, and the conductivity at low voltages remains high. This behavior implies that the "as deposited" semiconductor has a high carrier concentration so that the threshold voltage  $V_T$  is very large and negative. Large values of drain voltage would be required to bring the device into the saturation region. However, the current in such a case would be so high that the TFT would be destroyed and we don't observe the effect.

Annealing has an effect on the crystallinity of both the semiconductor and the insulator. The annealing is done after the circuit is complete so that the net composition of the semiconductor which is sandwiched between two insulators, is unlikely to be altered. One would expect, in this case, that any stoichiometric imbalance in the

semiconductor would be adjusted either by chemical reaction with the insulators or by precipitation of the excess specie in the grain boundaries.

It has been observed that TFT s made with sputtered insulators show the current saturation even before annealing.<sup>(15)</sup> Whether or not the effect is related to an insulator property or is due to an effect on the semiconductor during the sputtering operation is uncertain. It is certain, however, that the semiconductor was heated much more during the sputtering of the top insulator than it is during a corresponding electron beam evaporation so that the semiconductor, being only 100 Å thick, was adequately annealed during the sputtering.

No detailed analysis of the conduction mechanism in a 100 - 150 Å thick semiconductor has been given. Anderson<sup>(16)</sup> shows that the nucleated islands have just begun to touch at that thickness. He also shows that for CdSe, the sizes of the grains, after annealing, is about equal to the film thickness so that the granules are 100 - 150 Å in diameter. Normally, one would expect the conduction mechanism to be dominated by grain boundary scattering when the grains get very small; however, there is a lower limit on grain size below which quantum mechanical tunneling from one grain boundary to the next would be expected to become important. This, after all, is observed in electron tunneling through insulators at film thicknesses of the order of 100 Å or less.

Much more work must be done to understand the physics of such thin semiconductor films.

The materials used for the source and drain contacts are chosen primarily for their ability to make a good ohmic contact to CdSe. It had been discovered very early in the development of TFT's at Westinghouse that indium made good contact and that by adding a layer of gold, a highly conducting ohmic contact was established. Indium adheres well to the substrate and forms several intermetallic compounds with gold.

The TFT s made with gold-indium source-drains on 100 - 150 Å CdSe were quite clearly enhancement mode devices, that is to say, a



positive gate voltage was required in order to get the device to conduct. By adding indium to the semiconductor, the threshold voltage could be changed continuously from positive to negative. The real benefit, however, was the affect on the drift in the threshold voltage with time. By drift we mean the drift in the drain current immediately after the TFT is turned ON after it has been held OFF by a suitable gate voltage for an extended period (say 10 seconds). We found that with no indium added to the CdSe, the drain current would drift up after the OFF period. As the indium concentration in the CdSe was increased, the drift would gradually change from up to down so that there was an optimum value of the indium concentration at which the drift was zero. This occurred at .8 of % indium to CdSe. All of our TFT s are made with this amount of indium.

The indium is added directly to the CdSe source material and fried in N<sub>2</sub> at 800°C for 2 hours.

Experiments were performed in an attempt to understand the function of the indium in the source drain region and the way it was distributed with respect to the semiconductor. Several samples with different permutations of the semiconductor indium and gold layers (indium and gold in the source drain electrode positions) were made.

The samples made are listed in Table 5.1. Each sample was made with a source drain gap of 50  $\mu$ m and the source drain contacts extended beyond the semiconductor onto the substrate.

TABLE 5.1

Samples Made to Study Indium Diffusion

Film	Sample #1	Sample #2	Sample #3
Bottom	CdSe	CdSe	Indium
Middle	Indium	Gold	Gold
Top	Gold	Indium	CdSe

The samples were examined by Auger spectroscopy before and after annealing for 10 hrs. in nitrogen at 350°C. It was found that where there was no CdSe, the anneal caused the indium to alloy with the gold to form a very rough textured film. In sample #2, the gold did not adhere well to the glass and holes in the gold could be seen through the glass substrate. The Auger studies showed that indium diffuses through the gold into the CdSe. In fact, in sample #2, after the annealing, no indium was seen in the areas of the source and drain that overlapped the CdSe whereas it was present in abundance away from the overlap. In the gap between the source and drain there was no perceptible level of indium present before or after the anneal so that the indium added to the source-drain region apparently stays there and does not diffuse into the gap.

Other materials used for source drain contacts have invariably shown much higher leakage currents. Cu-In contacts, which might have a leakage current of 100 na/square (as compared with 1 na/square with Au - In), are found to produce transistors with considerably higher voltage capability.<sup>(17)</sup> Nickel source drains also make good ohmic contact and have been used but do not show the same high voltage capability as Cu-In.

A major advantage of the use of nickel is that it can be used universally in the circuit. In addition, nickel is a hard material and is therefore scratch resistant in contrast to aluminum which is very soft.

The results achieved so far with nickel devices are very encouraging; however, the occurrence of short circuits remain the most critical defect to be overcome. We do not have any information on the amount of charge trapping in  $\text{Al}_2\text{O}_3$  with nickel contacts nor on the effect of nickel on the breakdown field strength of the Ni- $\text{Al}_2\text{O}_3$  system.

### 5.1.3 Electrical Shorts

The most critical defects in the display panels at present are electrical shorts. They develop either during the deposition phase or during the post-deposition anneal. Evaporation of metals, insulators, and semiconductors results in the production of debris that may come

directly from the hearth (spitting) or from flakes of previously deposited material breaking away and ending up on the substrate. During the post deposition annealing phase, metals can diffuse and produce hillocks. Self diffusion in aluminum is particularly pronounced so that when the stresses build up due to thermal expansion, those stresses are relieved by the hillock formation. Long dendrites have been observed growing from the edges of exposed aluminum bus bars. Although no direct observations have been made of cases where aluminum actually punches through an overlying insulator, it is suspected that aluminum might migrate through pinholes in the  $\text{Al}_2\text{O}_3$  insulators. There are two approaches to solving this problem:

1. Replace aluminum with a non-migrating metal, e.g. nickel or even better, molybdenum.
2. Prevent insulator pinholes and prevent hillock and dendrite formation.

The first approach is the one that was adopted toward the end of this contract with nickel being used. The results have not been entirely satisfactory because electrical shorts remain and had to be manually removed before the panels could be used. The repair of panels is discussed elsewhere.

No serious attention was paid to the second option but some experiments we performed demonstrated feasibility. It was observed that a layer of copper under an aluminum layer allowed the aluminum to migrate easily during annealing. The copper seemed to provide the necessary "elbow room" and acted to prevent hillock formation completely. Several substrates were made using this technique on a laboratory vacuum system showing virtually no shorts.

#### 5.1.4 The Insulator-Semiconductor Interface

Of all the properties of thin film transistors, the one that has been held up as the most debilitating is the tendency of the threshold voltage to drift with time. The drift is basically a change in the number of carriers in the semiconductor due to the filling or emptying of traps at the insulator-semiconductor interface or at some shallow depth

in the insulator. We know, from our discussion above, that the insulator has plenty of electron traps in it because of oxygen deficiency and that it is very difficult, if not impossible, to get rid of them completely. The best that Chan and Hill<sup>(18)</sup> were able to do by way of eliminating charge trapping was to reduce the trapped charge in a 6000 Å film to  $6 \times 10^{-8}$  coulombs/cm<sup>2</sup>. If we take the dielectric constant of Al<sub>2</sub>O<sub>3</sub> to be 8, the induced charge density (coul/cm<sup>2</sup>) on a 6800 Å thick Al<sub>2</sub>O<sub>3</sub> insulator charged to 6 volts would just about equal  $6 \times 10^{-8}$  coulombs/cm<sup>2</sup>. As Chan and Hill point out, the trapped charge is distributed throughout the insulator, albeit non-uniformly, so that some number considerably less than  $6 \times 10^{-8}$  coul/cm<sup>2</sup> could be trapped from the semiconductor. However, these were the least "trappy" insulators and the level could easily rise one or two orders of magnitude as they showed.

The trap distribution is inherently non-uniform and increases towards the front (growing) surface of the insulator. In our panels, two insulator layers are used, one either side of the semiconductor. The oxygen depletion is therefore, non-symmetrical because the history of the Al<sub>2</sub>O<sub>3</sub> source material is non-symmetrical.

It has been found empirically that the stability of the TFT's against collapse (a phenomenon to be described below) can be improved by evaporating 200 Å oxide layer adjacent to the semiconductor, on both sides of it, without adding oxygen gas. The evaporation rate for this layer is 20 Å/sec - a very high rate that should produce a high density of oxygen vacancies. The rest of the insulators (both sides) is deposited at 5 Å/sec (still high) with  $5 \times 10^{-5}$  torr of O<sub>2</sub>. It is conceivable that this procedure acts to soak up any oxygen that may have been trapped or reacted with the CdSe. In another paper,<sup>(19)</sup> Chen & Hill demonstrate the effect of oxygen in reducing the conductivity of CdSe.

Many factors influence the characteristics of TFT's. The attempts to stabilize or optimize in one area invariably modifies the performance in another. We have not yet acquired sufficient experimental data nor have we conceived of the proper experiments to fully understand the behavior of TFT's. But within the framework of their application

in a display panel, they can be made so as to function well and drift just becomes a circuit design parameter. The major problem, the one that stands in the way of manufacturing a large number of panels cheaply seems to be the automatic elimination of electrical shorts. This can and will be accomplished through innovation in the manufacturing method.

## 5.2 The Automatic Vacuum Deposition System

This equipment is used for the fundamental task of sequentially registering series of masks over a substrate, and for each mask so registered, locating the substrate-mask composite assembly over the appropriate material source. The basic configuration and features of the equipment specified by Westinghouse and designed and built by Vacuum Technology Associates of Denver, Colorado is shown schematically in Figure 5.1.

The system provides the required function with three so-called wheels mounted as shown in Figure 5.1. Masks on the mask wheel are mounted with radial and axial symmetry as shown; the same applies for eight substrates on the substrate wheel. A third wheel accommodates the actuator mechanism which pneumatically registers a selected mask in contact with a selected substrate. Three material vapor sources are located approximately as shown in the Figure.

The basic mode of operation begins with the location of a selected mask over a selected substrate at an arbitrarily located pre-registration station. This is achieved first by rotation of the mask wheel and then by rotation of the substrate wheel, both by means of a concentric drive mechanism. Both wheels are then rotated synchronously until the selected substrate-mask pair are properly located over the selected source. The actuator mechanism located on the actuator wheel is then registered above the same source by rotation of the latter. Finally, the actuator engages the substrate and mask holders in a manner which ensures accurate registration of, and intimate contact between the mask and substrate. After evaporation of material, the actuator disengages the substrate and mask holders permitting subsequent independent rotation of their respective wheels for repetition of this basic step in the thin film pattern synthesis.

All operations described above, including a complex sequence of sub-operations involved in material operation, are controlled by a dedicated minicomputer system reading from a pre-formulated process

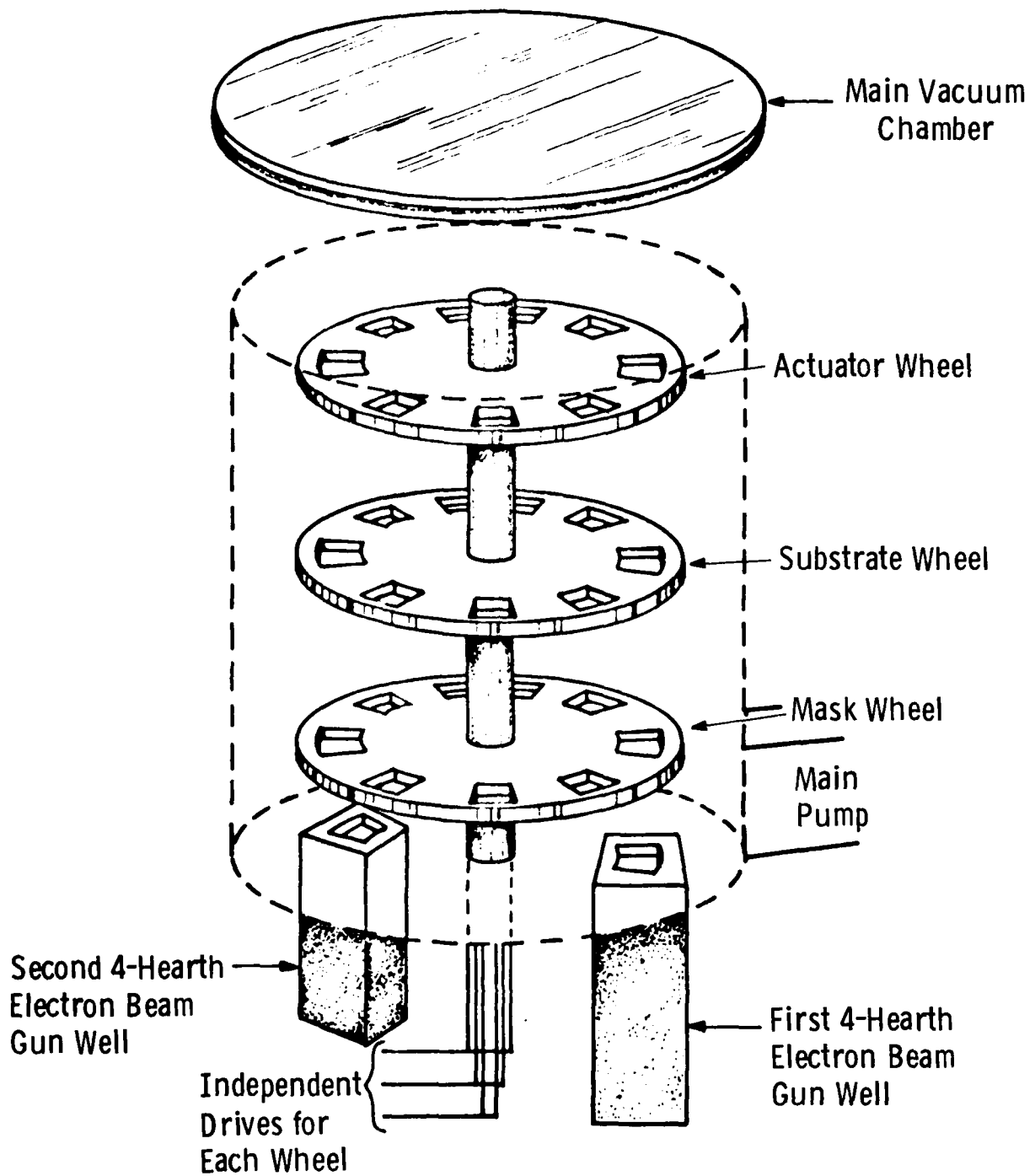


Figure 5.1 Basic features and configuration of the Automatic Vacuum System.

"recipe", described in Section 5.3. An overall view of the actual system is shown in Figure 5.2. From the left, the photograph shows the main vacuum chamber cabinet, the two control panels and two racks of the computer components. The latter are shown in more detail in Figure 5.3. The actual appearance of the mask and substrate wheels (shown schematically in Figure 5.1) are shown in Figure 5.4.

The horizontal diameter of the vacuum chamber is 40" and it is approximately 10" deep. It is constructed of 304 stainless steel to expedite cleaning. Volume has been kept to a minimum. An L-shaped VITON seal and a flat top cover are used. The side pumping post is rectangular with a transition to a 10" nominal circular post which has been adapted to mate with a 6" nominal pumping station.

The pumping system consists of an NRC VHG 2400 L/S diffusion pump with an NRC 316-6 Cryotrap. A first mechanical pump, a Welch # 1397 500 L/M model with a VTG coaxial trap, is used to rough the system and back the diffusion pump. A Welch # 1405H 35 L/M is also used to back up the diffusion pump during those times when the main pump is in other service.

Model NRC 801 thermogages monitor roughing line and foreline pressures. Shultry-Phelps and Bayard-Alpert gauges monitor process control information for the computer.

The pumping system has a capacity of  $27 \text{ ft}^3/\text{min}$ . Pressures of  $10^{-8}$  torr are possible although circuit synthesis can be conducted in the  $10^{-7}$  and  $10^{-5}$  torr range. An automatic pressure controller permits stable backfilling with argon or oxygen up to  $10^{-2}$  torr partial pressure.

The movement of the mask, substrate and actuator wheels is accomplished with reversible DC motors with forward/reverse positive stop capability. The position indexing of each wheel is read from a microswitch stack mounted on the wall of the vacuum chamber. Multiple cams mounted on the periphery of each wheel actuate these switches.





Figure 5.2 The Automatic Vacuum Deposition System.

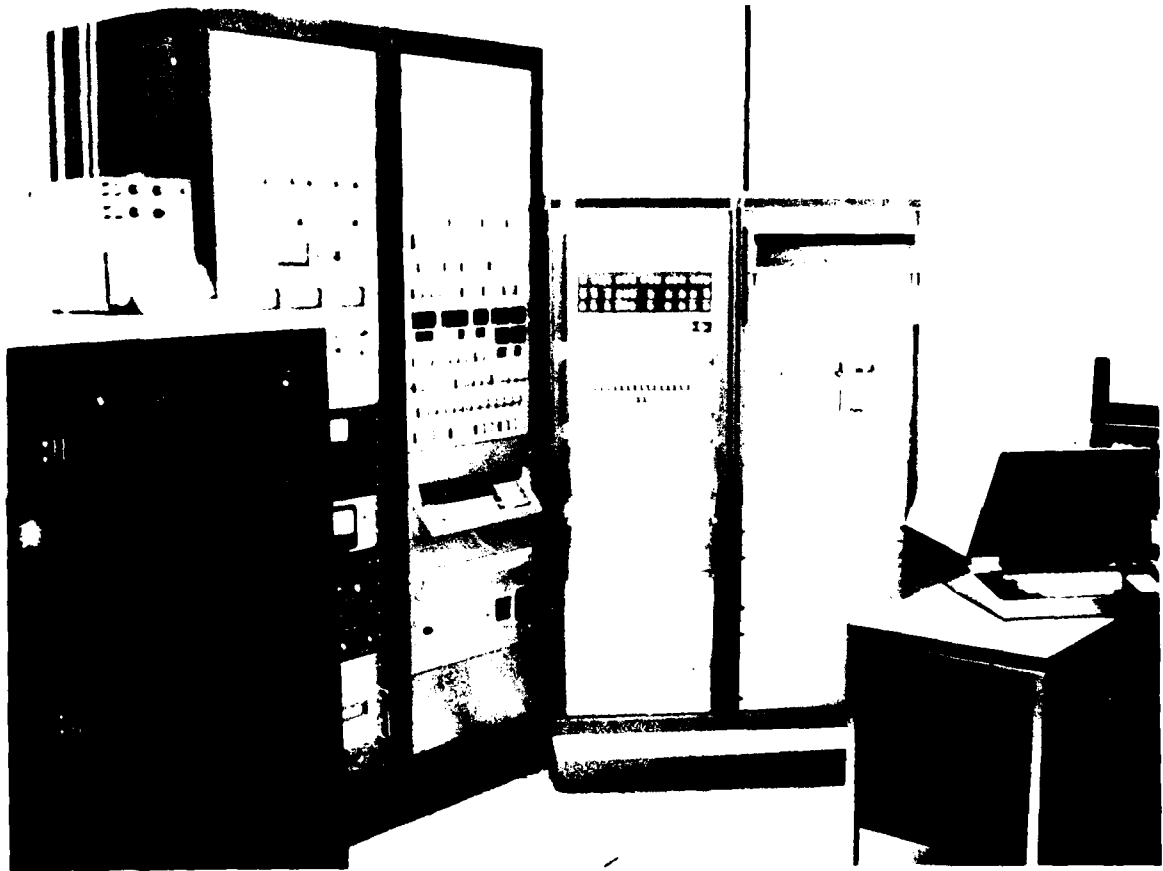


Figure 5.3 The main control panel and computer.

Electrically, the indexing is accomplished by reading in a BCD station code for the substrate, actuator and wheels and the desired station. These are combined to generate a binary code which is one of the address codes generated by a set of internal microswitches. There is a binary address code for each possible position of the substrate, actuator and mask wheels. The two binary numbers are compared digitally and if unequal, the motor drive to that wheel is actuated. When the numbers are equal the motor is turned off. The same system is used to select hearths for the two electron beam guns. The BCD numbers can either be entered manually or by the computer in the automatic mode.

Each substrate holder forms an integral part of the magnetic pull-up fixture, which operates with the mask holder to achieve the following functions:

- (1) A strong magnetic pull to the mask to keep it in intimate surface contact with the glass substrate. Surface polarized multipole magnets are used.
- (2) A registration of the substrate to the mask that is repeatable to  $\pm 0.2$  mil.
- (3) Control, through the pneumatic actuator, to correctly make and break the contact.

The operation of the magnetic fixture is as follows: The magnet must be retracted when the substrate is being entered. It then drops gradually, with uniform levelness relative to the substrate, onto the substrate. Eventually, being supported by the substrate metal frame, it contacts the glass substrate itself. At the end of the deposition, the controller must (a) retract the magnet slowly to a distance at least 1.5" from the substrate and (b) raise the substrate off the mask. Lastly, the transport mechanism engages and moves the substrate out.

The smoothness of the motion of the magnet as it comes up and down, the initial breaking of the magnet/substrate contact prior to the

breaking of the mask/substrate contact and the uniformity and levelness of the magnet on the substrate are all important.

Figure 5.4 is an assembly drawing showing the operation of the magnetic clamping unit and the details of the substrate and mask holder engagement mechanism. The substrate holder is supported by four springs (A) on the substrate fixture. The mask holders sit on the mask holder fixture. The mask has been prealigned and physically clamped to the mask holder. The actual process operates as follows:

- (1) The substrate is held firmly between pins and spring clamps on the substrate holder and faces downward toward the mask.
- (2) The substrate conveyor is brought to the correct location ( $\pm 0.030$ ") so that the substrate holder is in line with the desired mask holder.
- (3) The substrate holder is then pushed down by the actuator. Because of the action of Spring B, the substrate goes down in contact with the mask while the magnet is still  $1/4$ " away from the back of the substrate glass.
- (4) The actuator continues to press downward until the four Springs B are completely compressed and the magnet is very close or contacting the back of the substrate and pulling up the mask against the substrate.

When the particular deposition is finished, the actuator is slowly released. The four Springs A and four B are thereby released of their tension. The magnet is separated from the substrate because of Springs B and the weight of the substrate holder. This prevents the damaging pull-up on the mask while releasing the substrate holder.

The resistance heating source station, used for cadmium selenide in transistor patterning, is flange mounted in a deep well position to allow adequate source to substrate spacing. The resistance element supports are the copper conductors. One is grounded and the other is mounted on a high water-cooled feedthrough. The resistance heater is clamped to adjustable blocks mounted to the conductors. A

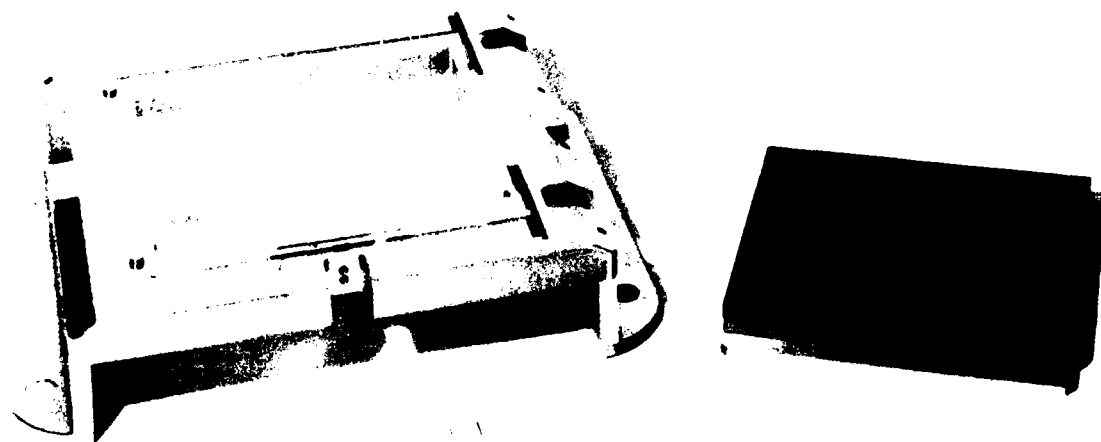


Figure 5.4 The magnetic clamping fixture.

shutter mechanism is mounted to the grounded conductor. It consists of two split plates which are pneumatically actuated. The de-energized position is closed and used during source conditioning, prior to deposition. The station derives power from a 2 kVA low voltage source reading a 0 to -9 VDC signal input for 0 to 95% control of power supply output, compatible with the control circuitry in Sloan's SL 1800 Series deposition control systems. The two electron beam gun wells are 7" x 14" x 22'4" deep with Viton o-ring gasket sealed doors for easy access and service. Each houses a Temescal Model TFE-180 four-position electron beam 270° focus gun. The four-crucible hearth wheels are driven by AC gear motors with internal breaking. Three of the crucibles in each assembly are shielded while the fourth is being accessed by the beam, in order to avoid cross contamination. Hearth position is registered through a chain-driven cam from the hearth drive shaft with three switches to give a binary count readout.

One of the electron beam guns has a (remotely adjustable) fixed beam and is used for metals. The other, used for aluminum oxide evaporation, has a swept beam. Evaporation rates and thickness are controlled by a programmable Sloan rate monitor. Evaporant flow to the substrate is regulated by electrically operated air-driven trap door shutters placed over each source.

The control panel is a human-engineered combination control and display panel. It permits complete push-button control of all tooling, pumping and valving, and deposition. It is used as the man-machine interface to the computer to permit process "recipe" generation. It displays computer commands to the system and the system's response to those commands during computer operation. Also, it permits human intervention in case of a malfunction or if an unforeseen change in operation is required at run-time.

The control computer is a 16 bit mini with 32K words of core, a 5-megabyte fixed and 5-megabyte removable disc, digital and analog process control interface equipment, a real-time disc-swapping executive with file manager software. All programs are written in Fortran IV.

### 5.3 Consideration of Processing Recipe Formulation

The processing recipe is used to execute the main vacuum system program. The substrate and recipe number to be used is selected by the operator and the sequence of events is started. The substrate and first mask is placed over the proper evaporation hearth at the direction of the computer. The density of the material to be evaporated, the rise power, soak power, evaporation rate and thickness is fed into the Sloan evaporation monitor by the computer and evaporation sequence is started. When the material is evaporating at the desired rate the shutter is opened for the length of time required to deposit the material on the substrate through the mask and the processing data is recorded. With the closing of the shutter the program proceeds to the next step. The processing recipe can be started or stopped at any step number in the recipe. Recipes are stored in the computer disc memory and executed identically every time. Figure 5.5 shows a 30-step recipe using the new mask design with nickel interconnect bus bar. The column headings in the figure refer to the following data.

- |           |  |
|-----------|--|
| 1. LYR    | Step number of the thin film layer to be formed                              |
| 2. STA    | Evaporation station (EB electron beam gun)<br>(RES resistance heated source) |
| 3. H      | Hearth   |
| 4. M      | Mask position number   |
| 5. GNTF   | Setting for evaporation monitor  |
| 6. DENS   | Density setting for evaporation monitor                                      |
| 7. RP/RT  | Rise power and rise time for evaporation process                             |
| 8. SP/ST  | Soak power and soak time   |
| 9. RATE   | Evaporation rate in angstroms per second                                     |
| 10. THK1  | Material to be evaporated before opening shutter                             |
| 11. THK2  | Total material to be evaporated  |
| 12. PRESS | Desired pressure   |
| 13. MATL  | Material (Al alumina)<br>(Cs cadmium selenide)                               |
| 14. MASK  | Mask name  |

RECIPE ID = RM4022

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GND-HIC1
2	EB2	2	3	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GATECAPG
3	EB2	2	2	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	HIC2VIC1
4	FMA	0	2	3100	8.90	22/1.0	28/1	5	300	1300	6.0X8	MT	HIC2VIC1
5	EB1	2	4	4100	4.00	50/1.0	50/1	20	300	5800	6.0X5	AD	INSULATR
6	EB1	2	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	AD	INSULATR
7	FMA	0	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	MT	INSULATR
8	FMA	0	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	MT	INSULATR
9	FMA	0	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	MT	INSULATR
10	EB2	2	6	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	VIC2TFIC
11	EB2	2	7	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	ELMIDCAP
12	RES	0	8	4100	5.80	30/1.0	32/5	4	350	450	6.0X8	CS	LCPWSEMI
13	RES	0	9	4100	5.80	30/1.0	32/5	4	300	350	6.0X8	CS	POWRSEMI
14	EB2	4	9	2100	2.40	19/1.5	22/1	40	3000	3000	6.0X8	IN	POWRSEMI
15	EB2	4	9	4100	2.40	19/1.5	22/1	10	1000	1000	6.0X8	IN	POWRSEMI
16	EB2	4	9	4100	2.40	19/1.5	28/1	1	200	200	6.0X8	IN	POWRSEMI
17	EB2	4	5	4100	7.30	19/1.5	28/1	2	300	600	6.0X8	IN	SO/DRAIN
18	EB2	3	5	4100	19.30	22/1.5	28/1	5	300	1300	6.0X8	AU	SO/DRAIN
19	EB1	2	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	AD	INSULATR
20	EB1	2	4	4100	4.00	55/1.0	65/1	20	300	5800	6.0X5	AD	INSULATR
21	FMA	0	4	4100	4.00	55/1.0	65/1	5	300	5800	6.0X8	MT	INSULATR
22	FMA	0	4	4100	4.00	55/1.0	65/1	5	300	5800	6.0X8	MT	INSULATR
23	FMA	0	4	4100	4.00	55/1.0	65/1	5	300	5800	6.0X8	MT	INSULATR
24	EB2	2	3	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GATECAPG
25	EB2	2	11	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GND-HIC1
26	EB2	2	12	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	HIC2VIC1
27	EB1	2	4	4100	4.00	55/1.0	65/1	20	300	3300	6.0X5	AD	INSULATR
28	FMA	0	4	4100	4.00	55/1.0	65/1	20	300	3300	6.0X8	MT	INSULATR
29	EB2	2	10	3100	8.90	22/1.0	28/1	5	300	1300	6.0X8	NI	EDGECONS
30	EB2	3	10	3100	19.30	22/1.5	28/1	5	300	900	6.0X8	AU	EDGECONS

Figure 5.5



There are several kinds of recipes used in the production of a DMD panel. They are Exercise, Precoat, Preheat, and Processing. The Exercise recipe is used to check the operation of the mask, substrate and actuator wheels. It directs the specified substrate to go through all of the motions it will be required to go through in the actual processing recipe without actual depositions. This can be done before actual pumpdown so as to save time, should some mechanical defect exist. All other recipes require a vacuum. The Precoat recipe is used to coat all the masks with aluminum for ease in cleaning the masks after a period of use. The Preheat recipe prepares all the Hearths that will be used in the processing recipe by premelting the various materials to be deposited. This also tends to cover the walls of the chamber and trap any moisture. This has proved very beneficial in preventing cracked insulators due to moisture settling on the substrate prior to  $\text{Al}_2\text{O}_3$  deposition. It is believed that the trapped moisture cracked the insulators during heat treatment of the substrate. Hearths 1 to 4 in EB Gun #1 is used exclusively for  $\text{Al}_2\text{O}_3$ . Hearths 1 to 4 EB Gun #2 is reserved for metals Al, Ni, Au, and In. CdSe is evaporated from a resistance heater (Res).

The formulation of the processing recipe can be very complex. Each step can have an effect on the previous steps or the following steps. In an attempt to illustrate this, three recipes will be used. Figure 5.7 is the recipe which uses the aluminum copper and chrome and old mask d-sign, Figure 5.5 uses the new mask design with nickel, and Figure 5.6 is the recipe with the new mask design with nickel, as well as recipe considerations to reduce the step count.

One can visualize the transistors and circuit of the DMD panel as three basic layers separated by insulators. The bottom layer is the bottom gate, capacitor plate and interconnect busbars. The middle layer includes the source drains, semiconductors middle capacitor plate and additional interconnects between layers. The top layer is the top gate, capacitor plate and interconnects between layers and additional busbars. Referring to Figure 5.5, steps 1 through 4 constitutes the bottom layer composed of horizontal interconnect masks #1 and #2 and gate mask #3. The mask number is the same as the mask wheel position

RECIPE ID = RM4042

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GND-HIC1
2	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GATECAPG
3	EB2	2	2	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	HIC2VIC1
4	EB1	2	4	4100	4.00	50/1.0	50/1.1	20	300	5800	6.0X5	AD	INSULATR
5	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AD	INSULATR
6	EB2	2	6	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	VIC2TFIC
7	EB2	2	9	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	POWRSEMI
8	EB2	2	7	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	ELMIDCAP
9	EB2	4	8	2100	2.40	19/1.5	22/1.1	40	3000	3000	6.0X8	IN	LGPWSEMI
10	EB2	4	8	4100	2.40	19/1.5	22/1.1	10	1000	1000	6.0X8	IN	LGPWSEMI
11	EB2	4	8	4100	2.40	19/1.5	22/1.1	1	200	200	6.0X8	IN	LGPWSEMI
12	EB2	4	5	4100	7.30	19/1.5	22/1.1	2	300	600	6.0X8	IN	SO/DRAIN
13	EB2	3	5	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	SO/DRAIN
14	RES	0	8	4100	5.80	30/1.0	32/1.5	4	350	500	6.0X8	CS	LGPWSEMI
15	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AD	INSULATR
16	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AD	INSULATR
17	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GATECAPG
18	EB2	2	11	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GND-HIC1
19	EB2	2	12	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	HIC2VIC1
20	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	3300	6.0X5	AD	INSULATR
21	EB2	1	10	4100	8.90	20/1.0	28/1.2	5	300	600	6.0X8	AL	EDGECONS
22	EB2	3	10	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	EDGECONS

Figure 5.6

RECIPE ID = RM3273

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	9	3100	2.70	18/1.0	25/1.1	5	500	1100	6.0X8	NI	POURSEMI
2	EB2	2	1	3100	2.70	18/1.0	25/1.1	5	300	1300	6.0X8	NI	GND-HIC1
3	EB2	1	8	4100	8.90	20/1.0	28/1.2	5	300	1000	6.0X8	AL	LGPWSEMI
4	FMA	0	1	3100	2.70	22/1.0	28/1.2	5	300	1500	6.0X8	MT	GND-HIC1
5	EB1	3	3	4100	4.00	50/2.0	50/1.1	20	300	6300	6.0X5	AO	GATECAPG
6	FMA	0	3	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	GATECAPG
7	FMA	0	3	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	GATECAPG
8	EB2	2	2	3100	2.70	18/1.0	25/1.1	5	300	900	6.0X8	NI	HIC2VIC1
9	FMA	0	10	3100	2.70	22/1.0	28/1.2	5	300	900	6.0X8	MT	EDGECONS
10	EB1	3	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
11	EB1	3	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
12	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
13	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
14	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
15	RES	0	6	4100	5.80	35/1.0	35/1.5	4	300	450	6.0X8	CS	VIC2TFIC
16	RES	0	12	4100	5.80	35/1.0	35/1.5	4	300	450	6.0X8	CS	HIC2VIC1
17	EB2	4	12	2100	2.40	19/1.5	22/1.1	40	3000	3000	6.0X8	IN	HIC2VIC1
18	EB2	4	12	4100	2.40	19/1.5	22/1.1	10	1000	1000	6.0X8	IN	HIC2VIC1
19	EB2	4	12	4100	2.40	19/1.5	22/1.1	1	200	200	6.0X8	IN	HIC2VIC1
20	EB2	4	5	4100	7.30	19/1.5	22/1.1	2	300	600	6.0X8	IN	SO/DRAIN
21	EB2	3	5	4100	10.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	SO/DRAIN
22	EB2	1	8	4100	8.90	20/1.0	28/1.1	5	300	1300	6.0X8	AL	LGPWSEMI
23	FMA	0	8	4100	8.90	20/1.0	28/1.1	5	300	1300	6.0X8	MT	LGPWSEMI
24	EB1	3	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
25	EB1	3	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
26	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
27	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
28	EB2	2	2	3100	2.70	18/1.0	25/1.1	5	300	900	6.0X8	NI	HIC2VIC1
29	EB2	2	7	3100	2.70	18/1.0	25/1.1	5	300	1300	6.0X8	NI	ELMIDCAP
30	EB2	1	8	4100	8.90	20/1.0	28/1.2	5	300	1000	6.0X8	AL	LGPWSEMI
31	FMA	0	2	3100	2.70	22/1.0	28/1.2	5	300	900	6.0X8	MT	HIC2VIC1
32	EB1	3	3	4100	4.00	55/1.0	65/1.1	20	300	6300	6.0X5	AO	GATECAPG
33	FMA	0	3	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	GATECAPG
34	EB2	2	10	3100	2.70	18/1.0	25/1.1	10	300	900	6.0X8	NI	EDGECONS
35	EB2	2	7	3100	2.70	18/1.0	25/1.1	10	300	1300	6.0X8	NI	ELMIDCAP
36	EB2	2	9	3100	2.70	18/1.0	25/1.1	10	300	900	6.0X8	NI	POURSEMI
37	EB2	1	9	4100	8.90	20/1.0	28/1.2	5	300	1000	6.0X8	AL	LGPWSEMI
38	EB1	3	4	4100	4.00	55/1.0	65/1.1	20	300	2300	6.0X5	AO	INSULATR
39	EB1	3	8	4100	4.00	55/1.0	65/1.1	5	300	500	6.0X8	AO	LGPWSEMI

Figure 5.7

number. Step 4 is a three-minute pause step indicated by the term FMA in the evaporation station column. Steps 5 through 9 is the bottom gate insulator delineated by mask #4 which includes three pause steps of three minutes each. Steps 10 through 18 is the middle layer composed of vertical interconnect masks #6 and #7, semiconductor mask #8 and #9 and source drain mask #5. Steps 19 through 23 is the top gate insulator delineated by mask #4 and includes three more pause steps of three minutes each. Finally, Steps 24 through 30 complete the recipe with the top layer which is composed of the top gate mask #3, redundant interconnect masks #1 and #2 in mask wheel position #11 and #12, cover insulator mask #4 with a three-minute pause step and edge contact mask #10.

Mask #1 and #2 are the horizontal interconnect masks and are in the mask wheel position #1 and #2. Copies of masks #1 and #2 are also in mask wheel position #11 and #12 and are deposited redundantly on the substrate, and as a result we have a very low open count on the horizontal bus bars. We do not have available an extra mask wheel position for the vertical interconnect mask #6, and as a result the vertical bus bar open count is much higher. One way to provide room for a redundant vertical interconnect mask #6 would be to eliminate mask #9 power semiconductor. Mask #9 adds to the semiconductor thickness and doping of the power semiconductor. The logic and power transistor would have the same recipe. This was tried and the logic transistor had a larger negative threshold gate voltage which was reasonable. Note that there are eight pause steps for a total of 24 minutes. These pause steps are a holdover from the old mask set recipe where aluminum bus bars were used (see Figure 5.7). Note that there is a pause step prior to the evaporation of  $\text{Al}_2\text{O}_3$  at 20 Å/sec rate which required  $\text{O}_2$  in the vacuum chamber. The reason for this pause step is to allow some time for cooling the substrate to prevent oxidation of the Al bus bar deposition of the previous step. Note also that additional pause steps after the  $\text{Al}_2\text{O}_3$  deposition are needed to cool the substrate and clear the vacuum chamber of  $\text{O}_2$ . This is very important prior to the semiconductor (CdSe) deposition.

With the discussion of the redundant masks and the pause steps (see 22 step recipe, Figure 5.6), note that all the pause steps have been removed because we no longer have the aluminum oxidation problem with nickel. We resolved the possible  $O_2$  problem by depositing the semiconductor through mask #8 for both logic and power transistors nine steps after the insulator  $Al_2O_3$  was deposited with  $O_2$ . Doping with indium is also done through mask #8. Mask wheel position #9 now contains a redundant mask #6 which improves the vertical bus bar open count. With this 22 step recipe (Figure 5.6) the run time was reduced to 65 minutes compared to 90 minutes with the 30-step recipe (Figure 5.5) with a larger negative threshold voltage on the logic transistor, but a lower open count for the vertical bus bars. Steps 9 and 10 (see Figure 5.6) prepares the indium for deposition onto the semiconductor in the source-drain gap through mask #8 by boiling off the impurities onto the shutter at a comparatively high rate. In step 11 the indium continues to be evaporated onto the shutter at approximately  $.33 \text{ \AA}/\text{sec}$  until a uniform rate is achieved for three consecutive readouts when the shutter is opened for six seconds timed by the computer for a total deposition thickness of approximately  $2 \text{ \AA}$ . The rate of  $.33 \text{ \AA}/\text{sec}$  is achieved by setting the density of indium at 2.4 instead of its normal 7.3. Step 12 evaporates the indium at a rate of  $2 \text{ \AA}/\text{sec}$  onto the source-drain through mask #5. The source-drain is completed by the evaporation of Au through mask #5.

Indium is used as an adhesive layer for the Au source-drain; however, it does play an important part in setting threshold voltage of the transistor. Indium added directly onto the semiconductor in the source-drain gap (doping the gap) at the proper CdSe In ratio can improve the stability and grain considerably.

#### 5.4 Throughput, Yield and Test Results

Data relating to circuit production using materials and techniques described in previous sections are discussed here within the separate frameworks of program phases II (May 1978 to October 1978) and III (October 1978 to July 1979). The chief difference in the two approaches relates to revised mask design and substitution of nickel for aluminum and copper in the synthesis of the busbar complex of the display circuits.

##### 5.4.1 Results Achieved in Phase II

In review, Phase II was structured as a six-month period immediately following the installation of Class 100 clean conditions in the substrate and mask preparation areas and the vacuum system environment. Mask design and deposition process were initially largely the same as those employed in Phase I when the technology was first transferred from the laboratory-scale "XY" approach, previously illustrated in Figures 1.10 and 1.11, to the pilot production facility with dedicated masks. The somewhat complex cell layout of this era is shown in Figure 5.8. It is substantially a dedicated mask facsimile of the pattern used in Phase I which was generated by variable aperture X-Y masking. The pattern shown in Figure 5.8 required full twelve masks for its synthesis and featured aluminum, chrome, copper, gold and indium metallic layers as well as the cadmium selenide semiconductor in the manner shown in Figure 5.9.

As noted earlier, the automatic vacuum deposition system was shut down for renovation to the pilot facility during much of the earlier part of Phase II. Much subsequent time was consumed by start-up problems and equipment malfunctions notably repeated premature monitoring crystal failure. Backup sensors with shutter mechanisms were installed; throughput per run increased from typically two to four circuits per month. Many were defective because of mask misregistration and human error. However, the remainder were packaged for evaluation in qualitative viewability testing.

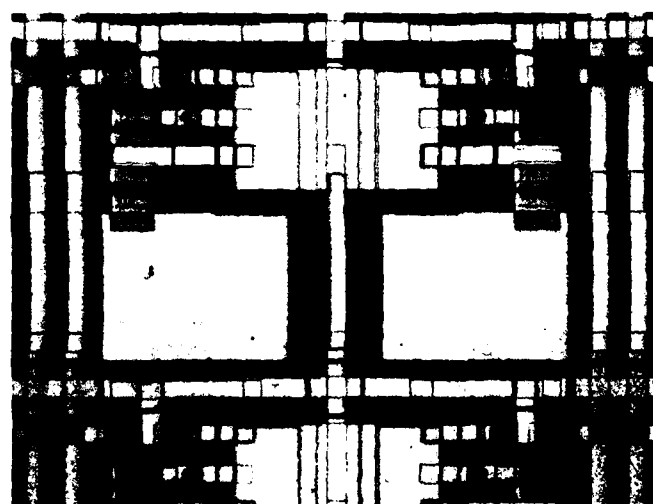
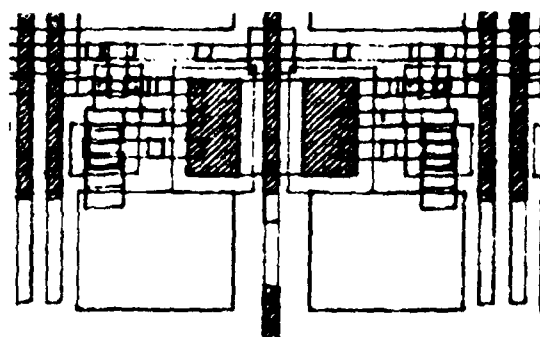


Figure 5.8 The layout featured in Phase II.

Typically less than half of the 128 character array was recognizable. The illegible characters were caused by both transistor and interconnect problems.

The general location of defective busbars correlated with mapping printouts generated by the automatic circuit tester described in Section 6.3, although it was later realized that this testing operation itself was responsible for creating its own defects.

An abnormally large number of open busbars was traced to defective mask apertures in a newly acquired set of masks. This means a replacement set of the beryllium-copper cored version, featuring the then existing pattern design consistent with Figures 5.8 and 5.9. During regorous re-inspection of these busbar masks, more than fifty apertures were found with microscopically small diameter nickel fibers extending from one side of an aperture to another. After detection and removal, character legibility significantly improved. An example is shown in Figure 5.10.



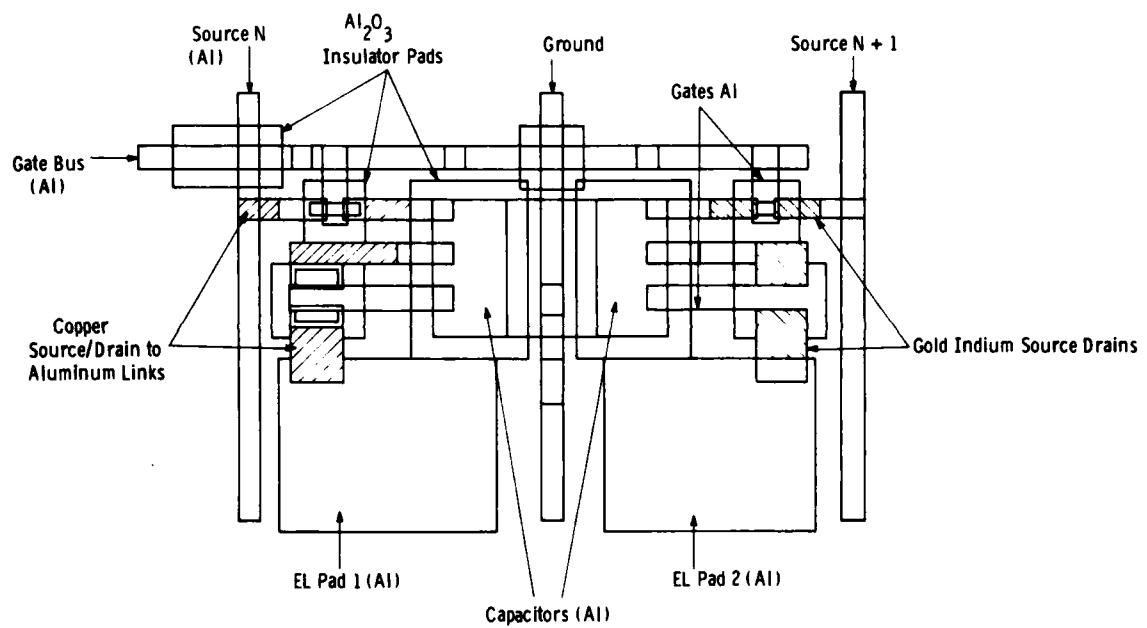


Fig. 5.4.2 - Materials used in the fabrication of the Phase II pattern

Figure 5.9 Materials used in the fabrication of the Phase II Pattern.

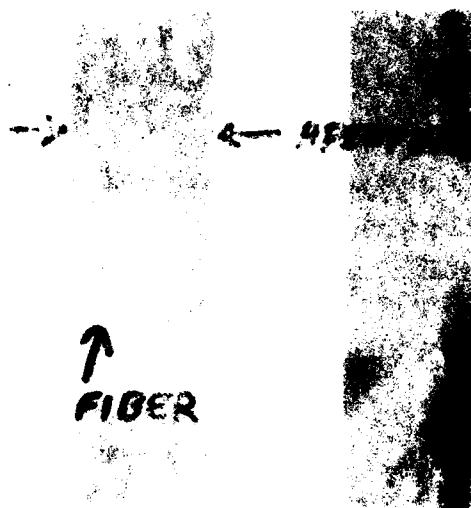


Figure 5.10 Example of nickel fiber spanning busbar mask aperture causing open circuits.

Curve tracer measurements generally showed that both the power and logic transistor characteristics were within specifications believed necessary at that time to provide a functional display. There was one major exception. The power transistors exhibited a tendency wherein their gain "collapsed" spectacularly under moderately hard drive conditions associated with minimally acceptable excitation of the phosphor dots. The collapse time constant was typically of the order of one second and the phenomenon was generally irreversible, providing large areas of the display which could not subsequently be illuminated. A model of the physics of this phenomena is offered in Section 2.4.1. Here we will describe how the problem was resolved on an empirical basis after first discussing other concurrent process development activities.

Some experiments were carried out with pre-doped cadmium selenide to improve repeatability of the transistor doping process. The experiments appeared successful in that transistors with adequate characteristics were fabricated with the pre-doped material. Unfortunately, it was found that preferred evaporation of the indium dopant occurred. Consequently, only one set of transistors could be deposited with each charge of material. As a result, the technique did not appear feasible for pilot production because of down time rendered necessary by breaking vacuum to replace the pre-doped source.

As soon as the circuit production rate was raised to four pieces per pump down, it became necessary to train a team of technicians to handle the increased volume. This was because the automatic prober systematically mutilated the circuits under test. The principle problem was the destruction of metal layers caused by probe overtravel. In addition, failures were being caused electrically when power transistors shorted under high voltage. New probes with .003" vs. .007" overtravel were evaluated but subsequent testing indicated that only very marginal improvement could be thereby obtained. It was concluded that flatter glass substrates were necessary to resolve the problem, and later (during Phase III), automatic testing with its full original

scope was abandoned altogether because we couldn't obtain such glass in sufficient quantities at a reasonable price.

The origins of other busbar defects created during and after deposition could be traced to the following:

- (1) Fine line scratches in the soft aluminum busbars exemplified in Figure 5.11.
- (2) Fibers and other debris transferred to substrates from the mask surfaces. These particulates probably originated in improper cleaning of mask apertures between runs and from in-process peeling of material accumulated on the relief sides of the masks. A typical result is shown in Figure 5.12.
- (3) A rather puzzling defect type was classified and called "Rabbit Tracks" due to their appearance (illustrated in Figure 5.13). They are believed to have originated from sliding contact between a mask and a previously deposited aluminum pattern, occurring during engagement and disengagement of the mask and substrate under conditions of magnetic pull up.

In spite of all these difficulties, analysis strongly indicated that the high incidence of open busbars was due to manageable causes. In many cases, they were repaired manually with small dots of conductive epoxy prior to phosphor application. The operation required substantial operator skill and time and was subject to occasional periods of poor reliability. Repaired connections sometimes reopened and/or rendered difficult making contact between the aluminum busbar and the epoxy. This originated in failure to properly burnish the aluminum surface in order to remove the oxide skin. The former could have resulted from improper proportions or insufficient mixing of the components of the conductive epoxy.

Initial counts of transistor, capacitor and crossover shorts were concurrently reduced to a fairly low level of between four and ten per circuit. However, these assessments may have been distorted

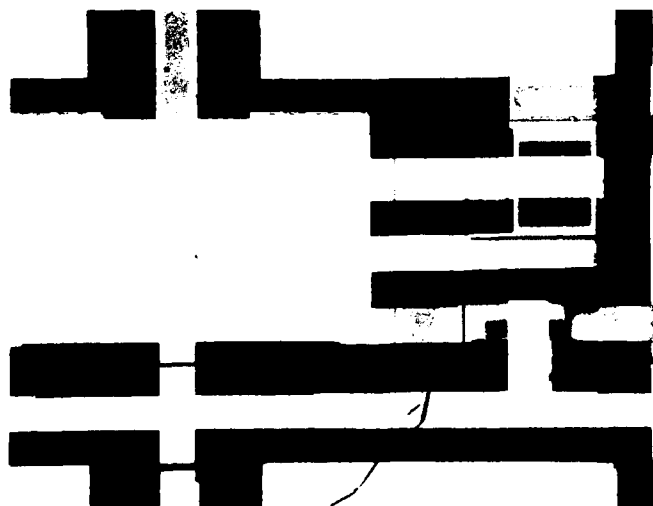


Figure 5.11 Open busbars caused by scratching during post-process handling.

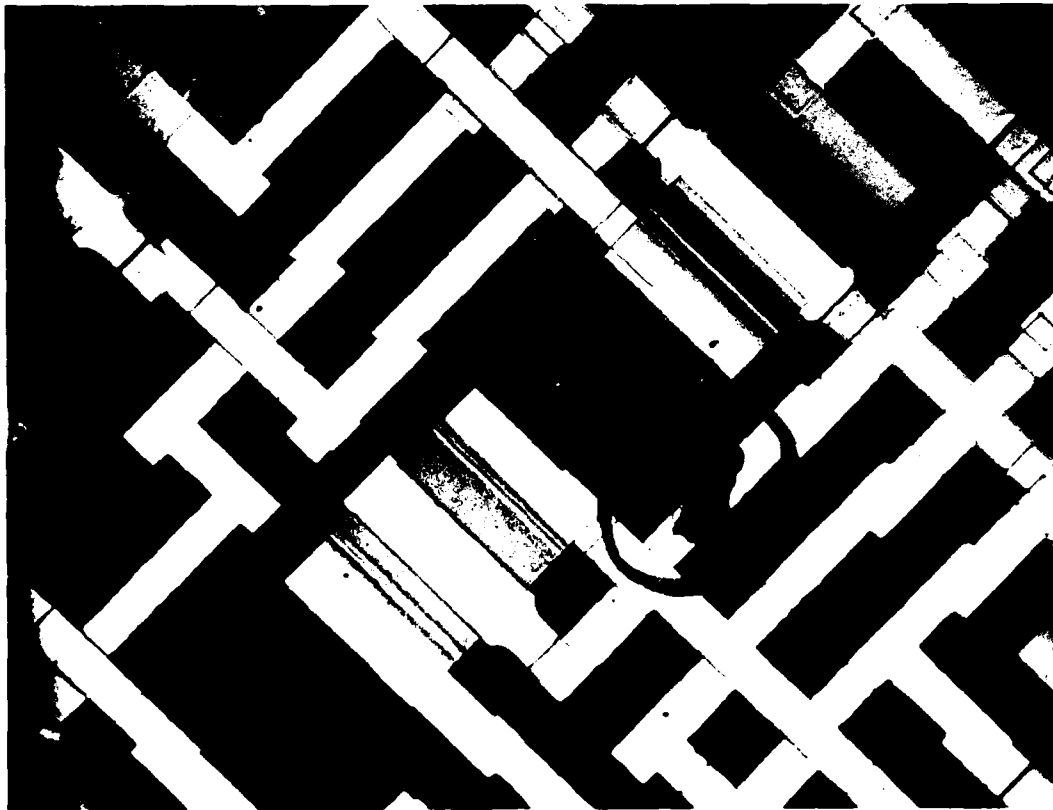


Figure 5.12      Open busbar believed due to loose flake of material of undetermined origin resting on a mask thereby blocking an aperture.

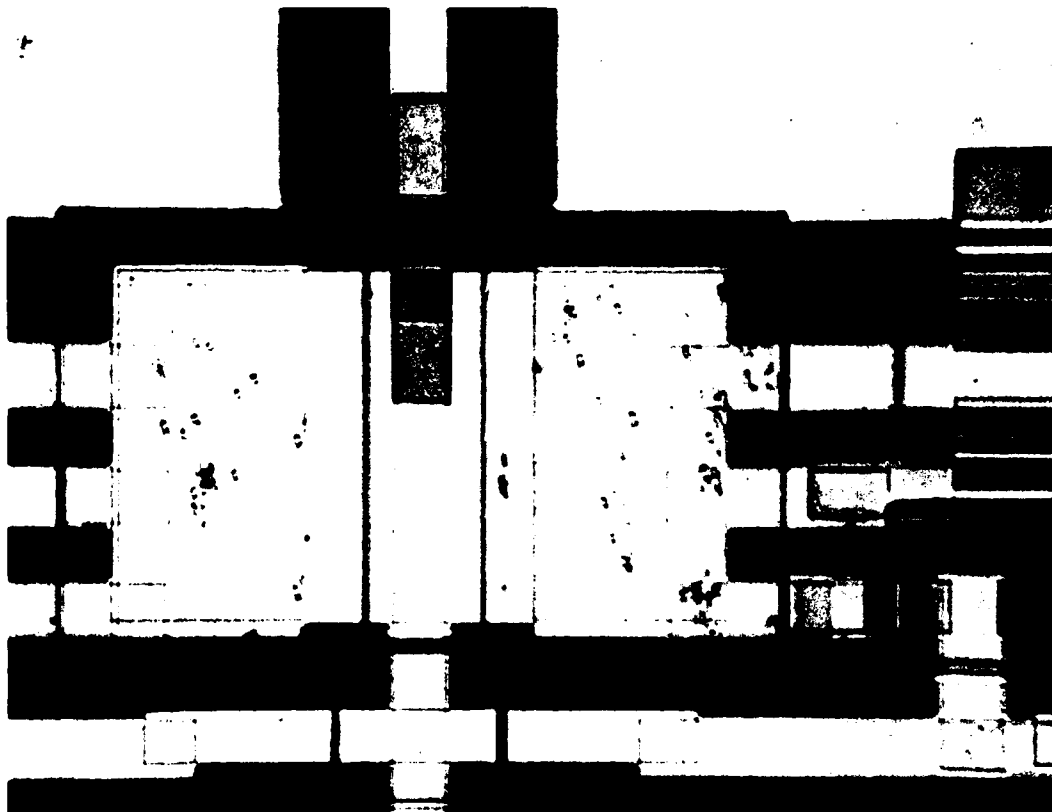


Figure 5.13 "Rabbit Track" defects affecting metal capacitor plates.

downward due to the simultaneous existence of busbar opens, the total short count not becoming evident until all busbar opens are reconnected. In any event, the short count typically increased as the time after the previous mask cleaning. In addition, residual particulates were tended to become lodged in mask apertures as a result of insufficient cleaning and rinsing.

A majority of shorts examined revealed a small dark spot under a crossover. An example is shown in Figure 5.14. Illustration (a) shows such a dark speck several microns in diameter; (b) shows the same area after clearing with a voltage pulse and (c) shows the same area again with a scanning electron microscope image.

Even in the face of all these difficulties, a dozen or so circuits were readied for preliminary viewability testing. The details of the Phase II phosphor application technique and its shortcomings are discussed fully in Section 7.2. Testing was accomplished by mounting the half panel in a special test fixture that provided electrical connection to individual source busbars, the top gold transparent electrode and a ground line. The fixture was connected to an exerciser that provided an adjustable 5 kHz AC drive voltage, source and gate bias voltages and a keyboard to enter alphanumeric characters at the 128 locations on a half panel. This fixture, however, gauged each corresponding dot row of each character row in parallel so that independent entry on each character row was not possible and defects such as shorts tended to "propagate" up each column of characters.

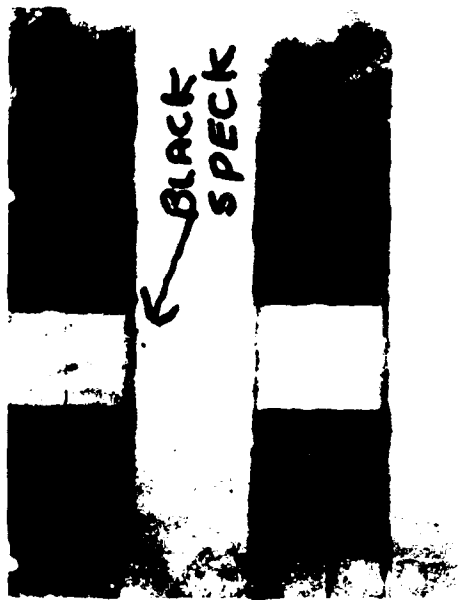
During such tests, even at very low levels of phosphor excitation with low AC voltages, and viewing in a dark ambient, supposedly defect free circuits failed to perform commensurably.

A typical test sequence involved a series of legibility tests during which time final repairs were made. The effects of open busbars or shorts not detected during initial circuit repair could be seen when the character array was displayed. Open busbars were reconnected by probing through the phosphor layer and making connection with

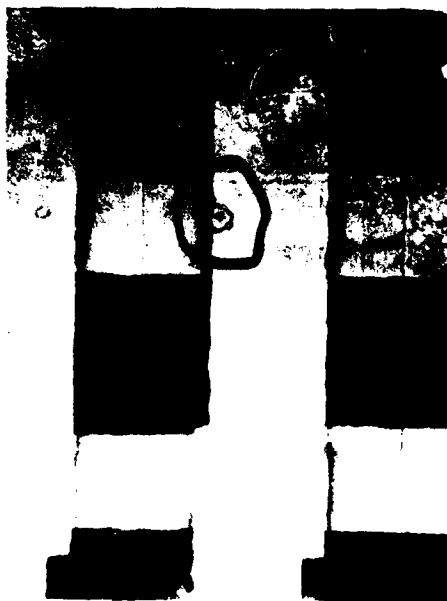


conductive epoxy. Shorts were sometimes cleared with voltage pulses. When this was not possible, the shorted device was disconnected from the circuit matrix resulting in a single elemental defect, that is, an unmodulated element. Twenty-five percent of the panels registered legibilities greater than 90%. This level of performance was achieved only as a result of a labor-intensive post phosphor repair process. The panel shown in Figure 5.14 represents the best level of quality achieved. Other panels would have required more extensive repairs to match this performance. The higher level of defects was determined to be due primarily to one or more of the following:

- (1) Marginal reliability of the epoxy repairs made prior to phosphor application as previously discussed.
- (2) Scratched busbars from handling during phosphor processing. Due to Riston laminating problems, some panels were recoated which required extra handling and removal of the first Riston layer.
- (3) Damaged or scratched contact pads. This effect has frequently been observed when the panel is inserted several times into the test fixture. The pad metallization consisted at that time of an aluminum, copper and gold multi-layer. This metal combination often exhibited poor adherence and scratch resistance.
- (4) Interface corrosion at the pad-aluminum busbar connection. It was frequently observed that this joint area could be electrically open after application of voltage and current due to a thinning of the aluminum as a consequence of diffusion into the pad metal during annealing. This effect was not observed at aluminum-nichrome/gold interfaces as shown in Figure 5.15.
- (5) Occurrence of areas in the panel that could not be modulated and remained permanently dark. The effect on panel legibility is shown in Figure 5.16. The source of the problem was traced to poorly defined insulator patterns in localized areas of the panel. These insulator film segments spread sufficiently under the mask



(a) Shorted Busbar Crossover  
(before cleaning)

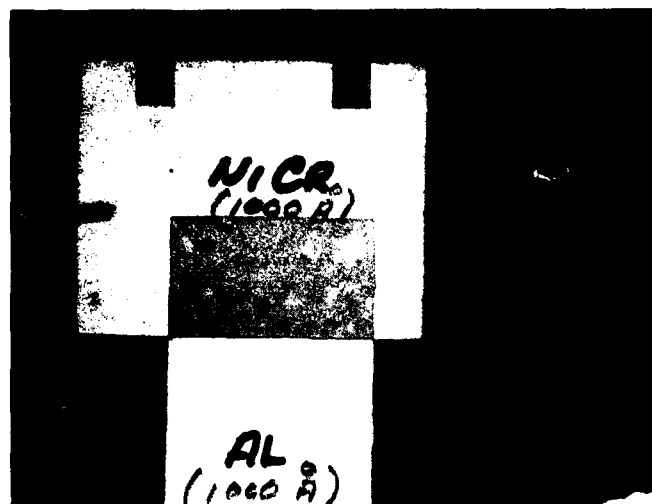


(b) Crossover after Clearing  
with Voltage Pulse



(c) Scanning Electron Microscope,  
Closeup of Cleared Area

Figure 5.14 A typical busbar crossover short before and after clearing.



Reflected Light



Transmitted Light

Figure 5.15 Aluminum/nichrome-gold interface showing no corrosion effects after annealing.

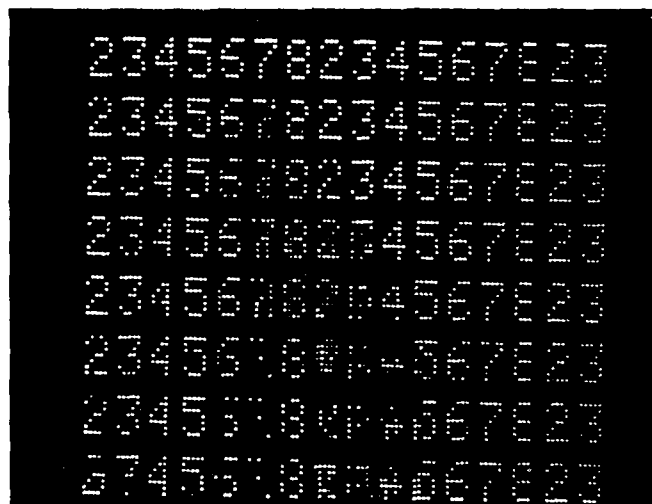
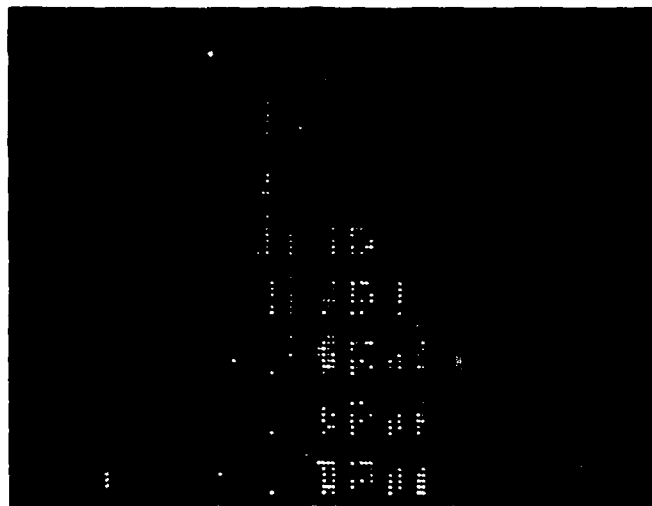


Figure 5.16 Panel legibility degradation due to contamination of unformed busbars with "Aluminum Underspray".

aperture to form a barrier at a connecting joint between the power transistor ground line or the logic transistor source connection. The same phenomenon was again observed occasionally later with the new Kovar masks, and was referred to as the "aluminum underspray" syndrome. The deposition sequence was analyzed and it appeared that the addition of several extra connecting metal layers between insulator steps helped to eliminate the barrier. However, the basic problem was related to local mask buckling or warpage and was not fully resolved until all-Kovar masks were used in Phase III.

During Phase II of the program, the most serious processing problem by far was identified as the "collapse" effect, mentioned previously. At the same time, a major triumph was systematic experimental investigations which resulted in its resolution, and paved the way for a transistor fabrication process which later proved quite capable of meeting the phosphor drive requirements. Phenomenologically, the effect is characterized by a rapid ( $< 1$  sec) dimming of a large number of lit elements as the phosphor excitation voltage is raised to about 300 volts peak-to-peak, which is typically required for viewing in subdued room light. An example is shown in Figure 5.17. Concurrent behavior at the device level is shown in Figure 5.18.

The so-called "standard" recipe being used before the collapse problem was resolved is shown in Figure 5.19. The reader is referred to Section 5.3 for a discussion and interpretation of recipe format. Previous experience and the theoretical model discussed in Section 2.4.1 indicated that the immediate cause of the problem related to the stoichiometry of the aluminum oxide gate insulator films. Indirectly, the conductivity type of the n-channel transistors was affected and consequently their threshold voltages. In Figure 5.20 we observe that the critical gate insulator depositions in steps 9 and 19 were uniquely executed in an oxygen partial pressure of  $6 \times 10^{-5}$  torr. Total oxide thickness was  $6000\text{\AA}$  and was then deposited at  $5\text{\AA}/\text{sec}$ . These numbers resulted directly from Program Phase I process development

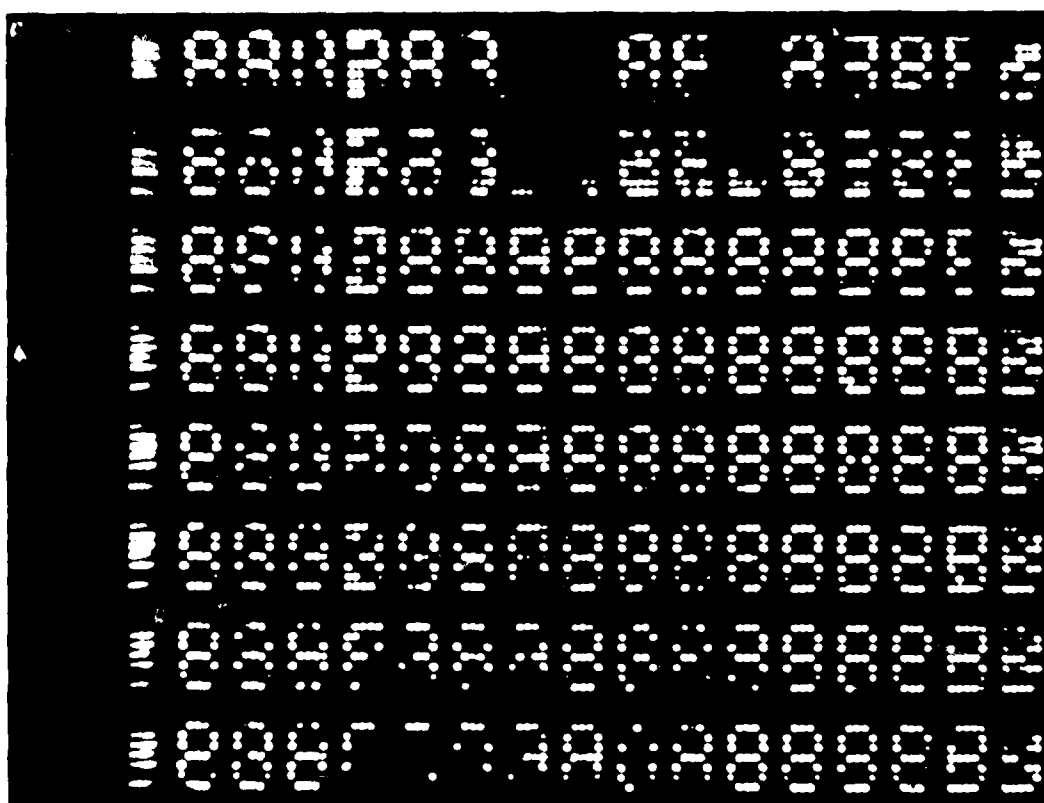
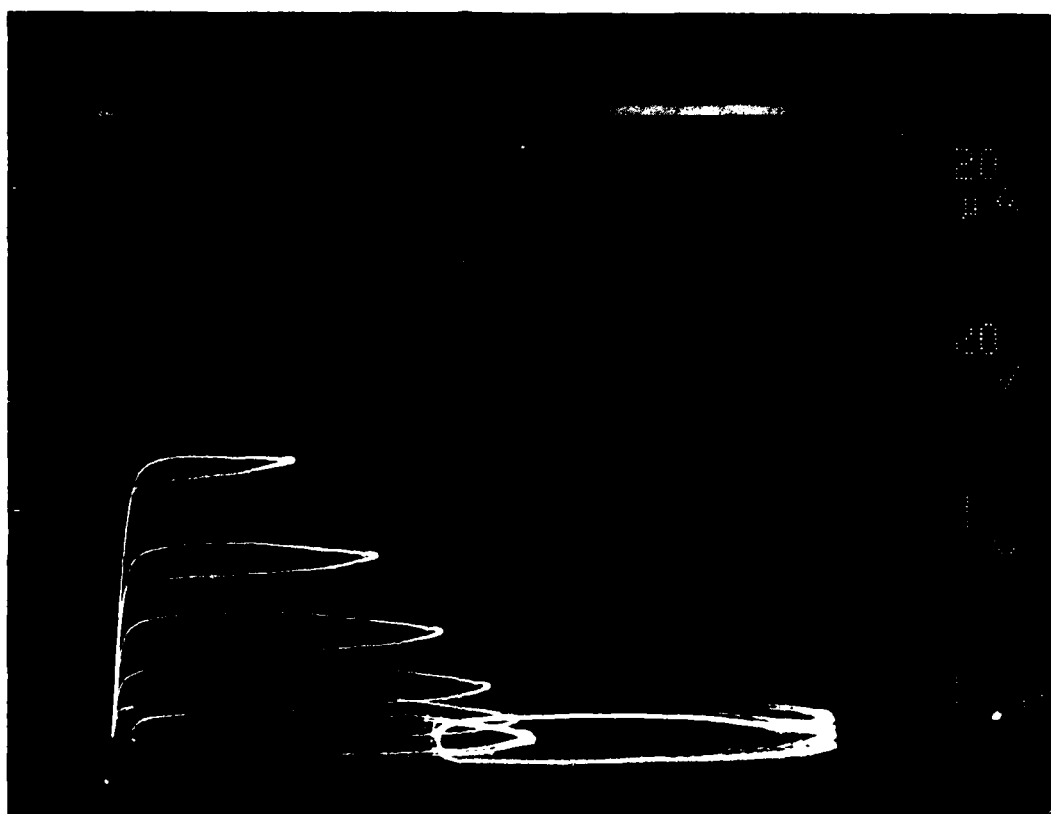


Figure 5.17 Poor legibility due to power transistor "collapse".



Left Side  
Power TFT in  
Normal Display  
Area

Right Side  
"Collapsed" Power  
TFT in Dark Area  
of Display

Figure 5.18 The collapse phenomenon at the device level; source-drain current-voltage characteristics before and after "collapse".

RECIPE ID = RM3171

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	9	3100	2.70	22/1.0	28/ .2	5	500	1100	6.0X8	AL	EL,HIC 2
2	EB2	2	1	3100	2.70	22/1.0	28/ .2	5	300	1300	6.0X8	AL	CG,HIC 1
3	EB2	1	8	4100	8.90	20/1.0	28/ .2	5	300	1000	6.0X8	CU	SD,CONT.
4	FNA	0	1	3100	2.70	22/1.0	28/ .2	5	300	1500	6.0X8	MT	CG,HIC 1
5	EB1	1	3	4100	4.00	50/2.0	50/ .1	5	300	6300	6.0X5	AD	CAP INS.
6	FNA	0	3	4100	4.00	45/1.0	60/ .1	5	300	6300	6.0X8	MT	CAP INS.
7	EB2	2	2	3100	2.70	22/1.0	28/ .2	5	300	900	6.0X8	AL	G, VIC 2
8	FNA	0	10	3100	2.70	22/1.0	28/ .2	5	300	900	6.0X8	MT	CT,VIC 3
9	EB1	1	4	4100	4.00	55/1.0	65/ .1	5	300	6300	6.0X5	AD	G,X INS.
10	FNA	0	4	4100	4.00	45/1.0	60/ .1	5	300	6300	6.0X8	MT	G,X INS.
11	FNA	0	4	4100	4.00	45/1.0	60/ .1	5	300	6300	6.0X8	MT	G,X INS.
12	FNA	0	4	4100	4.00	45/1.0	60/ .1	5	300	6300	6.0X8	MT	G,X INS.
13	RES	0	6	4100	5.80	35/1.0	35/ .5	4	300	450	6.0X8	CS	SEMICOND
14	EB2	4	12	4100	2.40	19/ .5	22/ .1	1	9999	9999	6.0X8	IN	DOPING
15	EB2	4	5	4100	7.30	19/ .5	22/ .1	2	9300	9600	6.0X8	IN	SD/DRAIN
16	EB2	3	5	4100	19.30	22/ .5	28/ .1	5	300	1300	6.0X8	AU	SD/DRAIN
17	EB2	1	8	4100	8.90	20/1.0	28/ .1	5	300	1300	6.0X8	CU	SD,CONT.
18	FNA	0	8	4100	8.90	20/1.0	28/ .1	5	300	1300	6.0X8	MT	SD,CONT.
19	EB1	1	4	4100	4.00	55/1.0	65/ .1	5	300	6300	6.0X5	AD	G,X INS.
20	FNA	0	4	4100	4.00	45/1.0	60/ .1	5	300	6300	6.0X8	MT	G,X INS.
21	EB2	2	2	3100	2.70	22/1.0	28/ .2	5	300	900	6.0X8	AL	G, VIC 2
22	EB2	2	7	3100	2.70	22/1.0	28/ .2	5	300	1300	6.0X8	AL	C, VIC 1
23	FNA	0	2	3100	2.70	22/1.0	28/ .2	5	300	900	6.0X8	MT	G, VIC 2
24	EB1	1	3	4100	4.00	55/1.0	65/ .1	5	300	6300	6.0X5	AD	CAP INS.
25	FNA	0	3	4100	4.00	45/1.0	60/ .1	5	300	6300	6.0X8	MT	CAP INS.
26	EB2	2	10	3100	2.70	22/1.0	28/ .2	10	300	900	6.0X8	AL	CT,VIC 3
27	EB2	2	7	3100	2.70	22/1.0	28/ .2	10	300	1300	6.0X8	AL	C, VIC 1
28	EB2	2	9	3100	2.70	22/1.0	28/ .2	10	300	900	6.0X8	AL	EL,HIC 2
29	EB2	2	11	3100	2.70	22/1.0	28/ .2	10	300	500	6.0X8	AL	EDGE CON
30	EB2	1	11	4100	8.90	24/ .5	30/ .1	.20	300	1800	6.0X8	CU	EDGE CON
31	EB2	3	11	3100	19.30	20/ .7	28/ .3	10	300	900	6.0X8	AU	EDGE CON
32	EB1	1	4	4100	4.00	55/1.0	65/ .1	10	300	2300	6.0X5	AD	G,X INS.
33	EB1	1	8	4100	4.00	55/1.0	65/ .1	5	300	500	6.0X8	AD	SD,CONT.

Figure 5.19 The "Standard Recipe" in use prior to the resolution.



effort and seemed at that time immediately transferable to the pilot facility automatic vacuum deposition equipment. In retrospect it appears that conventional process variables alone do not exclusively determine film quality and that vacuum system hardware configuration variations prevent uninterrupted transferability.

In any event, three experiments were successfully conducted to investigate the collapse phenomenon. All three focussed on varying the conditions under which the critical gate insulator films were deposited. Variables were the oxygen partial pressure, the rate of deposition, and the separation of the composite gate insulator into a single or composite layer of two components. The so-called double-layer configuration is illustrated in cross section in Figure 5.21 which identifies the so-called second layer of  $\text{Al}_2\text{O}_3$  as that adjacent to the semiconductor. The "standard" recipe responsible for producing collapse-prone transistors and shown in Figure 4.12 features only the second layer.

Process variations and transistor test data characterizing the first experiment are shown in Table 5.4.1. Conditions under which the measurements of 'ON current',  $I_{\text{ON}}$ , and leakage,  $I_{\text{O}}$ , are made are explained in Section 6.4. The so-called "200V test" being made during the collapse era was simply an assessment of whether the devices would sustain such a level for an arbitrary period of ten seconds or so. Vulnerability to collapse was determined by increasing this voltage while a complete "family" of conductance curves was being generated until several hundred volts was being switched repeatedly in a mode simulating phosphor drive.

In this first experiment, four substrates were fabricated in a single run. The first two substrates, 153-1 and 153-2, featured a standard recipe identical to that shown in Figure 5.19 except for the selection of aluminum oxide hearth. These were circuits complete with transistor interconnects and a full complement of busbars. The third and fourth substrates hosted only transistors, eliminating those steps

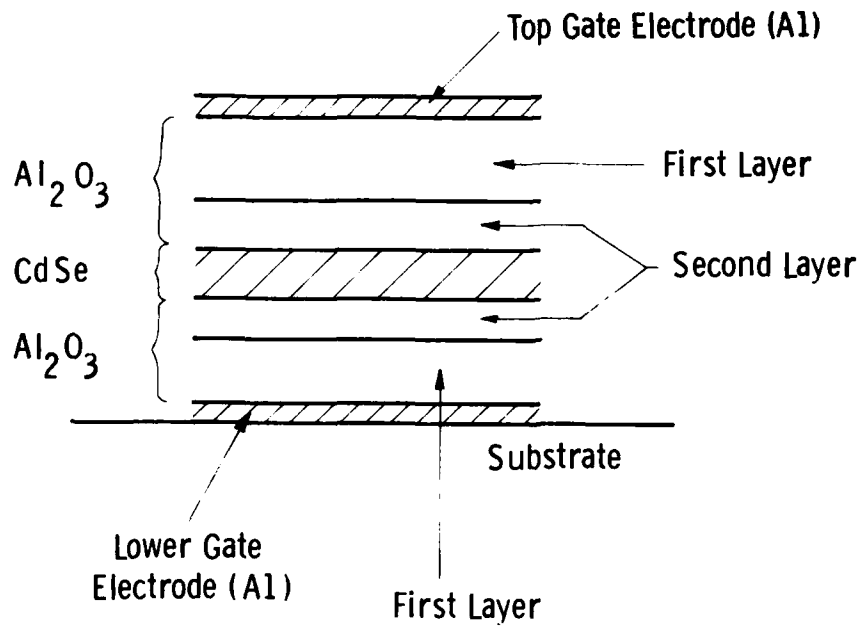


Figure 5.20 Cross section of the double layer gate insulator configuration.

Dwg. 7715A32

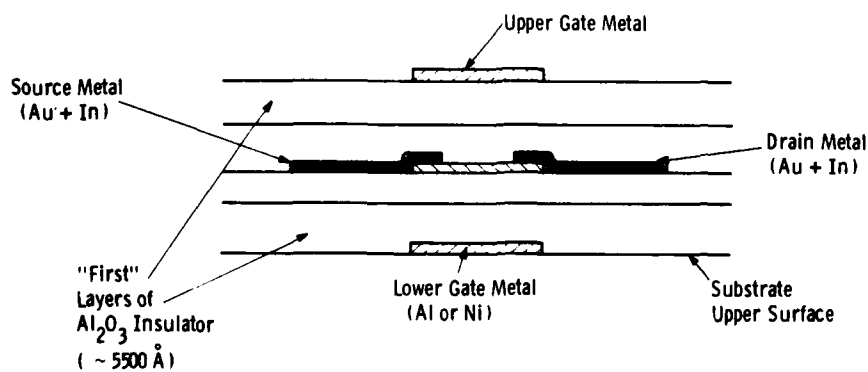


Fig. 5.21 — Identification of components of the 'double layer' gate insulator

in the standard recipe necessary for interconnection. This was done in the interest of expedience and to minimize nullification of the results by premature random system failure. In no way was the omission of these steps likely to affect transistor performance.

The first truly experimental substrate, 154-4 in Table 5.2 featured the double layer configuration shown in Figure 5.21. Deposition rates were maintained but the 500Å of oxide adjacent to the semiconductor, the second layer, was deposited in an oxygen-free ambient, unlike the first layers. Total oxide thickness was 6000Å as before.

Whereas power transistors on all four substrates passed the 200V dc test, the first two made by "standard" recipes collapsed in the preliminary viewability test as anticipated. Naturally the third and fourth substrates were not processed for viewability since there were no interconnect lines but they were stable under curve tracer test. The fourth substrate, 156-6, was oxygen-starved and exhibited characteristics consistent with a substantial downward shift in threshold voltage, with attendant high leakage. The variations in ON current from substrate to the next are not readily explained.

The results from this first experiment were encouraging but not conclusive. Rather than ruin the product, a decision was made to conduct the more comprehensive experiment shown in Table 5.3. Here processing responded not only to the pressures to decrease the total processing time but also to synthesize the critical CdSe/Al<sub>2</sub>O<sub>3</sub> interface more carefully with an even lower rate of deposition of the oxide. A batch of seven substrates hosting transistors only was processed in a single pumpdown, and featured not only double versus single layer comparisons and absence and presence of oxygen but also different deposition rates. This time, all transistors were driven to failure by collapse or breakdown.

The only transistors which showed no evidence of collapse in the second experiment, shown in Table 5.4.2, were fabricated in complete absence of oxygen. However, the undesirable threshold shift resulted

TABLE 5.2 Results of first collapse experiment featuring different oxygen partial pressures during evaporation of  $\text{Al}_2\text{O}_3$  gate insulators. Evaporation rate is constant at  $5 \text{ \AA}/\text{sec}$ .

Substrate No.	Recipe No.	Full Circuit	Transistors Only	Al <sub>2</sub> O <sub>3</sub> Deposition Conditions						Power Transistor Test Data			
				First Layer		Second Layer <sup>1</sup>		I <sub>ON</sub> na	I <sub>O</sub> na	200V Test	Collapse		
				Thick Å	Rate Å/sec	O <sub>2</sub>	Thick Å					Rate Å/sec	O <sub>2</sub>
153-1	3171	✓					6000	5	6 x 10 <sup>-5</sup>	1.0	150-400	✓	Yes <sup>2</sup>
153-2	3172	✓					6000	5	6 x 10 <sup>-5</sup>	1.0	300-450	✓	Yes
154-4	3178		✓	5500	5	6 x 10 <sup>-5</sup>	500	5	0	1.2	300-450	✓	?
156-6	3180		✓				6000	5	9 x 10 <sup>-6</sup>	0.6	400-5000	✓	?

<sup>1</sup>Adjacent to semiconductor

<sup>2</sup>After application of phosphor during test

TABLE 5.3 Results of second collapse experiment featuring double Al<sub>2</sub>O<sub>3</sub> layers at different rates and oxygen partial pressures

Substrate No.	Recipe No.	Full Circuit	Transistors Only	Al <sub>2</sub> O <sub>3</sub> Deposition Conditions				Power Transistor Test Data				
				First Layer		Second Layer 1		I <sub>ON</sub> na	I <sub>O</sub> na	200V Test	Collapse	
				Thick Å	Rate Å/sec	O <sub>2</sub>	Thick Å					Rate Å/sec
158-1	3188		✓			6000	5	6 x 10 <sup>-5</sup>	0.7	25-600	✓	Yes
158-2	3189		✓			6000	5	6 x 10 <sup>-5</sup>	0.6	10-60	(✓)	Yes
158-5	3191		✓	5500	5	6 x 10 <sup>-5</sup>	500	2	0	10-300	✓	Tendency
159-3	3192		✓			6000	20	6 x 10 <sup>-5</sup>	1.0	5-60	✓	Yes
159-6	3194		✓	5500	20	6 x 10 <sup>-5</sup>	500	2	0	10-250	✓	Tendency
159-7	3188		✓			6000	5	6 x 10 <sup>-5</sup>	0.5	5-30	No	Yes
159-8	3195		✓			6000	20	0	1.2	> 10,000	✓	No

<sup>1</sup>Adjacent to semiconductor

in unacceptable leakage, consistent with a model of aluminum migration from the oxygen-poor second layer into, and doping, the semiconductor creating a depletion device. However, both double-layer configurations gave encouraging results, and the higher rate  $20\text{\AA}/\text{sec}$   $\text{Al}_2\text{O}_3$  first layer, indicated a potential advantage in terms of throughput. The third and final experiment depicted in Table 5.4 built on the experience of the first two and consisted of three different runs. In the first run (substrates 164-1 through 166-8) an attempt was made to compare  $5\text{\AA}/\text{sec}$  and  $20\text{\AA}/\text{sec}$  deposition rates of the first layer, in both cases featuring a second layer of  $500\text{\AA}$  deposited at  $2\text{\AA}/\text{sec}$  with no oxygen. The results were somewhat marred in the failure of all five to convincingly pass the 200V test for reasons never determined. However, under severe drive, the slow rate second layer devices conductively exhibited collapse while at least one circuit, 166-5, with a second layer deposited at  $20\text{\AA}/\text{sec}$  convincingly failed to collapse. Because of throughput considerations, recipe 3214 was tentatively adopted as the new "standard". The remaining two runs in this experiment, 170-2 through 171-6 and 173-2 thru 174-6, were identical in terms of recipe. The purpose was to confirm or otherwise refute the merit of the recipe change as described. With reference to Table 5.4, we observe prevention of collapse at the expense of leakage current increases which were subsequently demonstrated not to be excessively detrimental in terms of display performance.

At this point, recipes 3211 and 3216 were verified and provisionally accepted as standard. The final state-of-the-art towards the conclusion of Phase II activity is shown in Table 5.5. Here we observe very respectable leakage levels, adequate and consistent ON current, and no tendency to collapse. The leakage current improvements we observe in Table 5.5 in comparison to Table 5.4 result from fine tuning the exposure of the as-deposited CdSe layer to indium in the doping step, described in further detail in Section 5.3.

RECIPE ID = RM3242

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	9	3100	2.70	25/1.0	28/1.1	5	500	1100	6.0X8	NI	POURSEMI
2	EB2	2	1	3100	2.70	25/1.0	28/1.1	5	300	1300	6.0X8	NI	GND-HIC1
3	EB2	1	8	4100	8.90	20/1.0	28/1.2	5	300	1000	6.0X8	AL	LGPWSEMI
4	FMA	0	1	3100	2.70	22/1.0	28/1.2	5	300	1500	6.0X8	MT	GND-HIC1
5	EB1	2	3	4100	4.00	50/2.0	50/1.1	20	300	6300	6.0X5	AO	GATECAPG
6	FMA	0	3	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	GATECAPG
7	FMA	0	3	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	GATECAPG
8	EB2	2	2	3100	2.70	25/1.0	28/1.1	5	300	900	6.0X8	NI	HIC2VIC1
9	FMA	0	10	3100	2.70	22/1.0	28/1.2	5	300	900	6.0X8	MT	EDGECONS
10	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
11	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
12	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
13	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
14	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
15	RES	0	6	4100	5.80	35/1.0	35/1.5	4	300	450	6.0X8	CS	VIC2TFIC
16	EB2	4	12	2100	2.40	19/1.5	22/1.1	40	3000	3000	6.0X8	IN	HIC2VIC1
17	EB2	4	12	4100	2.40	19/1.5	22/1.1	10	1000	1000	6.0X8	IN	HIC2VIC1
18	EB2	4	12	4100	2.40	19/1.5	22/1.1	1	200	200	6.0X8	IN	HIC2VIC1
19	EB2	4	5	4100	7.30	19/1.5	22/1.1	2	300	600	6.0X8	IN	SO/DRAIN
20	EB2	3	5	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	SO/DRAIN
21	EB2	1	8	4100	8.90	20/1.0	28/1.1	5	300	1300	6.0X8	AL	LGPWSEMI
22	FMA	0	8	4100	8.90	20/1.0	28/1.1	5	300	1300	6.0X8	MT	LGPWSEMI
23	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
24	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
25	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
26	FMA	0	4	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	INSULATR
27	EB2	2	2	3100	2.70	25/1.0	28/1.1	5	300	900	6.0X8	NI	HIC2VIC1
28	EB2	2	7	3100	2.70	22/1.0	28/1.2	5	300	1300	6.0X8	NI	ELMIDCAP
29	FMA	0	2	3100	2.70	22/1.0	28/1.2	5	300	900	6.0X8	MT	HIC2VIC1
30	EB1	2	3	4100	4.00	55/1.0	65/1.1	20	300	6300	6.0X5	AO	GATECAPG
31	FMA	0	3	4100	4.00	45/1.0	60/1.1	5	300	6300	6.0X8	MT	GATECAPG
32	EB2	2	10	3100	2.70	25/1.0	28/1.1	10	300	900	6.0X8	NI	EDGECONS
33	EB2	2	7	3100	2.70	25/1.0	28/1.1	10	300	1300	6.0X8	NI	ELMIDCAP
34	EB2	2	9	3100	2.70	25/1.0	28/1.1	10	300	900	6.0X8	NI	POURSEMI
35	EB2	2	11	3100	2.70	22/1.0	28/1.1	10	300	500	6.0X8	NI	GND-HIC1
36	EB2	1	11	4100	8.90	24/1.5	30/1.1	20	300	1800	6.0X8	AL	GND-HIC1
37	EB2	3	11	3100	19.30	20/1.7	28/1.3	10	300	900	6.0X8	AU	GND-HIC1
38	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	2300	6.0X5	AO	INSULATR
39	EB1	2	8	4100	4.00	55/1.0	65/1.1	5	300	500	6.0X8	AO	LGPWSEMI

Figure 5.22

At the conclusion of Phase II the state-of-the-art is best exemplified by the excellent performance from a circuit viewpoint illustrated in Figure 5.23. Unfortunately, this was the only complete unit fabricated in spite of intense and sustained effort and itself did not fully respond to requirements of the program detailed in the SCS-501 specifications, particularly in regard to phosphor maintenance at high temperature (72°C) and humidity. Nonetheless, it provided a firm basis from which to proceed in Phase III activity, which focussed on its deficiencies.

#### 5.4.2 Results of Circuit Fabrication Achieved in Phase III

As a reminder, Phase III of the contract refers to the period November 1978 through June 1979. This timeframe saw implementation of the technical strategy previously discussed in great detail in Section 1.5. In summary, the activity highlighted revised mask design and circuit deposition processes, more comprehensive test data logging and redesign, and rebuilding of test electronics. Not all activities could begin instantly. In actuality, events proceeded approximately as indicated in Figure 5.29. This figure indicates:

- (1) Identification of tasks and reference to fuller descriptions in other sections of this report.
- (2) A "crash" mask redesign effort proceeding in parallel with evaporated nickel busbar development, from the outset.
- (3) Minimal time remaining for actual "pilot production" itself.

In effect, the mask and process redesign tasks were one integral operation. In order to maximize benefit from mask redesign, the process had to be simplified and vice versa. The element of risk in this tactic was the unknown in nickel evaporation, with which we had little previous experience. The reason for venturing into this unknown, as we shall see, was that process simplification suggested replacement of the aluminum, chrome and copper circuit components with those formed by a single metal. In addition, one problem identified earlier was the failure vulnerability



THIS IS A TFT-EL DISPLAY PANEL  
OFF THE WESTINGHOUSE AUTOMATED  
PILOT PRODUCTION LINE. IT CON-  
TAINS 34000 HIGH VOLTAGE TRAN-  
SISTORS AND 17000 CAPACITORS.  
EACH PICTURE ELEMENT OPERATES ON  
A 100% DUTY CYCLE. AUTOMATED PRO-  
DUCTION PROMISES VERY LOW COSTS

Figure 5.23 The fully assembled display constructed from circuits fabricated during Program Phase 11.

of the copper link previously used to attach gold/indium source drains to the aluminum busbars. Another was the relative "unrepairability" of the aluminum busbars.

This process reformulation was initiated immediately. The assumption was that the risk in redesigning masks to be made from Kovar, which would function at least as well as those previously made from beryllium-copper, was acceptable. Conversely, mask redesign was initiated on the hypothesis that nickel could adequately replace aluminum, copper and chrome. Again as we shall see, both assumptions were subsequently proved solid. The reasons we selected nickel as the metal to replace the three then used were:

- (1) We had previously had at least some limited experience with it on other projects.
- (2) It was not physically, chemically or metallurgically incompatible with any other of the deposition materials we were going to continue using.
- (3) Electrical conductivity was reasonable.
- (4) Nickel films were potentially less vulnerable to mechanical damage.

Problems which we had to keep in mind were as follows:

- (1) Nickel's reputation for not sticking to glass.
- (2) Higher temperatures induced during the evaporation.

We later found that the first of these concerns was indeed no problem at all, but the second presented difficulties we had to work around.

As a first maneuver, we substituted a nickel slug for the aluminum and copper charges in the electron beam gun well, and otherwise left the processing recipe unchanged. The result was a fairly severe mask warpage resulting from heating during evaporation. The outcome was catastrophic circuit failure due to multiple short circuits. As explained above, the masks being used then were the conventional beryllium-copper core model. Although we had available some Kovar

cored masks, these had been obtained before the supplier had been able to perfect his fabrication process and hence the masks were geometrically defective to a greater or lesser extent. However, since our immediate task was to develop a nickel evaporation expertise, rather than futilely attempt to make perfect panels, we substituted Kovar masks for those pattern segments most vulnerable to evaporation heat induced distortion. The aperture patterns of these prototype Kovar masks were of course geometrically consistent with the "old" (Phase II) layout shown in Figures 5.8 and 5.9. The effects of distortion convincingly disappeared, although the circuits so produced were extensively defective in terms of discontinuous busbars and short circuits. The defective geometries of these stop-gap Kovar masks, however, were the prime reason. In spite of this, there were some positive characteristics of the preliminary results obtained. These were:

- (1) The nickel films adhered very effectively to the glass. They were virtually unscratchable.
- (2) Where electrical busbar opens existed and had to be manually "repaired", epoxy bridges adhered substantially better than they previously had to aluminum busbars, probably because the nickel did not so readily oxidize.
- (3) Crossover insulators were sustaining about the same voltages as previously, i.e., 300-900 VDC before breakdown.
- (4) Busbar impedances were only marginally higher with nickel instead of aluminum as shown in Table 5.4.5. The "nickel" substrates in this tabulation reflect the state-of-the-process at the beginning, middle and end of the nickel busbar process development period. Chronological gyrations in the busbar impedance values resulted from processing variations designed to overcome the peeling problem we shall discuss later. However, we never observed, at that time or subsequently, display performance inhibited by busbar impedance of this order of magnitude.

TABLE 5.4 Results of third collapse experiment featuring three runs made with different Al<sub>2</sub>O<sub>3</sub> deposition rates and oxygen partial pressures

Substrate No.	Recipe No.	Full Circuit	Transistors Only	Al <sub>2</sub> O <sub>3</sub> Deposition Conditions					Power Transistor Test Data		
				First Layer		Second Layer <sup>1</sup>			I <sub>ON</sub> na	I <sub>o</sub> na	200V Test
				Thick Å	Rate Å/sec	O <sub>2</sub>	Thick Å	Rate Å/sec			
164-1	3201	✓		5500	5	6 x 10 <sup>-5</sup>	500	2	1.0	600-10000	✓
165-2	3202	✓		6000	5	6 x 10 <sup>-5</sup>	500	2	1.0	200-12000	(✓)
165-4	3213	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.2	1000-5000	(✓)
166-5	3214	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.1	40-450	(✓)
166-8	3214	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.1	150-500	(✓)
170-2	3211	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.2	600-12000	✓
170-4	3222	✓					6000	5	1.0	10-150	✓
171-6	3216	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.0	20-400	✓
173-2	3211	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.0	200-1400	✓
173-3	3222	✓					6000	5	0.7	10-50	✓
174-6	3216	✓		5500	20	6 x 10 <sup>-5</sup>	500	2	1.2	25-100	✓
											Yes
											Yes
											No
											No
											No
											Yes
											No
											No
											Yes
											No

<sup>1</sup>Adjacent to semiconductor

TABLE 5.5 Power transistor fabrication state-of-the-art at termination of program Phase II with Be-Cu masks and Al and Cu interconnects

Substrate No.	Recipe No.	Full Circuit	Transistors Only	Al <sub>2</sub> O <sub>3</sub> Deposition Conditions					Power Transistor Test Data			
				First Layer		Second Layer <sup>1</sup>			I <sub>ON</sub> na	I <sub>o</sub> na	200V Test	Collapse
				Thick Å	Rate Å/sec	O <sub>2</sub>	Thick Å	Rate Å/sec				
209-3	3242	✓		5500	20	$6 \times 10^{-5}$	500	2	0	900 20-25	✓	No
212-6	3244	✓		5500	20	$6 \times 10^{-5}$	500	2	0	1000 25-40	✓	No
216-2	3245	✓		5500	20	$6 \times 10^{-5}$	500	2	0	1200 30-7000	✓	No

<sup>1</sup>Adjacent to semiconductor

TABLE 5.6 Busbar impedance comparisons using the old mask design before and after nickel substitution for aluminum, copper & chrome. (All measurements made on circuits featuring the "old" Phase II mask design).

Substrate No.	Busbar Material	Source	Resistance k $\Omega$	
			Gate	Ground
8-268-5*	Al	0.7 - 1.0	0.8 - 1.0	0.53 - 0.75
8-314-4	Ni	1.3 - 2.9	1.7 - 2.4	0.8 - 1.1
9-017-1	Ni	1.4 - 1.7	2.4 - 3.9	0.8 - 1.1
9-052-1	Ni	1.4 - 1.6	1.5 - 2.2	1.4 - 1.8

\*Typical values for the Al-Cu-Cr recipes

In addition, with nickel-gated transistors, for some reason we were experiencing significantly less leakage than previously, as illustrated in Table 5.7. Here we have measurements of "ON" and "OFF" currents of transistors of each type made on eight different substrates. Four of the substrates were fabricated with aluminum gates and four with nickel, as shown. Each measurement, or measurement range, represents data taken on a sample of ten transistors in each case. Leakages for both transistors (measured at zero gate voltage and minus ten source-drain volts), are typically an order of magnitude lower for nickel gates than for aluminum gates. We have no explanation for this since the active regions, including the source and drain metals of the transistors, were made identically. This also applies to the insulator layer synthesis. The strange thing is, however, that the variations in transistor performance seem to have minimal discernible effect on the display performance, as can be observed from the rightmost four columns in Table 5.7. These measurements were made after phosphor was applied to the circuit and it was driven in an alphanumeric message display mode. The procedure required the operator to adjust the source and gate drive voltage positive and negative bias controls until the displayed message was the most clearly and uniformly viewable. He was required to do this three times; the controls were randomly reset after each measurement so that no one judgment of the best picture was influenced by the previous judgment. The data shown in Table 5.4.6 represents the average of the three measurements, all of which were typically within a range of one or two volts.

Thus, although we had inadvertently and inexplicably made "better" transistors, the drive requirements of the display were unaffected within the "noise level" associated with random variations from display to display. This was only the beginning of a pattern of events which focussed attention subsequently even more clearly on the hypothesis that rudimentary but fully functional thin film transistor addressed displays are in no way limited in manufacturability by the characteristics of the state-of-the-art of thin film transistor

TABLE 5.7 Comparison of transistor characteristics and drive voltage requirements of display half-panels made from randomly selected circuits fabricated immediately before and after the process change substituting nickel for aluminum, copper & chrome. Substrate order is order of fabrication, chronologically.

Substrate No.	Current				Drive Voltages Required for Display Legibility for V <sub>EL</sub> = 1000 VAC, 5 kHz			
	Logic Transistor ON $\mu$ a	Logic Transistor OFF na	Power Transistor ON $\mu$ a	Power Transistor OFF na	S+	S-	G+	G-
(Standard Al, Cu, Cr process)								
228-8	60-100	2-8	1000-1200	400-6000	4	6	11	12
261-4	40-150	10-18	1200	30-1000	9	4	12	12
268-5	100-150	8-15	1000-1200	25-50	14	1	17	11
291-8	150	5-10	1200	30-400	7	7	20	12
(Process change: substitute Ni for Al, Cu, Cr)								
342-3	30	5	180-600	15-25	5	4	13	5
044-2	60-80	1	800-1000	5-9	8	3	18	14
072-2	60	1-2	1000-1200	3-10	8	6	14	11
072-3	30-80	0-2	1200	6-20	9	8	8	9



fabrication. It does not follow, but is nonetheless probably true, that thin film transistor addressed displays are readily manufacturable. However, the barriers which must be overcome are related to deficiencies in the state-of-the-art of transistor interconnection technology rather than to those associated with transistor performance. Further evidence in favor of this hypothesis emerges later. A physical model for the improved behavior of the nickel as opposed to aluminum gated transistors is provided in Section 2.4.1.

Immediately after this vindication of the substitution of nickel for aluminum, copper and chrome with the old Phase II circuit design, at least as far as transistor and circuit performance was concerned, we were immediately confronted with a new problem. Whereas there was no difficulty persuading nickel films to adhere to the glass substrates, it insisted on feeding extensively from the relief sides of the stop-gap Kovar masks. We were able later to modify the recipe by way of lowering nickel film thicknesses, without further appreciable increase of busbar impedance. This, combined with vigorous cleaning of the masks after every three runs, virtually resolved the mask peeling problem.

Another undesirable characteristic of the nickel-wired circuits were defects believed related to a generally "dirty" appearance. To what extent this resulted from our using impure nickel is not clear. However, in a later batch of three substrates, which was processed with "pure" nickel, the circuits appeared visually much cleaner. At the same time, the transistors were observed to have the lowest leakage ever observed by the operator who had been making these tests for over a year. In Tables 5.8 through 5.9 and in Tables 5.11 through 5.13 we show test results, in detail, made on power and logic transistors, respectively, from the three substrates fabricated in the run in question. The test procedure and the related notation itself is described in detail in Section 6.4. Note that two power transistors of each type are tested at each specified location.

TABLE 5.8 Power transistor characteristics for circuit number 9033-2 made in the first run which featured busbars and gates synthesized from EB-evaporated high purity nickel. (Refer to Section 6.4 for notation and explanation of test procedure).

Test Transistor Location* S G	Leakage		ON Current $I_{ON}$ ( $\mu a$ )	Stability S
	$I_o$ (na)	$I_{10}$ ( $\mu a$ )		
• 8 12	5	16	1000	9/5
•	8	14	1000	9/5
• 47 12	10	14	1000	8/5
•	8	12	1000	8/5
• 26 37	60	25	1200	10/6
•	40	20	1200	10/6
• 5 63	60	20	1200	10/6
•	50	22	1200	10/6
• 46 63	10	18	1200	10/6
•	10	24	1200	10/6

\* Address definitions are described in the discussion of Fault Identification in Section 6.4.

TABLE 5.9

Power transistor characteristics for circuit number 9036-3 made in the first run which featured busbars and gates synthesized from EB-evaporated high purity nickel. (Refer to Section 6.4 for notation and explanation of test procedure).

Test Transistor Location*		Leakage		ON Current $I_{ON}$ ( $\mu$ a)	Stability S
		$I_o$ (na)	$I_{10}$ ( $\mu$ a)		
.	8 12	800	140	1200	10/6
.		1000	120	1200	10/6
.	47 12	200	90	1000	9/5
.		400	70	1000	9/5
.	26 37	100	90	1200	10/6
.		400	90	1200	10/6
.	5 63	800	100	1200	10/6
.		600	70	1200	10/6
.	46 63	150	90	shorted	—
.		100	80	1200	10/6

\* Address definitions are described in the discussion of Fault Identification in Section 6.4.

TABLE 5.10 Power transistor characteristics for circuit number 9036-5 made in the first run which featured busbars and gates synthesized from EB-evaporated high purity nickel. (Refer to Section 6.4 for notation and explanation of test procedure).

Test Transistor Location* S G		Leakage		ON Current I <sub>ON</sub> (μa)	Stability S
		I <sub>0</sub> (na)	I <sub>10</sub> (μa)		
•	8 12	8	25	1000	9/5
•		10	25	1000	9/5
•	47 12	10	20	1000	9/5
•		10	25	1000	9/5
•	26 37	15	35	1200	10/6
•		10	25	1200	10/6
•	5 63	8	18	1000	9/5
•		10	20	1000	9/5
•	46 63	12	25	1200	10/6
•		50	30	1200	10/6

\* Address definitions are described in the discussion of Fault Identification in Section 6.4.

TABLE 5.11      Logic transistor characteristics for circuit number 9033-2 made in the first run which featured busbars and gates synthesized from EB-evaporated high purity nickel. (Refer to Section 6.4 for notation and explanation of test procedure).

Test Transistor Location* S    G		Leakage		ON Current $I_{ON}$ ( $\mu$ a)	Stability S
		$I_o$ (na)	$I_{10}$ ( $\mu$ a)		
•	8    12	2	50	60	7/3
•					
•	47   12	2	60	60	7/3
•					
•	26   37	3	60	100	9/5
•					
•	5    63	2	60	80	9/4
•					
•	46   63	3	60	100	9/5
•					

\* Address definitions are described in the discussion of Fault Identification in Section 6.4.

TABLE 5.12      Logic transistor characteristics for circuit number 9036-3 made in the first run which featured busbars and gates synthesized from EB-evaporated high purity nickel. (Refer to Section 6.4 for notation and explanation of test procedure).

Test Transistor Location* S    G		Leakage		ON Current $I_{ON}$ ( $\mu a$ )	Stability S
		$I_o$ (na)	$I_{10}$ ( $\mu a$ )		
•	8 12	1	90	80	9/4
•					
•	47 12	1	80	60	7/3
•					
•	26 37	2	80	120	10/6
•					
•	5 63	3	60	100	9/5
•					
•	46 63	4	50	120	10/6
•					

\* Address definitions are described in the discussion of Fault Identification in Section 6.4.

TABLE 5.13

Logic transistor characteristics for circuit number 9036-5 made in the first run which featured busbars and gates synthesized from EB-evaporated high purity nickel. (Refer to Section 6.4 for notation and explanation of test procedure).

Test Transistor Location* S G		Leakage		ON Current $I_{ON}$ ( $\mu$ a)	Stability S
		$I_o$ (na)	$I_{10}$ ( $\mu$ a)		
•	8 12	3	50	60	7/3
•					
•	47 12	3	40	80	9/4
•					
•	26 37	2	60	80	9/4
•					
•	5 63	4	60	80	9/4
•					
•	46 63	3	55	80	10/4
•					

\* Address definitions are described in the discussion of Fault Identification in Section 6.4.

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With reference to Figures 5.14 through 5.19, the columns labeled  $I_{10}$  refer to a measurement which is explicitly described in Section 6.4. It is not clear, in fact it remains contentious, how relevant this measurement really is relative to projecting circuit performance in driving a display. In any event, typical measurements shown in Tables 5.4.7 through 5.4.12 are not significantly different than those obtained for aluminum-gated transistors.

Whereas our records do not contain data on the voltage breakdown capability of these earlier devices, we do know they could all sustain in excess of two hundred volts DC from source-gate to drain. It was only after circuit fabrication with masks featuring the revised-pattern design that we systematically breakdown voltage tested to destruction. At no time during Phase III of the program did we ever observe the troublesome power transistor collapse problem described in the previous section. The uniformity of the test data from point to point across the four-inch substrates, and from substrate-to-substrate, of these nickel-gated devices should once and for all dispel myths of irreproducibility and non-uniformity historically associated with thin film transistor fabrication, for the limited purpose of driving displays. This level of uniformity and reproducibility prevailed throughout the remainder of the program, except when mechanical or electrical equipment failure or human error resulted in catastrophic failure. The most gratifying of all the test results are, of course, the low quiescent leakages of particularly the logic transistors shown in Tables 5.8 through 5.13. The practical impact is a substantially lower minimum picture refresh rate, all other things being equal, when using nickel-gated instead of aluminum-gated transistors. At the same time, a word of caution is in order concerning this distinction. The implication is that the fabrication of the gate electrodes alone was responsible for the improvement in performance. It is most likely that the absence of a copper from the vicinity of the active semiconductor regions of the devices and the more favorable behavior of indium in a gold-nickel vs. a gold-copper environment was the origin of the improvements. This issue is discussed further in Section 2.4.1.

Shortly before the arrival of the new masks made from Kovar with the revised pattern, a short adventuresome experiment was conducted to determine whether nickel could also be used as a source drain material rather than indium-doped gold. The advantages were an ultimately simpler fabrication process. Although prior experience had led us to believe that these so-called "nickel transistors" were inherently leaky, the new drive electronics scheme discussed in Section 9.5 promised to render nominal ill-effects of low threshold voltages inconsequential.

The results of two experiments in which circuits were fabricated with transistors featuring nickel instead of gold source drains are shown in Table 5.14. The nature of the experiments was simply to substitute nickel for gold, depositing it at the same rate and to the same depth, namely  $1000\text{\AA}$  at  $5\text{\AA}/\text{sec}$ . All other steps in the recipes were identical. Referring to Table 5.14, all three circuits in lines 3 through 5 were fabricated in the same run. Circuits 110-5 and 115-3 in lines 6 and 7 were synthesized in consecutive runs. (The circuit fabricated with recipe 4012 in the same run as circuit 110-5 was destroyed due to a once-in-a-lifetime event — depletion of the gold charge in the electron beam gun hearth ). However, the comparison is otherwise meaningful. Lines 1 and 2 serve as a basis to compare transistor characteristics before and after substitution of nickel for aluminum gates. Other relevant summary information is listed under the "Comment" columns in Table 5.14. In all cases, the source drains were identically doped with indium by the technique described in Section 5.3.

The result of substituting of nickel for gold is probably best summarized by commenting on its impact on a phenomenological basis. The transistor current characteristics it consistently generated were remarkably similar to those shown in line 4 of Table 5.2 and line 7 of Table 5.3 when aluminum ride gate insulators were deposited without the presence of oxygen. One could argue therefore that both mechanisms eventually doped the semiconductor to an extent that it reverted to n-type polarity creating depletion device with

TABLE 5.14 Results of substituting nickel for gold source-drains in an attempt to make "all-nickel" transistors

Substrate No.	Recipe No.	Source-Drain Material (all In-doped)	Gate Material	Transistor Test Data				Comment	
				Power Device		Logic Device		Process	Results
				I <sub>ON</sub> μa	I <sub>O</sub> na	I <sub>ON</sub> μa	I <sub>O</sub> na		
209-3	3242*1	Au	Al	900	20-25	60-80	8-18	Phase II state-of-art Al/Cu busbars -old masks- see Table 5.4.4	Produced functional displays
212-6	3244	Au	Al	1000	25-40	80-100	10-15		
059-1	3285	Au	Ni	1000-1200	4-12	80	< 1 <sup>3</sup>	Phase II pattern -old masks- Ni busbars	See also Tables 5.4.7 thru 5.4.12
060-2	3286	Au	Ni	1000-1200	3-20	80-100	< 1 <sup>3</sup>		
060-3	3287	Ni	Ni	1000	2000-7000	150	1000-2000		
110-5	4016	Ni	Ni	400-800	4000-12000	80-150	200-400	New Phase III pattern & masks Ni busbars	Au source drain produced functional display
115-3	4012 <sup>2</sup>	Au	Ni	600-700	25-60	20-40	2-3		

\*<sup>1</sup> Shown in Figure 5.4.14

<sup>2</sup> Shown in Figure 5.4.22

<sup>3</sup> Too low to measure

TABLE 5.15 Results of experiments comparatively investigating "common transistor" and "differential doping" recipe formulations. (Five transistors tested for each line of data).

Line No.	Run No.	Substrate No.	Recipe No.	Process Comment	Transistor Characteristics								Results/Comments
					Power Transistor				Logic Transistor				
					I <sub>ON</sub> μa	I <sub>O</sub> na	S	V <sub>BD</sub> volts	I <sub>ON</sub> μa	I <sub>O</sub> na	S	V <sub>BD</sub> volts	
1	20	124-3	4022	"Standard" Differential Doping	800-1000	4-30	6/5	> 200	60-100	2-4	7/5	NT	Much better logic ION
2	20	124-5	4023		1000-1200	12-80	8/5	> 200	40-100	2-3	7/5	NT	
3	21	131-3	4022	"Standard" as above	800-1000	7-12	8/5	> 200	30-40	2-5	7/4	NT	
4	21	131-4	4021	Common transistor	800-1000	4-8	8/5	> 200	250-350	4-5	8/6	NT	
5	21	134-5	4023	"Standard" as above	800-1000	5-10	7/5	350-600	30-50	0-4	7/4	NT	
6	25	151-1	4026	Common xstor	1000	5-14	8/5	450	300-350	4-15	10/7	300-550	"
7	25	151-3	4027	Common xstor	1000	4-10	9/5	400-500	400	3-15	7/4	400-550	"
8	25	151-5	4027	Common xstor	1000	3-8	8/5	150-500	300-400	2-4	6/4	300-500	"

<sup>1</sup>NT = not tested

During Phase III, several other processing alternatives relating to the transistors were evaluated before the final processing recipe was developed. These were the "common transistor" subprocess, single-gated transistors and "wait step elimination." All three alternatives were tried in the interests of further process simplification. (A discussion of the remarkable throughput improvements already achieved by this time as a consequence of the new mask design and process is postponed until later ). The first and third of these subprocess alternatives were proved successful and were subsequently adopted. Although the second, involving single gated transistors, was unsuccessful, it also will be described because of its technical interest.

The common transistor subprocess relates to the procedure wherein, historically, the power transistor active semiconductor layer was doped by indium to a higher level than the logic transistor. The latter had always been doped only by diffusion from indium deposited through the source drain masks whereas the active layer of the power transistors were exposed to additional indium deposited through a mask with apertures conforming to their active (semiconductor-defining) geometries. The resulting preferred doping of the power transistors, performed as described in Section 5.3, was designed to differentially lower the threshold voltage of the power devices to provide enhanced driving of the electroluminescent phosphor dots. Whereas the mask count had been reduced from twelve to ten in the transition from the old to the new masks, there was a very good reason for attempting to reduce the new mask count to nine, which will be discussed later. Eliminating differential doping promised to make this possible through the discarding of the differential doping step and associated mask. The mechanics of the common transistor synthesis was simply to indium dope the power transistor through the semiconductor mask (number 8). This means that the logic transistor as well as the power device receives doping "in the gap" in addition to that through diffusion from the source drain pads. The two types of devices are said to be

strongly negative threshold voltage. On the other hand, under high voltage test, whereas the stoichiometry of the aluminum oxide gate insulator, preferentially favoring aluminum, prevented collapse as described in Section 5.4.1, the nickel source drain devices of circuit 060-3 in line 5 of Table 5.14 showed a distinct tendency to collapse. This was the only time when this problem ever reared its head in the fabrication of nickel-gated transistors. The discussion of Section 2.4.1 has elaborated further on likely physical mechanisms.

Other than the effects of the substitution of nickel for gold, Table 5.14 displays other interesting trends. A further general chronological improvement in the leakage levels occurs particularly for the logic devices, with its promising impact on minimum allowable frame refresh rate. The levels shown in the table were maintained in transistor fabrication throughout the rather brief remaining duration of program activity.

Table 5.14 also typifies progression of events not only as nickel was substituted for aluminum as gate metal but also as the new Kovar masks replaced the older beryllium-copper cored ones. The much improved design of the former, described in detail in Sections 4.3 through 4.6, also made possible the easier and more comprehensive transistor testing through its strategic placement of special test transistors with readily accessible contact pads. The somewhat low ON-currents shown in lines 6 and 7 of the table were anomalous in that "normal" ON currents of 1 mA and 75  $\mu$ A were subsequently readily reproduced by recipes similar to 4012 (line 7, Table 5.14) in the fabrication of transistors with the new Kovar masks. This recipe is shown in Figure 5.26 and the reader is invited to compare its step count of 30 with that of 39 in recipe 3242 shown in Figure 5.22. However, in spite of the further potential process simplification and throughput implicit in the substitution of nickel for gold in the transistor source drain pads, severe limitations on remaining resources convinced us to err on the side of caution and stay with the gold formulation with which we had had extensive experience.

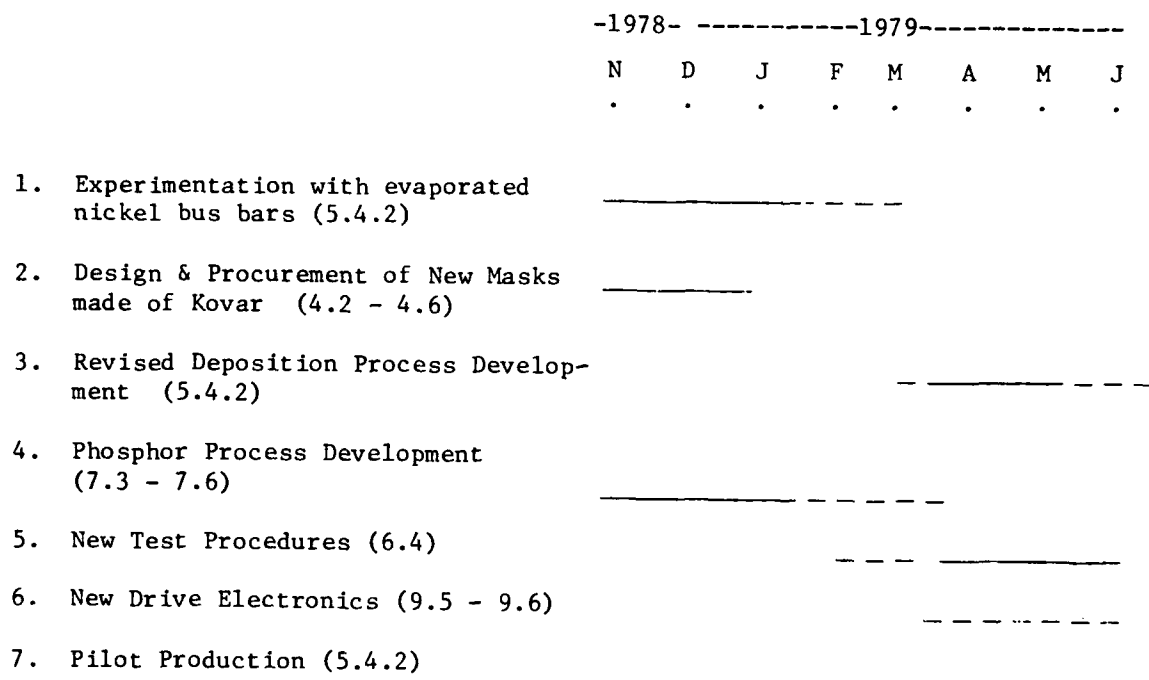


Figure 5.24 Schedule of major events during Program Phase III.

"commonly doped" and differ only in their geometries, not their metallurgies.

Results, in terms of transistor characteristics of three experimental runs, wherein the effects of omitting differential doping was assessed, are shown in Table 5.15. Here we compare transistor characteristics featuring non-differential doping with those made by the then standard recipe. Naturally, only the logic transistor characteristics are affected. This table also demonstrates, through inspection of the power transistor characteristics, the remarkable level of transistor reproducibility not only between devices on the same substrate and from substrate to substrate within the same run, which we have also shown in earlier tabulations, but also from run to run. We became quite accustomed to this level of consistency as events unfolded in the last two months of the program.

Referring to Table 5.15, lines 1 and 2, pertaining to Run 20, reflects the state-of-the-art at the beginning of the experiment. The only difference between the recipes used here exemplified by recipe number 4022 shown in Figure 5.25 and the previous standard recipe 4012 shown in Figure 5.26 is the decrease in the thickness of the nickel busbars from 1000Å to 600Å as exemplified by line 1 in each figure. The purpose of this maneuver was further to prevent peeling of in-process deposited material on the relief sides of the masks and also to increase throughput.

Lines 3 through 5 in Table 5.4.14 report results from Run 21 wherein one circuit was deposited with a common transistor doping configuration. Lines 6 through 8 reflect one of the common transistor recipes in a verification run with all substrates being made with common transistor recipes modified from recipe 4021, shown in Figure 5.27 only to permit post-process deposition of the edge connectors. Accordingly recipe 4021 in Figure 5.27 reflects state-of-the-art at the conclusion of the common transistor recipes.



RECIPE ID = RM4022

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GND-HIC1
2	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GATECAPG
3	EB2	2	2	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	HIC2VIC1
4	FMA	0	2	3100	8.90	22/1.0	28/1.1	5	300	1300	6.0X8	MT	HIC2VIC1
5	EB1	2	4	4100	4.00	50/1.0	50/1.1	20	300	5800	6.0X5	AO	INSULATR
6	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
7	FMA	0	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	MT	INSULATR
8	FMA	0	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	MT	INSULATR
9	FMA	0	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	MT	INSULATR
10	EB2	2	6	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	VIC2TFIC
11	EB2	2	7	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	ELMIDCAP
12	RES	0	8	4100	5.80	30/1.0	32/1.5	4	350	450	6.0X8	CS	LGPWSEMI
13	RES	0	9	4100	5.80	30/1.0	32/1.5	4	300	350	6.0X8	CS	POURSEMI
14	EB2	4	9	2100	2.40	19/1.5	22/1.1	40	3000	3000	6.0X8	IN	POURSEMI
15	EB2	4	9	4100	2.40	19/1.5	22/1.1	10	1000	1000	6.0X8	IN	POURSEMI
16	EB2	4	9	4100	2.40	19/1.5	28/1.1	1	200	200	6.0X8	IN	POURSEMI
17	EB2	4	5	4100	7.30	19/1.5	28/1.1	2	300	600	6.0X8	IN	SO/DRAIN
18	EB2	3	5	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	SO/DRAIN
19	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
20	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
21	FMA	0	4	4100	4.00	55/1.0	65/1.1	5	300	5800	6.0X8	MT	INSULATR
22	FMA	0	4	4100	4.00	55/1.0	65/1.1	5	300	5800	6.0X8	MT	INSULATR
23	FMA	0	4	4100	4.00	55/1.0	65/1.1	5	300	5800	6.0X8	MT	INSULATR
24	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GATECAPG
25	EB2	2	11	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GND-HIC1
26	EB2	2	12	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	HIC2VIC1
27	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	3300	6.0X5	AO	INSULATR
28	FMA	0	4	4100	4.00	55/1.0	65/1.1	20	300	3300	6.0X8	MT	INSULATR
29	EB2	2	10	3100	8.90	22/1.0	28/1.1	5	300	1300	6.0X8	NI	EDGECONS
30	EB2	3	10	3100	19.30	22/1.5	28/1.1	5	300	900	6.0X8	AU	EDGECONS

Figure 5.25 Recipe 4022 providing differential doping in circuit 124-3 (line 1, Table 5.4.14).

RECIPE ID = RM4012

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	8.90	22/1.0	28/1.1	5	300	1300	6.0X8	NI	GND-HIC1
2	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GATECAPG
3	EB2	2	2	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	HIC2VIC1
4	FMA	0	2	3100	8.90	22/1.0	28/1.1	5	300	1300	6.0X8	MT	HIC2VIC1
5	EB1	2	4	4100	4.00	50/1.0	50/1.1	20	300	5800	6.0X5	AO	INSULATR
6	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
7	FMA	0	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	MT	INSULATR
8	FMA	0	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	MT	INSULATR
9	FMA	0	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	MT	INSULATR
10	EB2	2	6	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	VIC2TFIC
11	EB2	2	7	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	ELMIDCAP
12	RES	0	8	4100	5.80	30/1.0	32/1.5	4	350	450	6.0X8	CS	LGPWSEMI
13	RES	0	9	4100	5.80	30/1.0	32/1.5	4	300	350	6.0X8	CS	POWRSEMI
14	EB2	4	9	2100	2.40	19/1.5	22/1.1	40	3000	3000	6.0X8	IN	POWRSEMI
15	EB2	4	9	4100	2.40	19/1.5	22/1.1	10	1000	1000	6.0X8	IN	POWRSEMI
16	EB2	4	9	4100	2.40	19/1.5	28/1.1	1	200	200	6.0X8	IN	POWRSEMI
17	EB2	4	5	4100	7.30	19/1.5	28/1.1	2	300	600	6.0X8	IN	SO/DRAIN
18	EB2	3	5	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	SO/DRAIN
19	EB1	2	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
20	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
21	FMA	0	4	4100	4.00	55/1.0	65/1.1	5	300	5800	6.0X8	MT	INSULATR
22	FMA	0	4	4100	4.00	55/1.0	65/1.1	5	300	5800	6.0X8	MT	INSULATR
23	FMA	0	4	4100	4.00	55/1.0	65/1.1	5	300	5800	6.0X8	MT	INSULATR
24	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GATECAPG
25	EB2	2	1	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	GND-HIC1
26	EB2	2	2	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	HIC2VIC1
27	EB1	2	4	4100	4.00	55/1.0	65/1.1	20	300	3300	6.0X5	AO	INSULATR
28	FMA	0	4	4100	4.00	55/1.0	65/1.1	20	300	3300	6.0X8	MT	INSULATR
29	EB2	2	10	3100	8.90	22/1.0	28/1.1	5	300	1300	6.0X8	NI	EDGECONS
30	EB2	3	10	3100	19.30	22/1.5	28/1.1	5	300	900	6.0X8	AU	EDGECONS

Figure 5.26

Recipe 4012 adopted as "Standard" after acquisition of new Kovar masks.

The Transistor Characteristic columns in Table 5.15 show also stability and breakdown voltage data derived as explained in Section 6.4. While the characteristics of common transistor doping were being evaluated, we established the practice of routinely testing the breakdown of selected test transistors, provided by the new masks, to destruction. As can be clearly seen from inspection of the logic transistor data in Table 5.15, the effects of common doping are clearly and exclusively beneficial in that the gain of the devices is substantially enhanced with no apparent ill-effects. The single apparent power transistor low breakdown voltage event portrayed in line 8 was believed, with good reason, to be anomalous. The impact of this development was a simpler process providing potentially faster display writing speeds.

Another process variation being conducted concurrently with common transistors was elimination of the wait steps explained in Section 5.3. Here the idea again was strictly to improve throughput. This gave us the unprecedentedly short 2 hour 22 step process defined by recipe 4041, shown in Figure 5.28. A very important feature of this recipe is the sixth step. Here we observe segments of the vertical busbars, the "source" lines, being deposited after the insulators instead of before as in recipe 4021 in Figure 5.27. In this way, "waiting for cooling" following aluminum oxide deposition effectively proceeds in parallel with an actual circuit synthesis step, thereby compensating for the wait steps. We had observed, on one earlier occasion, mechanical softness and vulnerability of the nickel films to damage, accompanied by extraordinarily high transistor threshold voltages when the wait steps were eliminated from recipe 4021 without reordering the steps, as explained above, in recipe 4041. This recipe, shown in Figure 5.28, therefore represents our final recommendation for optimal circuit production and was used for the duration of the program.

In a later run, we had the unexpected opportunity to examine the characteristics of "single gate" transistors when mechanical failure

RECIPE 10 = RM4021

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GND-HIC1
2	EB2	2	3	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GATECAPG
3	EB2	2	2	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	HIC2VIC1
4	FMA	0	2	3100	8.90	22/1.0	28/1	5	300	1300	6.0X8	MT	HIC2VIC1
5	EB1	1	4	4100	4.00	50/1.0	50/1	20	300	5800	6.0X5	AD	INSULATR
6	EB1	1	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	AD	INSULATR
7	FMA	0	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	MT	INSULATR
8	FMA	0	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	MT	INSULATR
9	FMA	0	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	MT	INSULATP
10	EB2	2	6	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	VIC2TFIC
11	EB2	2	7	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	ELMIDCAP
12	RES	0	8	4100	5.80	30/1.0	32/5	4	350	500	6.0X8	CS	LCPMSEMI
13	EB2	4	8	2100	2.40	19/5	22/1	40	3000	3000	6.0X8	IN	LCPMSEMI
14	EB2	4	8	4100	2.40	19/5	22/1	10	1000	1000	6.0X8	IN	LCPMSEMI
15	EB2	4	8	4100	2.40	19/5	28/1	1	200	200	6.0X8	IN	LCPMSEMI
16	EB2	4	5	4100	7.30	19/5	28/1	2	300	600	6.0X8	IN	SO-DRAIN
17	EB2	3	5	4100	19.30	22/5	28/1	5	300	1300	6.0X8	AU	SO-DRAIN
18	EB1	1	4	4100	4.00	55/1.0	65/1	2	300	800	6.0X8	AD	INSULATR
19	EB1	1	4	4100	4.00	55/1.0	65/1	20	300	5800	6.0X5	AD	INSULATR
20	FMA	0	4	4100	4.00	55/1.0	65/1	5	300	5800	6.0X8	MT	INSULATR
21	FMA	0	4	4100	4.00	55/1.0	65/1	5	300	5800	6.0X8	MT	INSULATR
22	FMA	0	4	4100	4.00	55/1.0	65/1	5	300	5800	6.0X8	MT	INSULATP
23	EB2	2	3	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GATECAPG
24	EB2	2	11	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	GND-HIC1
25	EB2	2	12	3100	8.90	22/1.0	28/1	5	300	900	6.0X8	NI	HIC2VIC1
26	EB1	1	4	4100	4.00	55/1.0	65/1	20	300	3300	6.0X5	AD	INSULATR
27	FMA	0	4	4100	4.00	55/1.0	65/1	20	300	3300	6.0X8	MT	INSULATR
28	EB2	2	10	3100	8.90	22/1.0	28/1	5	300	1300	6.0X8	NI	EDGECONS
29	EB2	3	10	3100	19.30	22/5	28/1	5	300	900	6.0X8	AU	EDGECONS

Figure 5.27 Provisional common transistor recipe 4021.

RECIPE ID = RM4041

LYR	STA	H	M	GNTF	DENS	RP/RT	SP/ST	RATE	THK1	THK2	PRESS	MATL	MASK
1	EB2	2	1	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GND-HIC1
2	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GATECAPG
3	EB2	2	2	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	HIC2VIC1
4	EB1	1	4	4100	4.00	50/1.0	50/1.1	20	300	5800	6.0X5	AO	INSULATR
5	EB1	1	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
6	EB2	2	6	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	VIC2TFIC
7	EB2	2	9	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	POWRSEMI
8	EB2	2	7	3100	8.90	22/1.0	28/1.1	5	300	900	6.0X8	NI	ELMIDCAP
9	EB2	4	8	2100	2.40	19/1.5	22/1.1	40	3000	3000	6.0X8	IN	LGPWSEMI
10	EB2	4	8	4100	2.40	19/1.5	22/1.1	10	1000	1000	6.0X8	IN	LGPWSEMI
11	EB2	4	8	4100	2.40	19/1.5	22/1.1	1	200	200	6.0X8	IN	LGPWSEMI
12	EB2	4	5	4100	7.30	19/1.5	22/1.1	2	300	600	6.0X8	IN	SO/DRAIN
13	EB2	3	5	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	SO/DRAIN
14	RES	0	8	4100	5.80	30/1.0	32/1.5	4	350	500	6.0X8	CS	LGPWSEMI
15	EB1	1	4	4100	4.00	55/1.0	65/1.1	2	300	800	6.0X8	AO	INSULATR
16	EB1	1	4	4100	4.00	55/1.0	65/1.1	20	300	5800	6.0X5	AO	INSULATR
17	EB2	2	3	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GATECAPG
18	EB2	2	11	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	GND-HIC1
19	EB2	2	12	3100	8.90	22/1.0	28/1.1	5	300	700	6.0X8	NI	HIC2VIC1
20	EB1	1	4	4100	4.00	55/1.0	65/1.1	20	300	3300	6.0X5	AO	INSULATR
21	EB2	1	10	4100	8.90	20/1.0	28/1.2	5	300	600	6.0X8	AL	EDGECONS
22	EB2	3	10	4100	19.30	22/1.5	28/1.1	5	300	1300	6.0X8	AU	EDGECONS

Figure 5.28 The unprecedentedly short, 22 step, 2 hour, process 4041 featuring elimination of wait-steps, adopted as standard through the termination of the program.

of the vacuum system prevented complete fabrication of a circuit except for the top gate films. The transistors exhibited significantly less gain and substantially lower and variable threshold voltages. These results were not unanticipated and not subsequently reproduced, at least, deliberately.

One final minor process variation was introduced wherein circuit 135-6 was fabricated with the source drain pads between the cadmium selenide and the substrate instead of above both. The transistor characteristics were marginally better than any we had previously seen in all respects, particularly in providing breakdown potentials in excess of 550 volts and extraordinary uniformity of current leakage in the power and the logic devices, respectively.

Apart from minor variations in the process, concerning the edge connector metallurgy and mask precoating, it matured, as far as transistor fabrication was concerned, with recipes of the type shown in Figure 5.32. The only recommended change might be to insert steps 12 and 13, source-drain deposition, in between steps 18 and 19 to take advantage of the improvements in circuit performance likely in view of the discussion of the previous paragraph. The description of this topic concludes with a presentation in Table 5.16 of an overview of our accomplishments in this respect. It lists transistor characteristics extracted directly from the pilot facility log covering the last five runs conducted over a period of 20 days constituting the post-process development, "production phase" of our work.

We observe in Table 5.16 an apparently fairly smoothly running operation with circuits, all with excellent transistor characteristics, being produced at the rate of about thirty-two per month. Although this was about 50% better than at any time previously in the program, it should have been much higher. The reason was that the new circuit fabrication time had been reduced from over four hours to about two hours. In fact, the five circuits 169-1 through 169-7 were all fabricated in a single day! In addition, the theoretical capacity of

TABLE 5.16 Overview of transistor characteristics generated in a sequence of five runs constituting the final "production phase" of program activity

Line No.	Run No.	Substrate No.	Recipe No.	Transistor Characteristics									
				Power Device					Logic Device				
				I <sub>ON</sub> μa	I <sub>O</sub> na	I <sub>10</sub> μa	S	V <sub>BD</sub> volts	I <sub>ON</sub> μa	I <sub>O</sub> na	I <sub>10</sub> na	S	V <sub>BD</sub> volts
1	25	151-1	4026	1000	10	15	9/5	150-450	350	8	2000	10/7	300-550
2		151-3	4027	1000	7	12	9/5	400-500	400	5	8000	6/4	400-550
3		151-4	4029	1000	6	11	9/5	400-550	400	4	3000	6/4	500-550
4		151-5	4027	1000	5	10	8/5	150-500	400	3	3000	6/4	300-500
5	26	156-2	4031	900	4	1	8/5	200-450	300	2	120	9/6	350-400
6		156-3	4031	1000	7	3	8/5	250-550	300	2	120	7/6	350-500
7		156-4	4032	1000	6	5	8/5	400-550	350	2	200	9/7	250-450
8		156-5	4032	1000	5	5	9/5	350-500	350	3	250	10/7	350-500
9	27	156-8	4033	1000	6	10	9/5	200-500	350	3	300	10/7	350-500
10		159-1	4031	1000	8	8	8/5	200-550	250	5	400	8/5	200-550
11		159-3	4032	1000	8	8	9/5	350-550	310	4	300	10/7	450-500
12		159-4	4031	1000	10	16	9/5	500-550	350	6	600	5/4	500-550
13	28	159-6	4032	1000	12	12	9/5	450-550	400	6	400	6/4	450-550
14		169-1	4041	1000	10	6	9/5	400-550	300	4	600	8/6	500-550
15		169-3	4041	1000	10	11	9/5	450-550	400	7	1100	6/4	300-500
16		169-4	4042	1000	8	10	9/5	300-500	400	4	1000	6/4	300-450
17	29	169-5	4042	1100	8	12	9/5	300-600	400	4	4000	6/4	400-550
18		169-7	4043	1200	14	12	10/6	200-500	400	5	3500	6/4	100-450
19		172-1	4041	850	10	2	7/4	350-550	275	4	250	9/5	350-550
20		172-3	4041	800	9	15	9/4	250-500	325	5	4000	10/6	250-500
21	29	172-5	4042	700	7	10	9/4	400-500	275	4	500	9/6	400-500
22		172-4	4042	600	7	1	6/3	400-550	200	2	300	8/5	400-550

the machine was eight pieces per day, limited only by the accommodations for eight substrates which matched exactly the permissible sizes of the aluminum oxide hearths. In other words, the mask and process redesign of Phase III had permitted two circuits to be fabricated from each of four aluminum oxide hearths in the first electron gun beam system. The original mask design required two aluminum oxide mask operations generally constraining throughput to one circuit for each of the four hearths. What we believe we have convincingly demonstrated is the feasibility, with the existing equipment, of a throughput of eight pieces in three extended working days per week. This means a total of typically one hundred circuits, or fifty displays, per month, even providing one to two days down time between runs. The reason this demonstrated theoretical throughput rate was not achieved in practice is discussed in the next section.

In Table 5.16, all characteristics are listed as numerical averages except for the extremes of breakdown voltages, as indicated. We have also included for the first time the results of the dynamic leakage tests,  $I_{10}$ , described in Section 6.4, although the relevance of this particular test to circuit operation remains unclear, particularly within the context of the revised drive electronics scheme discussed in Section 9.5.

One final observation is in order prior to the discussion of the other component of the circuit, the busbar and transistor interconnect complex, which follows. This is the tendency for certain transistor characteristics to change systematically with the order in which each is processed within each run. For example, there seems to be a distinct tendency for  $I_{ON}$  of the logic transistor to increase. The breakdown voltage of transistors in the first circuit fabricated seems to be weaker than the subsequent ones. Finally, in some cases, leakage (reflecting threshold voltage) tends to range upward or sometimes downward consistently with the order of fabrication.



As far as the busbar and transistor interconnect component of the circuit is concerned, we have shown previously in Table 5.4.5 how the switch from aluminum to nickel busbars increased busbar impedance by a factor of two. However, no discernible effect on display performance was registered, either at that time or subsequently when, after the introduction of the new masks, nickel busbar segment thicknesses were reduced from 1000Å to 600Å. However, we were never really able to overcome all the factors blocking systematic fault-free busbar complex defects at any one given time, prior to the termination of technical activity. In the discussion which follows, we shall see, however, that we became rather close to doing so. Nonetheless, this shortcoming placed a formidable burden on the post-process manual repair activity described in Section 6.4.

We were very successful in Program Phase III in dealing with three major problem areas which had previously appeared at one time or another in Program Phase II. These were:

- cracked insulator films
- insulator underspray
- blocked apertures.

The well-known but not understood cracked insulator syndrome generates both shorts and opens at busbar crossovers, and capacitor and transistor active regions, as fissures develop in the aluminum oxide films. It almost exclusively affects only the first substrate processed in each run, but then does so catastrophically. During Phase III activity, we noticed its first appearance coincided with extremely damp weather. At about the same time, the building forced air supply was being switched from winter to summer control mode, and environmental humidity increased significantly. These observations led us to suspect water contamination of the aluminum oxide electron beam gun charges as the origin of the film fissures. We subsequently prevented its reoccurrence by additional conditioning of these sources during the preheat exercise as part of the run initiation procedure. This practice seemed less necessary during the very dry ambient conditions which prevailed during the winter.

Insulator underspray, in review, refers to the phenomenon which occurs when an insulator film is deposited between steps responsible for complementary segments of busbars. For example, a continuous busbar can be formed by depositions through two masks, each featuring complementing segments. If, for some reason, it is necessary to deposit one or more insulator films between the first and second segment sets, the first set can be contaminated by insulator underspray, thereby preventing electrical continuity with the second set. Underspray occurs because the heat of the aluminum oxide evaporation typically tends to warp the mask, destroying universal intimate contact with the substrate. During Program Phase II, insulator underspray was largely prevented by the cumbersome expedient of locating specially matching and patterned Kovar heat shields, or "back up" masks, between the relief side of the beryllium-copper cored patterning masks and the source. The Kovar cored patterning masks used in Phase III obviated this inconvenience. Their material selection naturally rendered them less susceptible to expansion in the first place. Secondly, the horizontal busbars, both gate and ground, were completely formed prior to, and again after, insulator deposition. Pattern geometry, moreover, required only one — not two, as previously — insulator depositions. However, the vertical (source) busbars remained vulnerable since, by necessity, the single insulator discrete film per cell had to be deposited between its corresponding segments. We declined to adjust insulator deposition rates because of the transistor collapse implications discussed in Section 5.4.2, and finally reluctantly resorted to an old trick of copper precoating the aluminum oxide mask in spite of undesirable implications on throughput rate. It required dedicating an electron beam hearth to copper, strictly for this purpose.

The resolution of open busbar defects generated by randomly blocked apertures by whatever cause was successfully overcome by exploiting features of the new pattern design. First, the new pattern design provided replication of the finally successful Phase II transistor recipe with ten instead of twelve masks, the maximum which could

be accommodated by the vacuum system. This freed up two mask stations for duplicates of the masks used for the formation of the horizontal busbars. As soon as a second set of horizontal busbar masks became available, they were installed in the two stations freed by the new mask design. The processing recipes were then modified to provide identical horizontal busbar patterns deposited through physically different masks. The idea was that the probability of an occlusion in one mask being exactly matched by a random occlusion in the second mask would be insignificant. As far as the horizontal busbars were concerned, this hypothesis was verified to the extent shown in Table 5.17.

Table 5.17

Frequency of Open Busbar Defects in Substrates  
Made with the New Masks Before and After Installation and Use of  
Duplicate Horizontal (Gate and Ground Busbar) Masks

	Average Defect Count	
	Before	After
Open (horizontal) grounds	13.3	2.2
Open (horizontal) gates	14.0	3.0
Open (vertical) sources	17.4	15.0
No. circuits in sample	15	5

The conclusions which were drawn from this data were that the duplicate horizontal busbar mask ruse worked well for open defects of that type, as intended. The qualitative nature of the improvement is important; 2 to 3 opens are easily repaired while more than 10 becomes too high a repair burden. On the other hand, the open source defect counts did not improve. This was expected since the only duplicate masks we had been able to use so far impacted the horizontal buses only.

This is the point where the importance of the work concerning the common transistor process formulation became paramount. Over and above implicit process simplification, it freed up yet a critical third

mask station to provide comprehensive duplication of all busbar segments. (It can be determined by inspection of the new mask geometries described in Section 4.4 that only one further mask station was needed for duplication of the vertical busbars.) Consequently, after verification of the common transistor process, we were able also to reduce dramatically the vertical busbar open count as portrayed in Table 5.4.17 which offers two observations. Firstly, process irregularities as depicted on the rightmost column have a major adverse impact on busbar continuity and, secondly, the state-of-the-art represented by the second through fifth circuits of 169 series substrates is about the best we achieved in a single run. With the exclusion of the processing irregularities as noted in Table 5.18, the overall impact of our attempts to deal with random mask aperture occlusions by the duplication of busbar segments is summarized in Table 5.19.

Where we were not able to improve on performance in Phase II concerned crossover shorts. Their origins have been discussed and nauseam in Section 5.4.1 and, in spite of all our cleanliness precautions, we were unable to substantially improve on circuit yield in this one respect. Although we made circuits with no shorts at all, and others with no opens at all, we were never able to do both at one time.

The overall impact of Phase III process development with the new masks is, however, underscored by the excellent statistics portrayed in Table 5.16 describing transistor performance and Table 5.19 representing improvements in open busbar defect reduction. This is further complemented by the impressive gains in throughput indicated in Table 5.20.

TABLE 5.18 Open busbar experience with the batches processed during the last two months of operations

Circuit No.	Open Defects Counts			Process Comment
	Vertical Source	Horizontal		
		Gate	Ground	
151-1	25	5	5	— EB gun short — Crystal failure
-3	17	5	5	
-4	1	2	1	
-5	0	0	0	
156-2	1	0	0	
-3	2	4	2	
-4	3	Not Meas.	0	
-5	1	1	1	
-6	0	0	0	
18	0	0	0	
159-1	5	5	4	
-3	1	1	1	
-4	1	2	1	
-6	0	1	0	
-7	8	4	1	
169-1	29	6	10	— Stopped to gold coat Al <sub>2</sub> O <sub>3</sub> mask
-3	0	1	0	
-4	2	0	0	
-5	0	0	0	
-7	1	0	1	
-6	42	1	0	
172-1	28	0	6	— } — } Operator error: — } mask misalignment — }
-4	41	0	0	
-5	18	0	0	
-3	62	6	5	

TABLE 5.19 Comparison of open busbar defect counts prior to and after the comprehensive duplicate mask process

	No. in Sample	Avg. Open Defect Counts		
		Source	Gate	Ground
Pre-duplication	15	17.4	14.0	13.3
Post duplication	29*	1.5	1.8	1.4

\* Except as noted in text

TABLE 5.20 Throughput-related parameters actually experienced in the last month of operations

	Best Phase II Experience with Old Mask/Process	Best Phase III Actual Experience with New Mask/Design*
Circuits fabricated per batch	5	7
Circuits fabricated per week	7	11
Processing time per circuit	4.1 hrs	1.9 hrs.

\* Last month of operations

### 5.5 Problems with Circuit Fabrication

All the substantial technical achievements in circuit fabrication process development and verification described in the previous Section were conducted in a chronic and pervading atmosphere of quiet desperation. The reason was that the centerpiece of our pilot facility, the automatic vacuum system described in Section 5.2, would never respond to our frantic and intense efforts to persuade it to get its act together. We simply quote from the contract-required Monthly Report for May 1979.

The single major difference in operating performance is in the negative gate voltage, and this is readily interpretable in light of the logic transistor test data. Logic transistors made with the common recipe had higher dynamic leakage than those made with the former differential doping recipe. We have consistently observed this difference in performance, but because the circuit continues to drive the phosphor adequately, the common transistor recipe has been accepted as standard.

This common transistor process, although shorter and requiring one fewer masks, is not in itself a technological breakthrough. What is important for our purposes is that it frees a mask station for duplicating the vertical busbars. At the time of writing, the first test of vertical busbar duplication is being made.

"As a final note, we have to report an extraordinary period of failures of the automatic vacuum system and errors with its operation. These are shown in Table 5.21. All the circuit fabrication activity described here has been executed against this backdrop of adversity. It has created something of a pressure cooker atmosphere, since we now have only four weeks to do what we planned to have ten for last October."

With reference to the last line in Table 5.21, the pilot facility log records that "pressure spikes" (later found to be due to a major failure in No. 2 electron beam gun system) forced termination

Table 5.21

Circuit Fabrication Setbacks Since the New Masks  
were Received on April 2, 1979

Batch No.	Date	Nature of Malfunction	No. Substrates
15	4-02	Mechanical failure of "actuator-up" sensor	2
16	4-10	Substrate wheel microswitch #7 failed	4
17	4-16	Operator loaded insufficient gold	4
18	4-23	Actuator indicator light connection broke	2
19	4-26	EB gun #1 power supply shorted	4
20	5-04	EB #2 vapor shutter jammed	1
21	5-10	Multiple failures of monitoring crystals	2
22	5-16	Mask wheel microswitch #2 failed	3
23	5-18	Premature failure of monitoring crystals	3
24	5-23	Mask misalignment - operator error	5
25	5-31	In progress	5

after only four circuits had been fabricated. In run 26, the actuator alignment mechanism failed. Runs 27 and 28 were terminated because of premature monitoring crystal failure. On July 3, 1979, program technical activity ceased on schedule when the automatic vacuum system was opened after a seemingly flawless run and we found piles of glass chips where there should have been substrates.



## 6. CIRCUIT TEST AND EVALUATION

### 6.1 Purpose of Circuit Test, Evaluation and Repair

Section 1 herein explained how the new mask and pattern design and procurement activity received top priority attention since it represented the critical path through the technical strategy formulated for the final eight month phase of the program. Subsequently, this activity lapsed into a period of waiting for mask delivery. Attention and effort were then shifted to the other four points of the final phase strategy which were:

- (1) Single metal (nickel) replacement of aluminum, copper, and chrome of the former process fabrication recipe.
- (2) Redesign of and rebuilding of drive electronics to lessen electrical stress on circuit matrix.
- (3) Characterization and, if necessary, development of phosphor and encapsulation methodology.
- (4) Reduction of the scope and method of pre-phosphor automatic circuit testing to a level more commensurate with critical program needs.

The remainder of the material in this section is divided into four subsections describing the circuit testing, evaluation and repair procedures which were developed during the third and final phase of the program. The topics covered are:

- Purpose of test, evaluation and repair.
- Classification of circuit defects.
- Evaluation procedures as they existed prior to the final eight-month phase.

- Details of the mechanics of the new test and evaluation procedure with an example of the case history of a particular circuit.
- Description of the pre-phosphor repair procedures.

If we were dealing here with development of manufacturing methods for a relatively mature product, one could argue that circuit evaluation and repair activity prior to application of phosphor and, perhaps also prior to encapsulation, might well be eliminated altogether. Ideally, the display could be assembled without any in-process testing and be subjected only to a final go/no-go test prior to delivery. However, what we have, in reality, is a low and highly variable yield and a less than fully-developed product. Thus, in-process evaluation and repair immediately after circuit deposition and prior to phosphor application serves four functions. These are:

- (1) Providing feedback to the vacuum system used for circuit deposition in a process control loop
- (2) Identifying defects and their characterization prior to fault clearing
- (3) Establishing essential requirements for drive electronics system development
- (4) Attempting to assemble some sort of picture of the economic viability vis-à-vis alternative fabrication methods.

Each of these will be briefly elaborated on in the remainder of this subsection.

A major manifestation of the immaturity of the current product is the continuing emergence of new ideas on its design and fabrication. Invariably, the analysis of each batch run produced at least one novel idea whose potential service to the program might have been substantial. One of the major difficulties in managing a program such as this is deciding

whether to follow up or discard such ideas, since all changes have to be evaluated in an orderly fashion. This in itself takes time, which, in recent months, has been a singularly precious commodity. Nonetheless, certain new ideas pass the most critical scrutiny; an example is the "duplication of bus-bars" concept. Another is the elimination of "wait" steps, etc. However, for every two "good" ideas, one typically wastes time on a poor one. The criticality of available elapsed time, the emergence of valuable ideas, and the limitation of an absolute minimum five-day cycle for processing a raw glass substrate into a finished display renders the interim circuit evaluation and test procedure of utmost importance. Such a procedure is extremely important for maintaining a vacuum system control loop in as responsive a mode as possible.

Besides the evident immaturity of the product, we are still confronted with immaturity of the manufacturing process. Defects in the circuit as fabricated by the vacuum system yet preclude the possibility of meaningfully applying phosphor to circuits without at least some pre-processing circuit repair. Whereas our repair techniques are quite primitive, they can be very effective in recovering circuits to drive phosphor dot displays which meet the viewability requirement spelled out by the contract. To be effective, however, each circuit must be thoroughly processed through a defect diagnosis procedure which is part of the circuit test and evaluation scheme.

Not only does the product and its manufacturing process remain in a relatively immature state, in the sense that ideas contributing to the development of both emerge continuously, the same also holds to a lesser extent with the drive electronics. Partly due to the inevitable continuing evolution of the product, and partly due to the increased scope of the circuit evaluation, the requirements for the drive electronics themselves evolve. Thus comprehensive circuit testing and evaluation plays a role indirectly in the design of the drive electronics systems. We might add here that earlier in the program, the drive electronics system had been frozen in a relatively unsophisticated state. Subsequently, substantial effort had been applied to trying to make the

displays drivable by the electronics. The spirit of the present approach is to recustomize the drive electronics as necessary to meet circuit requirements. The former, of course, is a much more mature technology and consequently all the more malleable.

The fourth purpose of circuit test and evaluation might be summarized as related to economics in two senses. Firstly, the phosphor application and encapsulation procedure, while relatively minor in terms of difficulty, has a limited capacity. One certainly prefers not wasting time encapsulating defective circuit modules. The other sense in which circuit test and evaluation relates to economics is that ultimately one wishes to establish the economic viability of this particular product-manufacturing system. To do this and compare it with alternative systems, one must have a good overall grasp of the state-of-the-art in order to make meaningful projections of the economic viability of any future larger scale operation. The circuit test and evaluation procedure we have recently developed certainly contributes substantially to the picture, although it may not be a particularly pleasant one.

## 6.2 Classification and Analysis of Defect Types

In Section 7 of the Eleventh Quarterly Report, display defects were discussed within the context of future yield improvements. However, some of that material is entirely appropriate also to this discussion of the classification and analysis of defect types and is being reproduced here for the purpose of completeness.

The technical strategy formulated for this final phase of the program implicitly hypothesized that the marginal visible success of prior work was largely attributable to the difficulty of fabricating a fault-free bus-bar complex. This is one of two components of the phosphor or dot matrix driving circuit. The other component is the assembly of identical, active, circuit switching elements located at the bus-bar intersections. The basis of the hypothesis is that a defect originating

during the synthesis of a particular elemental switching circuit generally affects the corresponding pixel only. We had earlier demonstrated that an 8 x 16 character half-display could accommodate up to 100 such defects and still meet contract viewability requirements. Furthermore, extensive experience had convinced us that over the long haul, the relative rate of appearance of such defects was typically less than 50 (out of 4480 pixels) and averaged more like 25. In addition, even during varied process experimentation over a course of 30 batch runs, we have never failed to make transistors capable of at least initially performing their required function.

On the other hand, a single bus-bar defect can "destroy" as many as 24 characters. A typical post-vacuum bus-bar defect count of as few as 10 can render an otherwise "perfect" display totally unreadable. Thus the essence of the stated hypothesis: visible success in the current program as evidenced by a copious flow of displays exceeding the 97% viewability requirement has been limited only by the difficulty of making a vacuum-deposited fault-free bus-bar complex. Next to this problem, transistor problems (including "stability"), real or otherwise, are minimal.

Consequently, redesign was highly directed at "bus-bar yield". Neither the new process "recipe" nor the mask redesign made any change in the transistor structure. We consider our modest success in routinely fabricating viewable displays (within limits permitted by an unprecedented and extended series of mechanical and electrical failures of the automatic vacuum system) a vindication of the hypothesis. That is, if our success has in any way been less than resounding, the reasons are:

- (1) The impact of defects on viewability is the major limiting factor of the manufacturing concept;
- (2) The most serious defect, by far, occurs in the bus-bar complex;
- (3) Defects in the elemental active circuits affect viewability performance relatively marginally;

- (4) At no time in this last phase of the program have transistor operating characteristics, their uniformity or reproducibility had any negative impact on reaching program goals.

These claims are, perhaps, subject to an exception which is illustrated in Figure 6.1. Strictly speaking, a short between the source and gate of the logic transistor at A produces much the same sort of result as bus-bar crossover short at B. Statistically one would not expect, and in practice one seldom observes, shorts at point A in the logic transistor. In any event, the short is treated as a local pixel defect rather than a bus-bar defect because it can be corrected simply by disconnecting the logic transistor at point C. Admittedly, this disables control of the pixel, but again, the present state-of-the-art is such that meeting contract requirements is not limited in any way by the local defective pixel element count. Naturally, this recourse is not available if the quest is only for a 100% "perfect" defect-free display. The spirit of the present program was not seriously directed at this next higher level of performance.

Having thus distinguished between bus-bar and local defects, we can proceed to further breakdown and classification of the former. To repeat, bus-bar defects constitute the chief and only obstacle to highly visible success in meeting the written requirements of the present program.

As a reminder, bus-bar defects can be broadly classified into two categories: open bus-bar lines and short circuits between crossing bus-bar lines. The nature of the new bus-bar complex is illustrated in Figure 6.2 with a four-character simplification, simply for the purpose of exposition. One can mentally project the pattern to a full 8 x 16 character array and apply subsequent discussion to this or any larger picture.

The bus-bar defect classification is explicitly listed in Table 6.1 where local defects of all kinds are accumulated under Type VI.

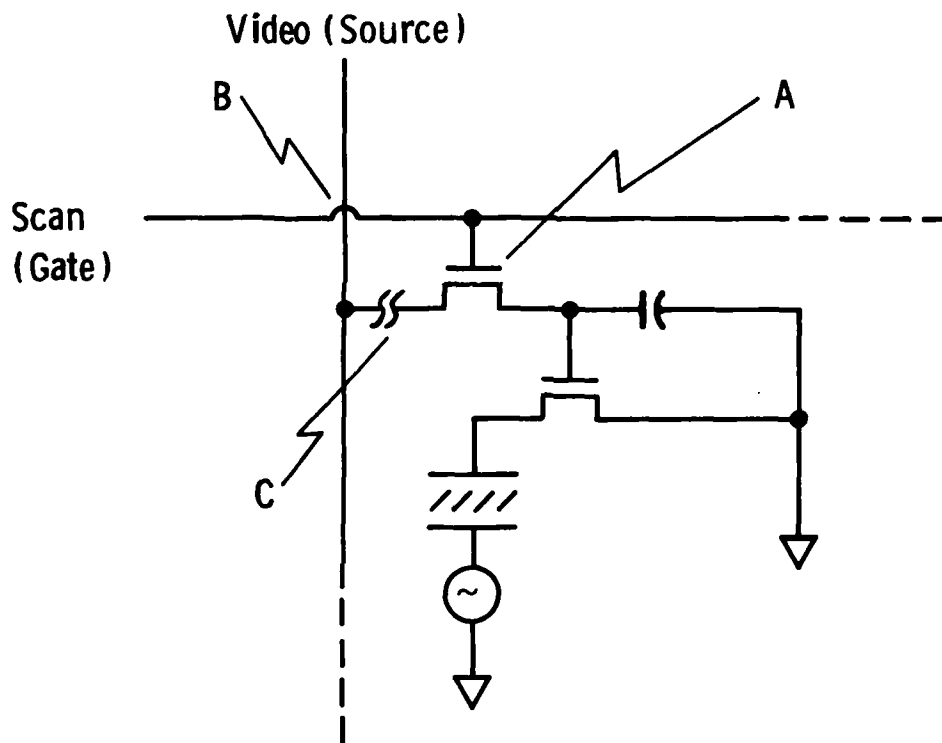


Fig. 6.1 Disconnection of the logic transistor source at C to correct for source to gate shorts at point A.

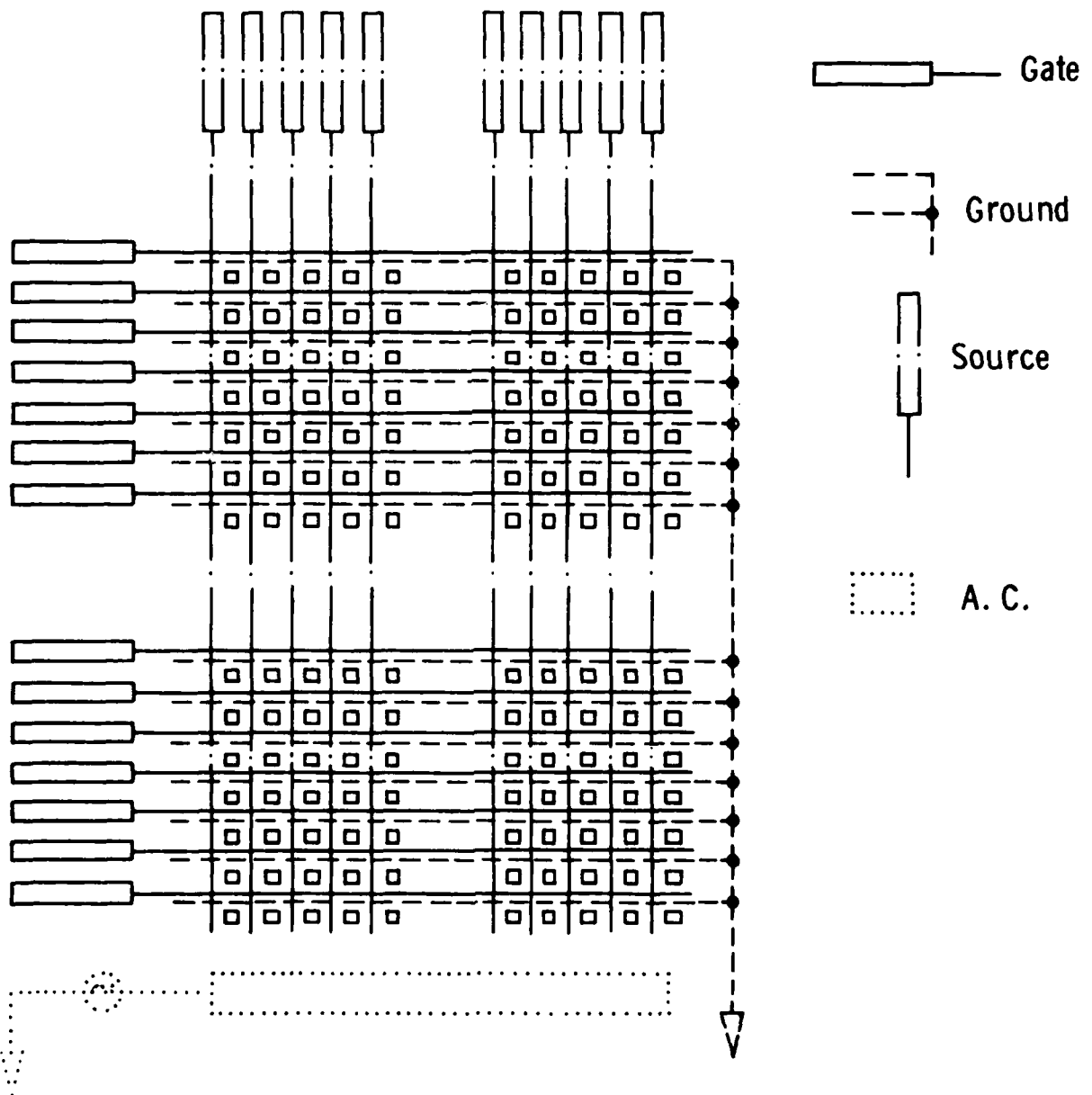


Fig. 6.2 Basic features of the layout used in Program Phase III with no provision for fault tolerance.



TABLE 6.1 CLASSIFICATION OF BUS-BAR AND LOCAL  
DEFECTS.

<u>Type Number</u>	<u>Circuit Component</u>	<u>Description</u>
I	Bus bar	Source opens
II	"	Gate opens
III	"	Ground opens
IV	"	Source-ground shorts
V	"	Source-gate shorts
VI	Local	All

This is because our practice in dealing with them is in every case simple surgical disconnection, as exemplified in Figure 6.1. In fact, the classification in Table 6.1 reflects, in general, more the method of treatment of the defect than the physical reason for its origination.

In the following discussion the terminology "old" and "new" will be used to distinguish between events prior to and after our beginning work with the new mask design and construction, consistent with the narrative of the Eleventh Quarterly Report.

#### Type I. Bus-Bar Defect - Source Opens

Along with defect Types II and III, these have historically been the most troublesome in terms of disabling the display. Their impact can, in principle, be overcome by location and repair. Although we have recently speeded up the repair operation substantially, as described later in Section 6.4 it remains basically a labor-intensive and unreliable process rather unsuited for any kind of pilot manufacturing operation. Consequently, our recent success in reducing the occurrence source opens to a manageable level (also described in Section 6.4) has been of major importance.

The origin of source-open defects can be most recently ascribed to three different causes:

##### (1) Cracked Insulators

This well-known but not understood syndrome prevents bus-bar continuity as post-processing fissures develop in the insulator films. In recent experience we attributed it to the sudden onset of extremely damp weather which the environmental control could not completely cope with. We prevented it by preheating the  $Al_2O_3$  EB gun well system, a practice which apparently was not necessary during the very dry ambient conditions which prevailed during the winter.

##### (2) Insulator Underspray

During earlier "nickel recipe" development, we discontinued the practice of loading a copper charge during prefabrication preparation.

This made it necessary to perform the copper precoating of the insulator mask (we now use only one) in a secondary vacuum system. The purpose of the copper coating is to radiate heat from the mask during  $\text{Al}_2\text{O}_3$  evaporation. Several times we have tried to avoid having to do this in the belief that the new Kovar mask construction would be the final solution; however, it wasn't. Without the copper precoat, even the new masks still warped, although not as severely as the former Be-Cu-cored ones. In any event, the outcome is the same. Intimate contact between mask and substrate is best, and insulator material contaminates unformed bus-bar segment junctions. However, as a consequence of the "three-layer approach" discussed in Section 4, only the source and not the ground or gate buses are affected by this mechanism. Thus we can claim assertively that with transposition of the "non-overlapping" source bus segments from the horizontal bus masks to a mask used in the central layer, the problem would reduce to the same level of insignificance experienced with the horizontal buses.

Whereas we have prevented chronic reoccurrence of the problem by reverting to copper precoat of the  $\text{Al}_2\text{O}_3$  mask in a secondary vacuum system, it still mysteriously persists to some extent, but only in the first substrate of a batch processed. The method of clearance of the fault is, however, particularly easy, even in this case, as long as it is not too extensive.

### (3) Blocked Mask Apertures

There are two types of occlusion:

(a) Debris originating from pre-process or in-process sources. The defect distribution is geometrically random. Until recently, it has been difficult to prevent. Generally, the resulting defects are not too easy to correct.

(b) Defective mask construction. This generates open defects easily identified by their common location on different substrates. Whereas the difficulties they cause can usually be prevented once discovered, they are as difficult to repair as (a) above.

Operationally, we observe the open section of a source bus usually generating permanently "OFF" pixels. We have not determined precisely why this is so, but one could argue that leakage to ground through a logic transistor in series with a leaky capacitor is responsible.

#### Type II. Bus-Bar Defect - Gate Opens

These differ from the source open defects in basically two ways. First of all, there is no possibility of insulator underspray since all segments of the bus are deposited sequentially with no intervening  $\text{Al}_2\text{O}_3$  deposition. Otherwise, their causes correspond to those for Type I defects. Secondly, an open section of the bus-bar often results in a permanently lit line. Again, the precise reason is not known. One can speculate, however, that the open gate section floats up to the average video level imposed on intersecting source lines due to coupling through the source-gate crossovers. Generally, gate opens are the least common of all bus-bar defects with the new pattern. This is consistent with the interpretation of their predominant cause as the occasional cracked insulator. Central parts of the insulator segments where the gate buses lie are statistically less likely to be affected by a crack.

#### Type III. Bus-Bar Defect - Open Grounds

The causes and frequency of these defects correspond very closely to those for the other horizontal (gate) buses, with two exceptions. First, they tend to be somewhat more frequent, which again is consistent with the interpretation of their direct cause as the occasional cracked insulator. The ground buses pass closely to one edge rather than through the center of the insulator segments. They also differ phenomenologically from gate opens because they tend to generate permanently off pixels. This is most likely because there is no path to ground for the phosphor excitation current.

#### Type IV. Bus-Bar Defect (Source-Ground Shorts) and Type V (Source-Gate Shorts)

These types are caused by a whole variety of reasons which have been discussed ad infinitum in earlier quarterly reports. Their

average frequency has remained essentially the same as it was before the new mask and pattern design.

Although undesirable, they are not usually limiting at present because they are usually clearable once located. Our recent activity in this area has been, therefore, learning how to live with these defects; in particular, how to locate and clear them. Unlike the situation with open defects, the new mask design does not provide direct relief from the basic problem of shorts.

#### Type V. Display Defect - Local Pixel Faults

Let it again be emphasized that this sixth defect type, associated with the elemental circuit transistors and capacitor, does not occur at a frequency which limits our capability routinely to make displays to pass the viewability requirement as spelled out in the contract. In fact, in the last quarter we did not fail, at any time, to fabricate transistors adequate to drive phosphor dots in a mode consistent with the basic viewability requirement. However, defects do occur at rates between five and fifty in a typical display and are totally undesirable, if only from an aesthetic viewpoint, since they result in permanently "ON" or permanently "OFF" pixels. They are, in addition, more serious in a way than the Types I through V bus-bar defects, because preventing them entirely is much more technically demanding in the long run. Some of the more common direct causes of permanently "ON" pixels are.

- (1) A short between the power device gate and drain causes it to behave as a forward conducting diode effectively shorting the respective EL pad to ground;
- (2) A power device semiconductor channel short likewise provides a direct path to ground from the EL pad. This condition can be induced by excessively high phosphor excitation voltage.

Permanently OFF pixels are caused by:

- (1) A shorted capacitor resulting in sub-threshold drive of the power transistor;

- (2) A drain-gate short in a logic transistor will result in average negative gate drive voltage being impressed on the gate of the power transistor with the same result as in (1) above.

Note that the analysis above deals exclusively with the impact of shorts. Our experience with the new mask design suggests that open circuits in the elemental switching circuits are much less common, although they will generate either permanently "ON" or permanently "OFF" dots, depending on their precise location.

One final remark concerns the so-called "rabbit track" defects described in the Eleventh Quarterly Report. Since working with the new Kovar-cored masks, we have never observed such defects. They seem to have disappeared as mysteriously as they appeared. At least we have support of the earlier suspicion that they were somehow related to mask construction.

### 6.3 Earlier Approach to the Task

In Section 6.1 four reasons for the overall circuit test and evaluation procedure were announced. Among these, the second has been of prime importance during the current reporting period. It relates to systematic identification and location of circuit defects prior to pre-phosphor repair. The procedure we finally developed, and will describe in the next section, is directed principally at serving this purpose. However, a review of the approach used for the same task, earlier in the program, is in order here. Some of the material was presented in the Eighth Quarterly Report.

Early in the program, an automatic tester was built and installed in the pilot facility in order to provide quality control measurements on the circuits. Electrical contact to the circuits is achieved by an Electroglas Model 1034X wafer probe which is used widely by manufacturers of silicon integrated circuits. Our unit is shown in Figure 6.3. This device contains twenty micropositionable probes mounted in a stationary ring, and a motor driven vacuum chuck to hold the substrate. The chuck is



Fig. 6.3 Electroglass model 1034X wafer probe.

mounted on air bearings and driven by precision linear motors in the X and Y (horizontal) directions, and by a motor-driven cam in the Z (vertical) direction. Electrical stimuli to the components under test are provided by programmable dc power supplies and a programmable oscillator. Programmable resistors provide loading and biasing, and a digital multimeter measures component response. The instrumentation is connected to the probes by a custom-designed 12 x 24 reed relay matrix capable of switching 500 volts with a minimum open impedance of  $10^{12}$  ohms. The wafer probe, switch matrix, and instrumentation are all driven by a control computer which accumulates test data on magnetic disc for further processing. The test procedure is similar to the vacuum deposition process procedure in that the test software operates on a test "recipe" which can easily be modified or edited by the test operator.

A software package for this system was written and verified. It includes:

- (1) a recipe editor to create new and to modify existing, test recipes;
- (2) test programs to
  - operate from a prescribed recipe
  - control and monitor the instrumentation--namely, the relay matrix and the probe mechanism.
  - log the test data.
- (3) programs to operate on the test data off-line.

Item 3, above, includes a routine to format the test data into a "map" of substrate addresses where a particular test parameter may be out of specification. An example of this output appears in Figure 6.4. Additional software has been written to perform statistical analysis of the data frequency distribution and to perform defect analysis such as defect location correlations to separate mask-induced defects from randomly distributed process-induced defects. An example of a computer-generated frequency distribution of source bus impedance is shown in Figure 6.5.

Generally, this approach was well conceived and was implemented with a high degree of persistence and technical sophistication. In spite



TEST 4 CONT-GATEBUS  
TEST 4 CONT-GATEBUS

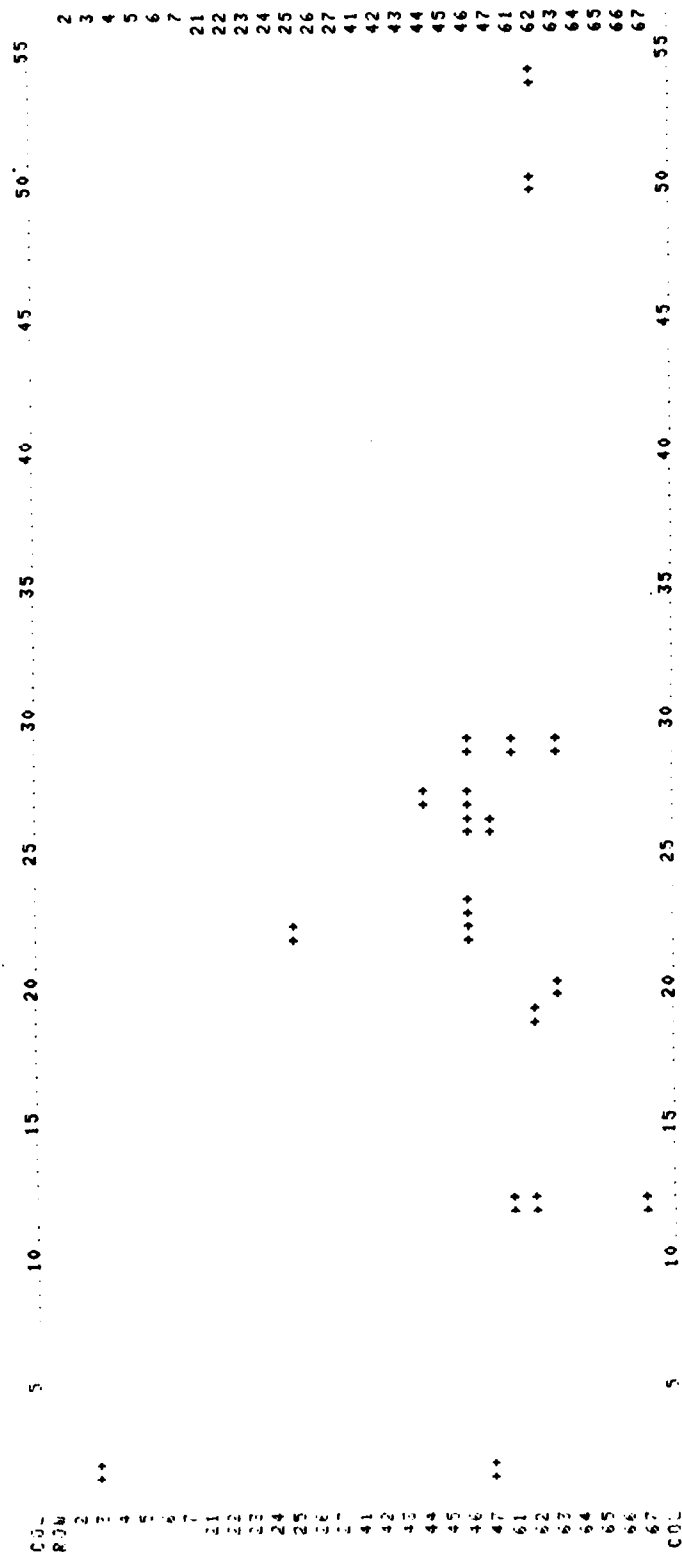


Figure 6.4 An example of computer-generated defect mapping of gate bus discontinuity.

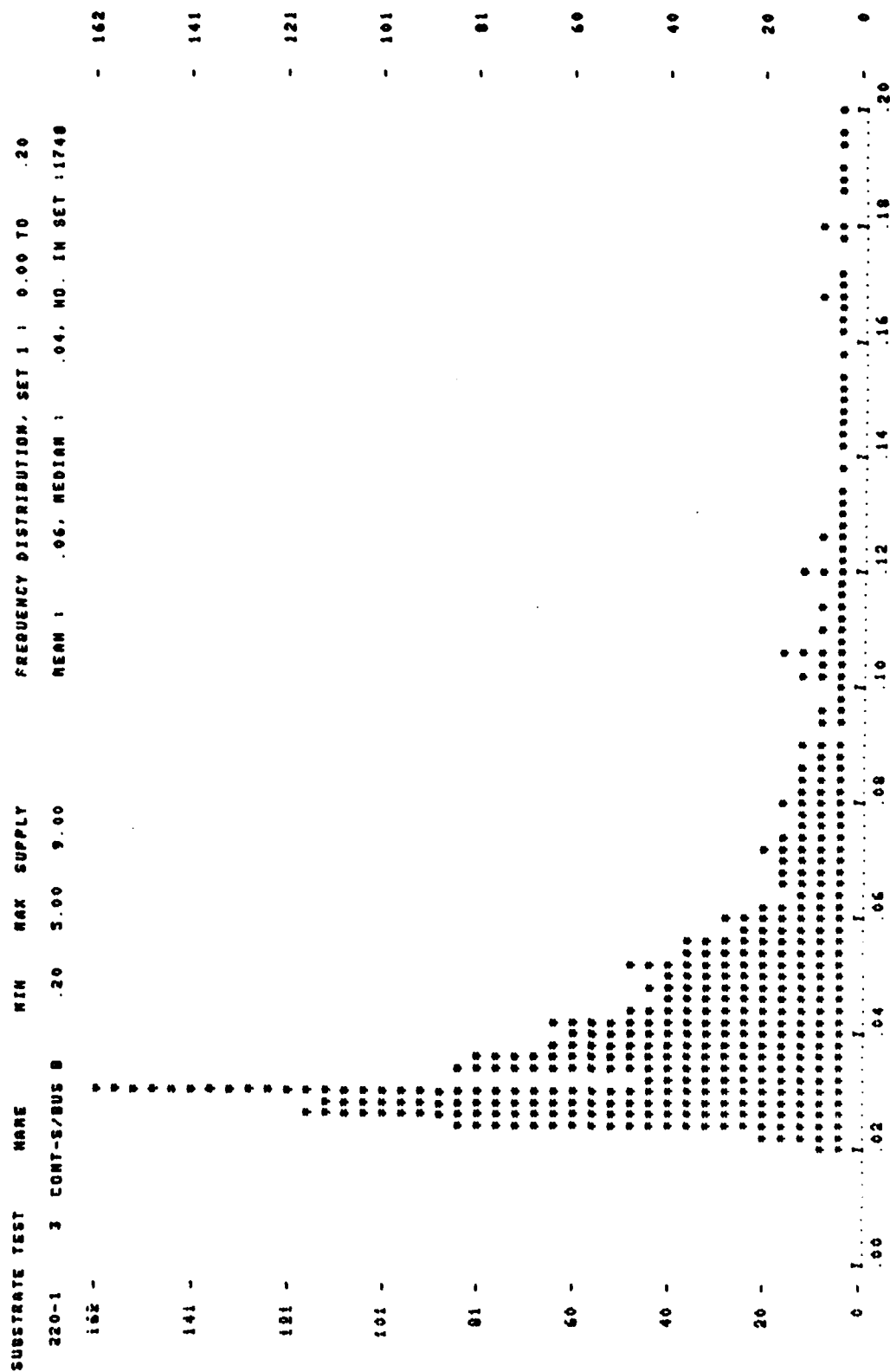


Figure 6.5. Example of a computer generated defect frequency distribution of source bus local impedance.

of this, we failed to render it operational and discontinued its use during Phase III for several reasons:

- (1) substrate glass flatness requirements
- (2) interpretation of transistor test data
- (3) inadequate throughput.

The only substrate glass we had been able to obtain in sufficient quantity at acceptable cost had not been flat enough to meet the requirements of the probe locating and lowering system. Generally, either one or more probes had failed to contact the circuit, or one or more had overtravelled and plowed up metallization films, often to an extent which subsequently rendered a circuit inoperable.

Historically, transistor test data has been acquired manually with a curve tracer. Such testing, however, does not properly simulate end-use conditions. The automatic tester, however, was naturally designed as far as possible to simulate such conditions. However, whereas substantial empirical experience has been accumulated to relate manual testing data to eventual circuit performance, the same had not been done for the numerical data extracted by the automatic tester. In view of the very light manning level we had to maintain on the program during the third phase, we chose to stay with tried-and-true quasi-manual data-logging.

Finally, when the original automatic data-logging system was instituted, vacuum system throughput was about four batches per month, each batch generating four to five circuits. When the mask and pattern redesign task was complete, it was evident that, something approaching twice this throughput level would result. Consequently, some supplementary testing capacity had to be developed anyway. What we did was to evolve the system of manual testing and data-logging which will be described in the next section.

#### 6.4 The Final Circuit Evaluation and Repair Procedure

Although circuit evaluation and repair activity has been pursued since the very first display circuit was made several years ago,

only in the third phase of the program was the procedure systematized into a form appropriate to a rudimentary pilot production facility. What we had earlier was a sophisticated automatic test system which had failed operationally for reasons discussed in Section 6.3. This was supplemented by an unstructured, manual, and a very labor-intensive, test and repair procedure using several technicians and extensive engineering time of sixty or more hours per month. During Phase III, this was transformed into a one-technician systematized operation providing twice the throughput rate at the cost of a non-recurring investment of forty engineering hours. The system is not particularly sophisticated or polished but it is very effective. It is directed almost exclusively at bus-bar defect identification and location. The actual repair procedure itself remains basically, but not entirely, unchanged. This is not through choice but by necessity -- a consequence of the severely reduced manpower level.

At the outset, we recognized that something drastic had to be done in the circuit test, evaluation, and repair activity in order to increase productivity for reasons stated above. However, at the same time we had several factors going for us:

- (1) Productivity was limited principally by defect-identification and location rather than repair itself.
- (2) The new pattern design provided easily accessible test transistors.
- (3) The pads on the test transistors were very large and were not functional parts of the circuit.
- (4) The pads were made from nickel which was known to be significantly harder and more scratch-resistant than the former aluminum bus-bars.
- (5) Bus-bar lines also were provided with special large scratch-resistant pads.
- (6) Our Electroglas prober was potentially very effective even when used in the manual mode, which it never had been previously.

- (7) Much defect analysis was ideally suited for execution by custom-designed but essentially straightforward digital circuitry.

Our overall approach was, therefore, to:

- (1) Use the Electroglas prober in a manual mode to access test transistors for test by conventional curve tracer.
- (2) Device a means whereby the Electroglas prober could be readily used (a) to detect open bus-bars and (b) to locate precisely bus-bar opens (all 3 types) and source-ground shorts.
- (3) Design and build an automatic short tester with an address display feature to locate precisely source-gate shorts and identify source-ground shorts.
- (4) Format a set of readily interpretable data-logging forms to (a) capture process control information and (b) determine the extent of, and to schedule the repair procedure.

The description of the execution of this approach will be described here in the following order:

- (1) Introducing the blank data-logging forms and the operating philosophy.
- (2) Demonstrating the use of the forms with the case history of a particular circuit.

A total of nine different forms are used and they are shown at approximately 60% of actual size in Figure 6.6A through 6.6I. The captions of these figures give a brief introduction to the operating mode.

Ordinarily, a booklet of these sheets is compiled with two copies of the horizontal bus open test (Figure 6.6C) and four of the short test (Figure 6.6D) and assigned to the substrate on its removal from the annealing oven. The operator, in general, works from sheet-to-sheet indicating his progress on the schedule (Figure 6.6A) for ready reference as he progresses. Obviously, this looks rather cumbersome and we would, by far, prefer to have a copious supply of defect-free circuits emerge from the vacuum system and eliminate the need for all this paper. However, the system has improved overall productivity by a factor of at least five. While there is still room for further improvement, perhaps using a computer based system, what we have here represents a sensible trade-off between desirability and possibility. One reason it is being described here in detail is that it is a convenient reference against which to present summary data for reporting purposes. Secondly, it might also form the basis for more efficient systems to be developed by future workers in this area.

On removal of substrates from the annealing oven, the first test conducted is a short test using the custom designed and built equipment shown in Figure 6.7. The electrical schematic is shown in Figure 6.8. To use it, the operator installs a circuit (or phosphorized half-panel) in the special fixture and presses the "start" button. The electronic system scans all bus-bars in sequence and as soon as a short is detected, disables the scan and displays the address of the short in alphanumeric code. The operator notes the address of the short on the assigned form shown in Figure 6.6D and pushes the "start" button again to continue the scan. If no shorts are detected, the scan of all 8960 crossovers is completed in about 20 seconds. With a typical number of

CIRCUIT

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EVALUATE AND REPAIR SCHEDULE

- Pre-Anneal Short Test
- Post Anneal Short Test
- Transistor Test
- Source Opens
- Gate Opens
- Ground Opens
- Locate Ground Shorts
- Locate Source Opens
- Locate Gate Opens
- Locate Ground Opens
- Draw Map
- Write up Repair Schedule
- Make Repairs
- Exercise
- Clear to EL
- Receive from EL
- Test Shorts
- Locate Opens
- Write up Repair Schedule
- Make Repairs
- Viewability Test
- Clear to Encapsulate

Figure 6.6A Cover sheet of form set used for ready appraisal of state of evaluation.

SOURCE BUS CONTINUITY TEST																DATE	CHARACTER COLUMN NO.	
12	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	CHAR	DOT
13	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	DATE	
23	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
34	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
35	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
45	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
46	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
56	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
57	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
67	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
68	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
78	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
79	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
CHECK	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	SUBSTRATE NUMBER	
IF																		
DOT																		
CONTINUITY																		
OK																		

Figure 6.6B Format used for recording source bus continuity



# HORIZONTAL BUS CONTINUITY TEST

POSITION	L R	L R	L R	L R	L R	DO NOT CHECK THESE PROBE PLACEMENTS	CHECK IF OK. ROW NO.
ROW NO.	1	2	3	4	5	7 8 9 10	1 2 3 4 5 6 7
1	12.13	23.24	34.35	45.46	56.57	67.-	
2							
3							
4							
5							
6							
7							
8							

OPENS REPAIRED (ENTER ROW NO.'S)

CHAR	DOT	DATE	CHAR	DOT	DATE

SUBSTRATE NO.

CHECK ONE

COMMENTS

☐ GATE

☐ GROUND

Figure 6.6C Horizontal (gate and ground) bus continuity coding sheet.

## SHORT TEST

- □ □

### Substrate

Date \_\_\_\_\_

Short Test No.

[illegible]

DECODER	9	A	b	C	d	E	F
(do not add).	10	11	12	13	14	15	16

302

# DMD TRANSISTOR TEST

☐ ☐ ☐  
CIRCUIT NUMBER

DATE

## POWER DEVICE

LOCATION		LEAKAGE		$I_{ON}$	S	$V_{BD}$	
SOURCE	GATE	$I_o$	$I_{io}$				

## LOGIC

LOCATION		LEAKAGE		$I_{ON}$	S	$V_{BD}$	
SOURCE	GATE	$I_o$	$I_{io}$				

Figure 6.6E Transistor test data sheet.

**REPAIR ANALYSIS CHART** TM 5-10

		DEFECTS USING RED																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
1	<u>GATES</u> USE <u>GREEN</u>	1																
		2																
		3																
		4																
2	<u>GROUND</u> (COMMON) USE <u>BLACK</u>	1																
		2																
		3																
		4																
3	INDICATE CUTS WITH BROKEN LINES OF PROPER COLOR.	1																
		2																
		3																
		4																
4		1																
		2																
		3																
		4																
5		1																
		2																
		3																
		4																
6		1																
		2																
		3																
		4																
7		1																
		2																
		3																
		4																
8		1																
		2																
		3																
		4																

INDICATE OPENS TAGS REPAIRED WITH BLACK O  
 INDICATE SHORTS WITH BLUE + (CIRCLE WHEN FIXED)

SUBSTRATE   
 DATE

Figure 6.6F Repair analysis chart for mapping defects.

CIRCUIT ☐ ☐ ☐ ☐

DATE

# REPAIR SCHEDULE

☐ BEFORE EL

☐ AFTER EL

## SOURCES

S	G/C	✓

O  
P  
E  
N  
S

## GATES

G	S	✓

O  
P  
E  
N  
S

## GROUNDS

C	S	✓

## BUS BAR SURGERY


NEW OPENS

## SOURCE-GATE

S	G	✓

S  
H  
O  
R  
T  
S

## SOURCE-GND

S	C	✓

Figure 6.6G Repair schedule developed from defect map on repair analysis chart.

SOURCES	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	EL
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
		GATES						

Figure 6.6H Coding sheet for lit display test message.

# VIEWABILITY TEST SHEET

SUBSTRATE \_\_\_\_\_

DATE \_\_\_\_\_

ALL DOTS ON

ALL DOTS OFF

MESSAGE

BIAS VOLTS	S+	S-	G+	G-	EL VOLTS

Figure 6.6I Viewability test sheet.



Figure 6.7 The custom designed and built DMD half-display circuit short-tester.



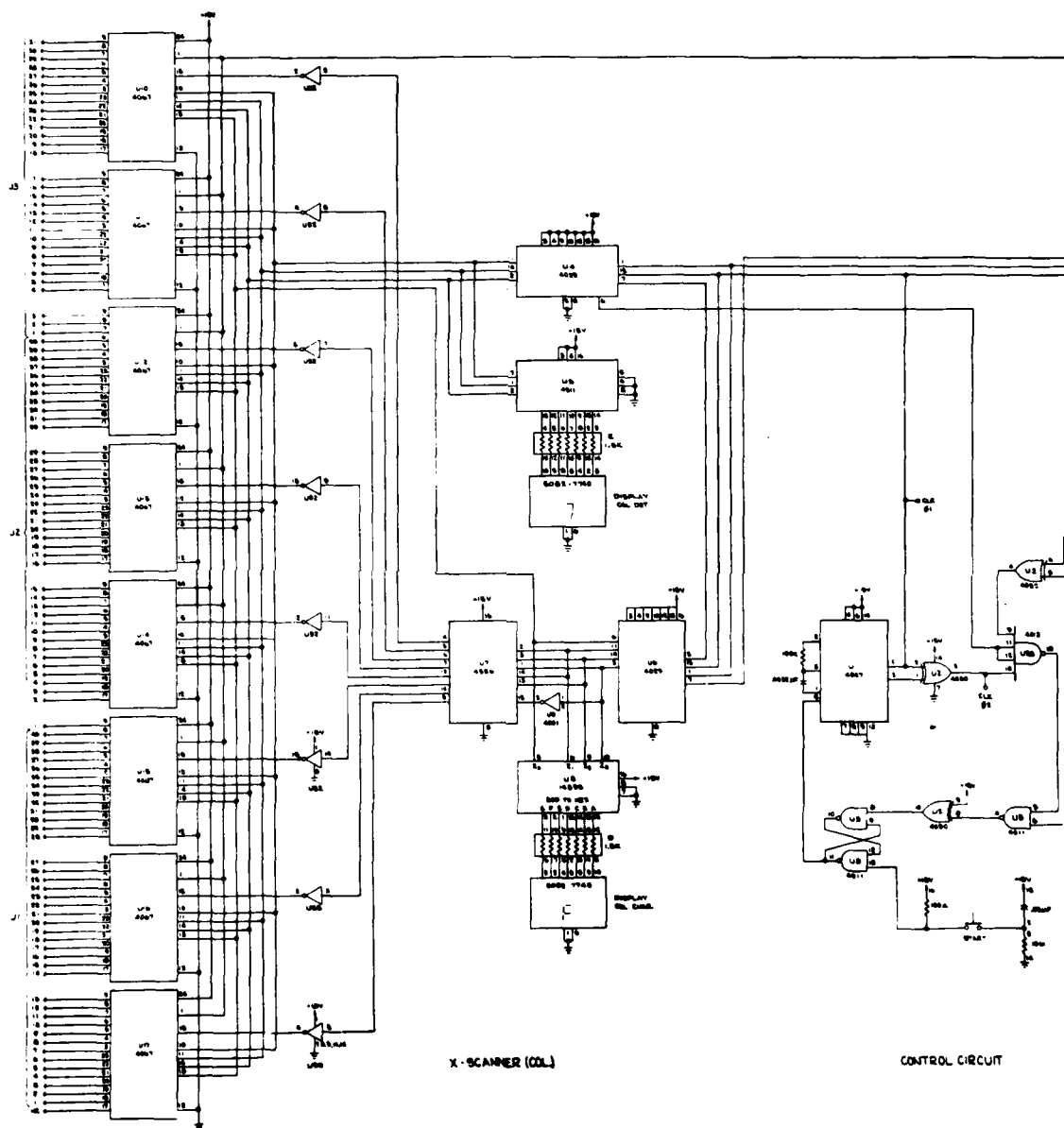


Figure 6.8 The electrical schematic of the custom designed automatic short tester.



shorts the operation lasts about two minutes. The completed docket cover form of sample 9-151-4 is shown in Figure 6.9 and the results of the short test in Figure 7.0.

There are now several points to be covered related to the test results shown in Figure 6.9 which are:

- (1) Sample Identification Number.
- (2) Bus-bar addressing scheme.
- (3) Conversion of tester display data.
- (4) Identification (but not location) of source-ground shorts.
- (5) "Ghost" shorts.
- (6) Further levels of automation.

During the final eight-month phase of the program we have retained the existing sample identification scheme. This is illustrated by example in Figure 6.11. The first two parameters, 9-151 in this case, are scribed into the substrate glass on the pattern side in the lower left corner. The substrate position, in this case 4, is scribed into the lower right corner. This is always done immediately as the substrate holder is removed from the vacuum system and before the substrate itself is removed from the holder. We are not entirely happy with the scribing technique because, on occasion, substrate glass cracks have appeared during encapsulation and these cracks may have been seeded by the scribing.

The bus-bar addressing scheme is illustrated in Figure 6.10. The source-to-gate shorts detected by the tester are specified on the left-hand side of Figure 6.10 by S and G numbers. The precise location of short S15.4, G2.2 is shown in Figure 6.13, which represents the upper right-hand portion of the layout shown explicitly in Figure 6.12.

When the short testing equipment shown in Figure 6.7 was built, we decided to make it fully compatible with a future graphics display with essentially the existing dot format. Consequently, the display

## CIRCUIT

9	151	4
---	-----	---

EVALUATE AND REPAIR SCHEDULE

<input checked="" type="checkbox"/>	Pre-Anneal Short Test		
<input checked="" type="checkbox"/>	Post Anneal Short Test		
<input checked="" type="checkbox"/>	Transistor Test	6-2-79	First circuit with common xstor recipe & 1 3/4 hr. process 6-01-79 <u>          </u>
<input checked="" type="checkbox"/>	Source Opens	"	
<input checked="" type="checkbox"/>	Gate Opens	"	
<input checked="" type="checkbox"/>	Ground Opens	"	
<input checked="" type="checkbox"/>	Locate Ground Shorts		
<input checked="" type="checkbox"/>	Locate Source Opens		
<input checked="" type="checkbox"/>	Locate Gate Opens		
<input checked="" type="checkbox"/>	Locate Ground Opens		
<input checked="" type="checkbox"/>	Draw Map	6-04	
<input checked="" type="checkbox"/>	Write up Repair Schedule	6-07	
<input checked="" type="checkbox"/>	Make Repairs		
<input checked="" type="checkbox"/>	Exercise		
<input checked="" type="checkbox"/>	Clear to EL	6-8-79	
<input checked="" type="checkbox"/>	Receive from EL	6-11-79	
<input checked="" type="checkbox"/>	Test Shorts	OK ①	
<input checked="" type="checkbox"/>	Locate Opens		
<input type="checkbox"/>	Write up Repair Schedule		
<input type="checkbox"/>	Make Repairs		
<input checked="" type="checkbox"/>	Viewability Test	6-11-79	
<input type="checkbox"/>	Clear to Encapsulate		

Figure 6.9 Cover sheet for test docket of circuit 9-151-4.

CHIEF, ONE

Before Exercise: Phosphor

LI After Exercise balance Phosphor

- 1) Car Phosphate before Exercise

n) After Phosphor after Exercise

## SHORT TEST

9 151 4

Substrate

6-279

14

Date

Short Test No.

[illegible]

## DECODER

DECODER	9	A	b	C	d	E	F
(do not add).	10	11	12	13	14	15	16

Figure 6.10 Results of post-anneal short test of sample 9-151-4.

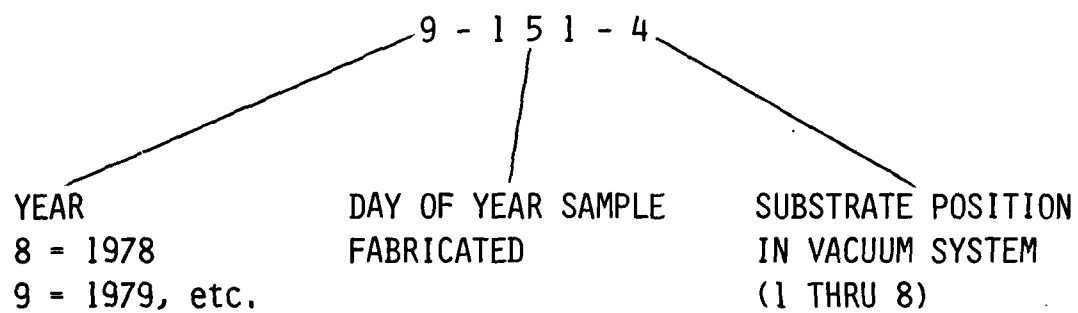


Figure 6.11 Example of circuit/substrate identification.

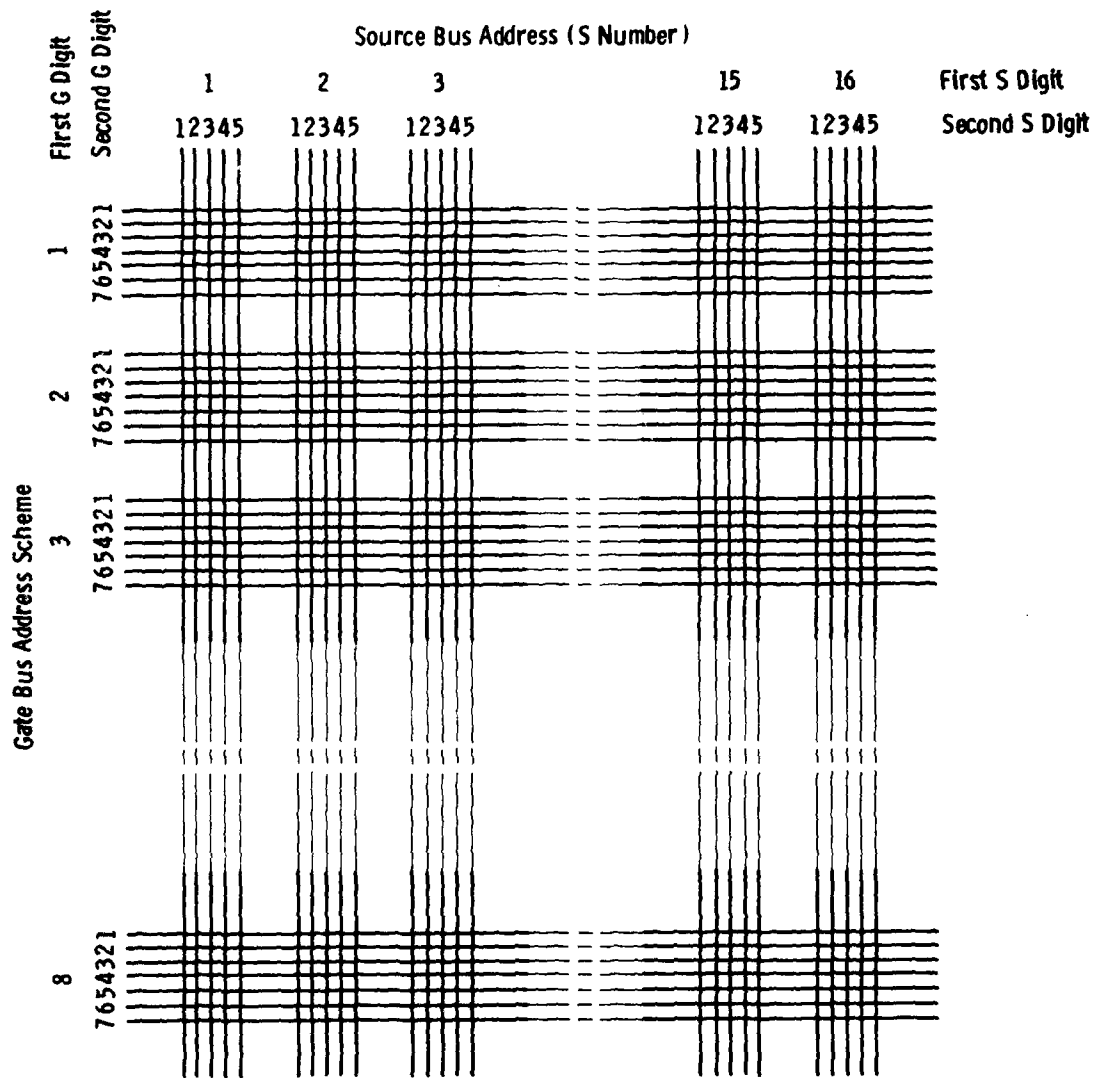


Figure 6.12 Bus-bar addressing scheme 8x16 character half-display circuits.

Dwg. 7699A03

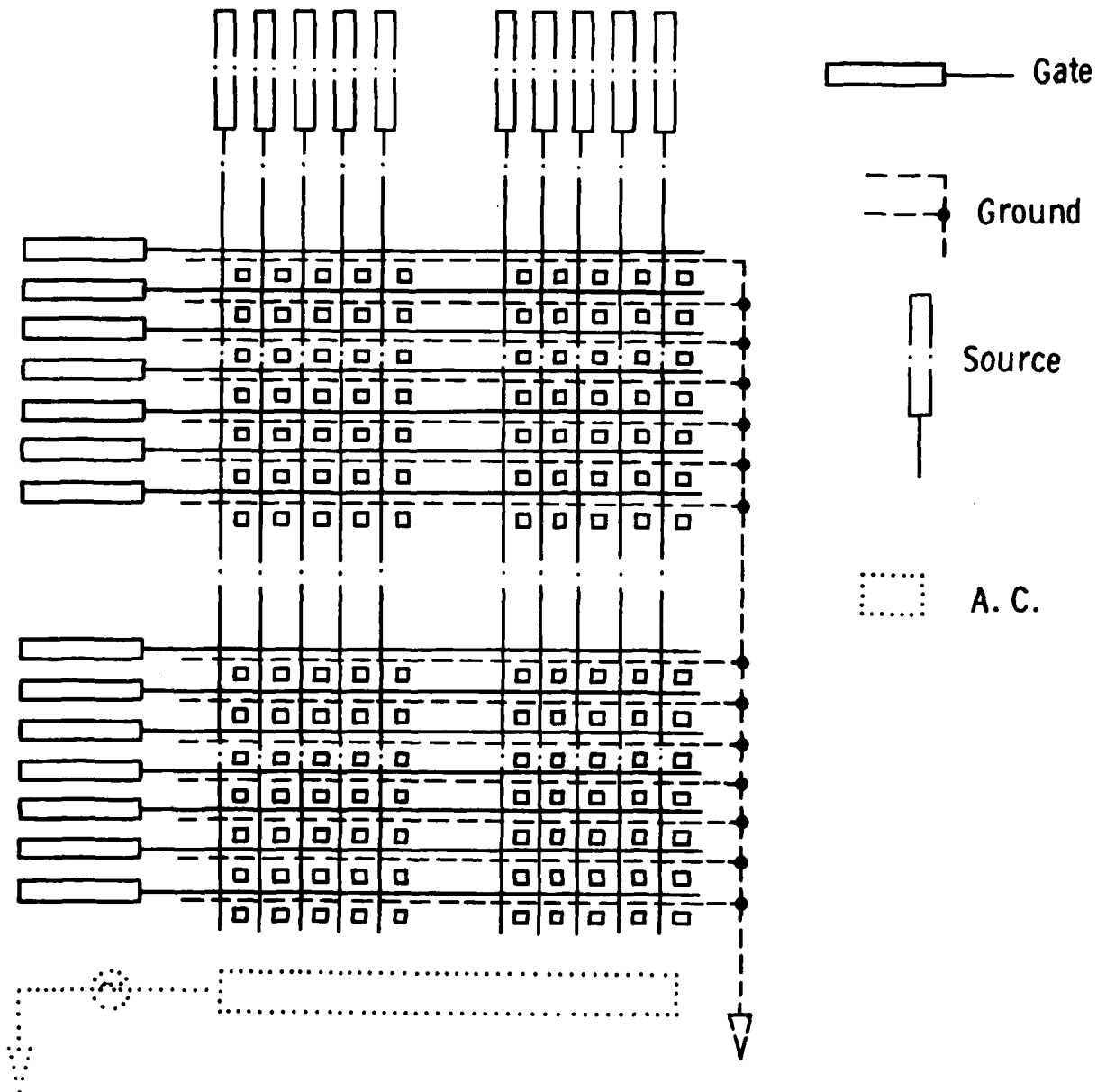


Figure 6.13 Precise location of short S15.4, G2.2.



character generator was designed to be consistent with an addressing code slightly different from that illustrated in Figure 6.12. In particular, the intra-character gate lines were identified, during design, as 0 through G. Consequently, while testing the alpha-numeric version we are presently making, the address S15.4, G2.2, illustrated in Figure 6.13, is actually displayed as E.6, 1.1. This snafu developed largely as a consequence of a communications gap between the circuit designer and the operator who had been using the scheme in Figure 6.12 since time immemorial. In any event, the operator mentally "adds one" to the components of the address code displayed by the tester before recording the address as in Figure 6.10. Also, for reasons of tester circuit simplification, we used the hexadecimal convention of A through F for addresses 9 through 14. Hence the cryptic instruction for conversion of source bus identification code at the foot of the form shown in Figure 6.10.

Our automatic short tester also has another problem in cases where the short defect complex is of a particular type. It may, in some circumstances, stop scanning at, and display, the addresses of so-called "ghost" shorts which may appear very real to the tester and, for that matter to a viewability exerciser, but really do not exist in a physical sense. A very simple example of how a ghost short can appear is shown in Figure 6.14 and is explained in the caption. In this example we have distinguished, as is our practice, between source-gate (Type V) defects and source-ground (Type VI) defects by using G for Gate and C for Common viz.

S3.3, G2.5 = Type V - Source Gate short

S1.2, C1.6 = Type IV - Source Ground short.

On the other hand, the tester will in certain cases fail to detect real shorts if open bus-bars exist. In actuality, we usually cycle back and forth between short and open testing if the defect pattern is tractable but complex.

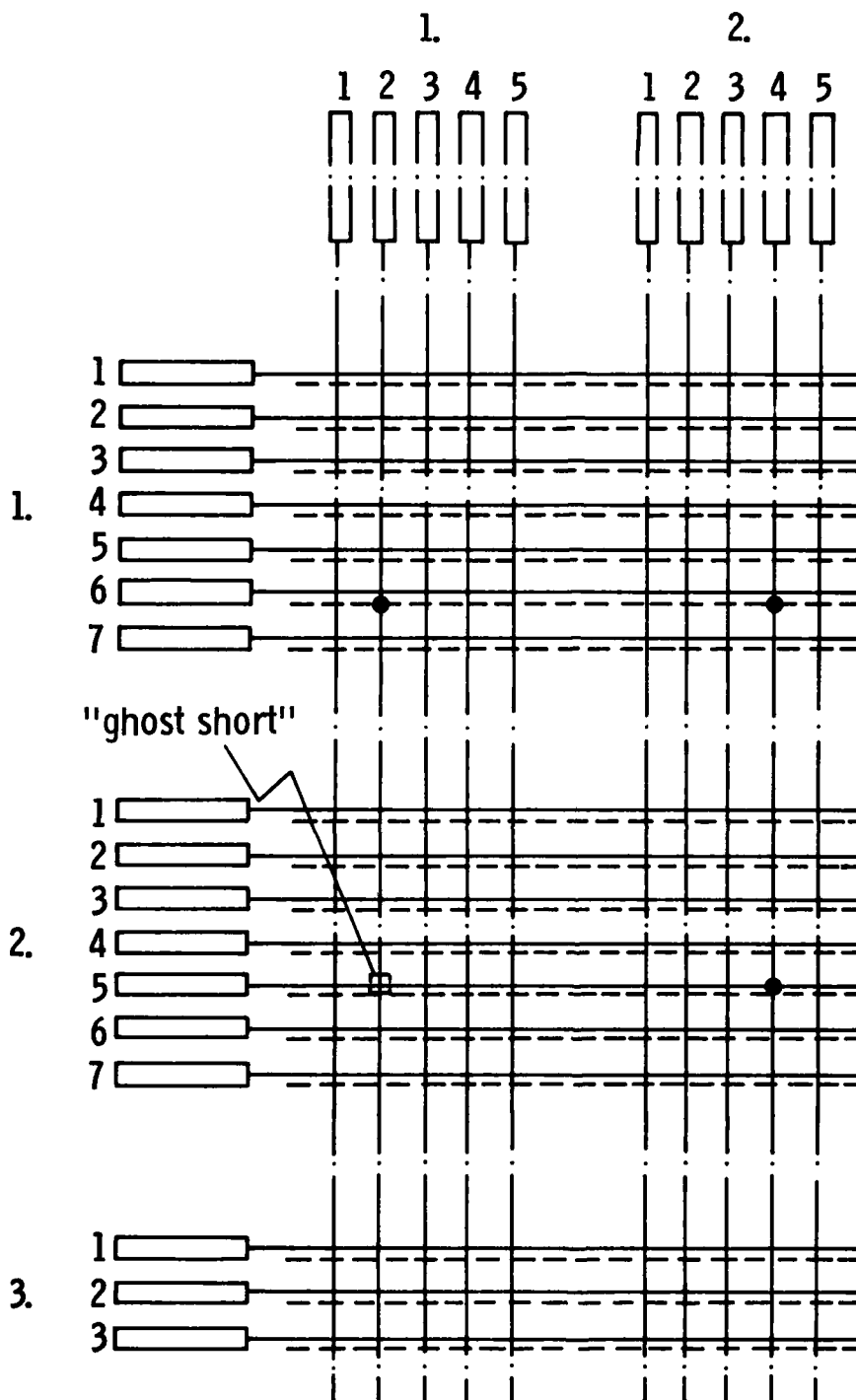


Figure 6.14 Example of how a "ghost" Type V (see Table 6.1) defect appears at S1.2, G2.5 as a consequence of an actual Type V defect S3.3, G2.5 and actual Type IV defects at S1.2, C1.6 and S3.3, C1.6.

A final note on short testing concerns what might be done further to improve productivity. Incorporation of the following features should be considered in any future activity pending routine production of entirely fault-free circuits. They include:

- print-out of short addresses
- analysis to separate ghost from real shorts
- automatic analysis of short generating cause (via analysis of the electrical load, for example)
- automatic microvision projection of defect area
- short-clearing robot

However, whether these chores are performed by our beleaguered operator, as at present, or by some more sophisticated means, no repairs are made at this stage. Instead, we accumulate the complete picture of all defects by testing the buses for electrical continuity and by looking at transistor characteristics.

Our test and evaluation procedure calls for measurements of bus-bar continuity prior to checking transistor characteristics for two reasons:

- (1) The transistor characteristics can be reliably predetermined by the fabrication recipe.
- (2) The open bus-bar test is significantly quicker and more critical.

The method for checking continuity was completely refashioned during the last quarter. Previously, we had no alternative but to use a manual method since the substantial effort applied to the old comprehensive testing scheme described in the previous section had not rendered it operational. The earlier manual method relied thus simply on using a manually held pair of probes attached to an ohmmeter. The new method we have developed uses the Electroglas prober disconnected from its computer interface. The source pads of the circuit under test

are all shorted by an easily removable conductive cement. Three probes of the Electroglas system are then lowered onto successive sets of the special bus-bar pads located at the ends of the source bus lines, as illustrated in Figure 6.15.

The Electroglas probe system provides for rapid sequential probe location at equally spaced intervals. The three probes located as in Figure 6.15 first test for continuity of bus-bars A and B, then A and C, through the curve tracer dashboard switch facility. Not by design, but in the interest of expedience, we thus check bus-bars in pairs. Both have to be continuous before either can be asserted continuous. The information in Table 5 illustrates the procedure in further detail for testing the bus-bars for the first few probe settings. Note that in positions 4, 11, 18 and so on, the joint conductivity is always open for the second switch setting. This is because every five bus-bars constituting a character column are separated by a distance equivalent to two bus-bar separations. Likewise, no conductivity is registered for probe settings 5, 6, and 7 or 12, 13, and 14 and so on for either switch position.

Executing this procedure requires two operators; one actuates the Electroglas probe stepping and the curve tracer dashboard switch. At each setting of the probes, he calls out 'yes' or 'no' as to whether continuity is observed for switch positions 1 and 2, respectively. The second operator notes down the responses on the chart shown in Figure 6.6B. A portion of the charts with some of the possible response sequences is shown in Figure 6.16 for the first character column and the first 4 probe settings. A checkmark corresponds to a 'yes' response and a cross to a 'no'. It is not immediately obvious through visual inspection of the responses to ascertain precisely which bus-bars are open or closed. Therefore, after the responses have been entered on the chart, they are analyzed using the five decoding squares allocated at the foot of each character column on the chart. In the third case in Figure 6.16, for example, the operator refers to the "buses tested" column (which is actually situated on the far left of the coding form

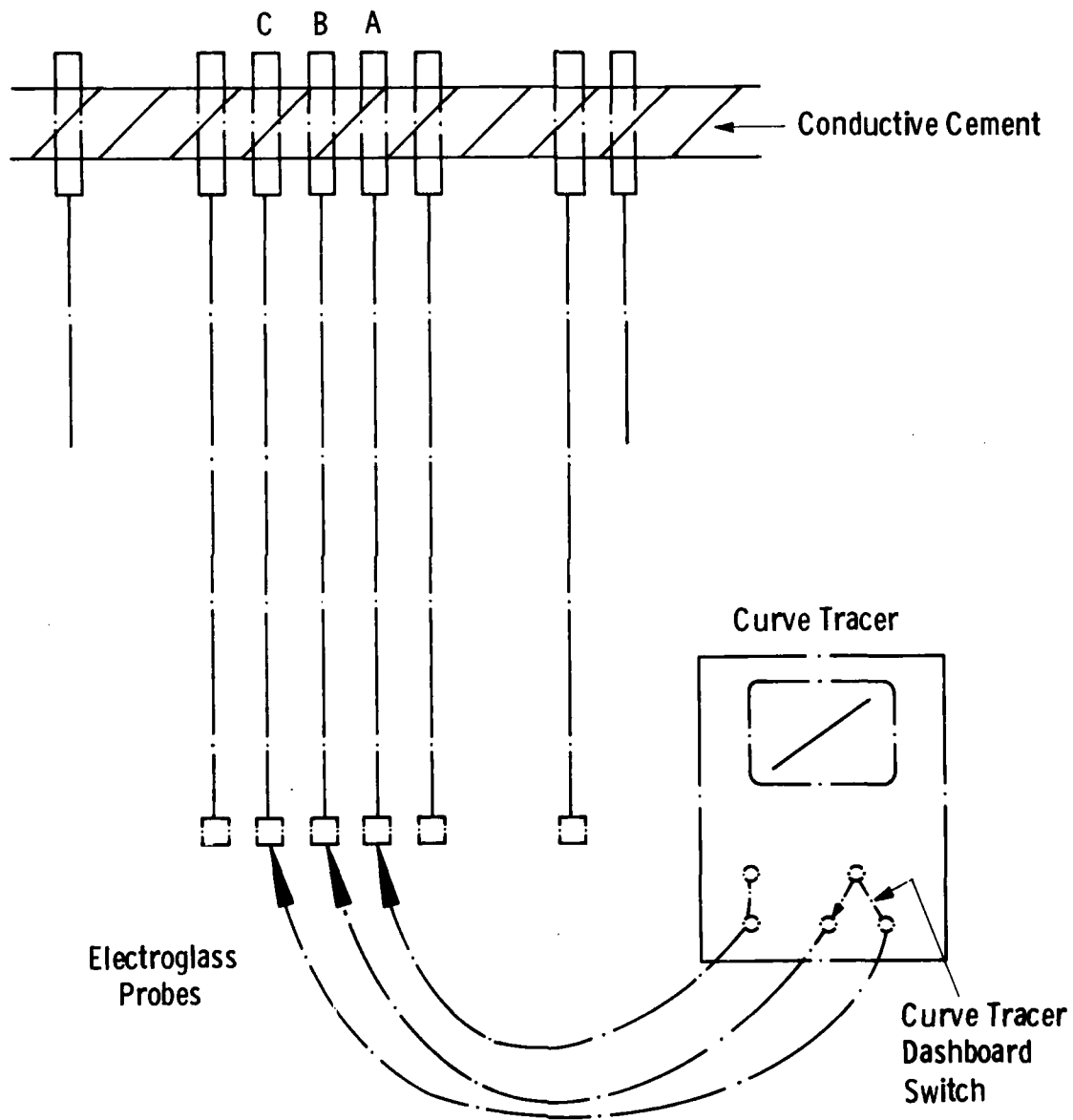
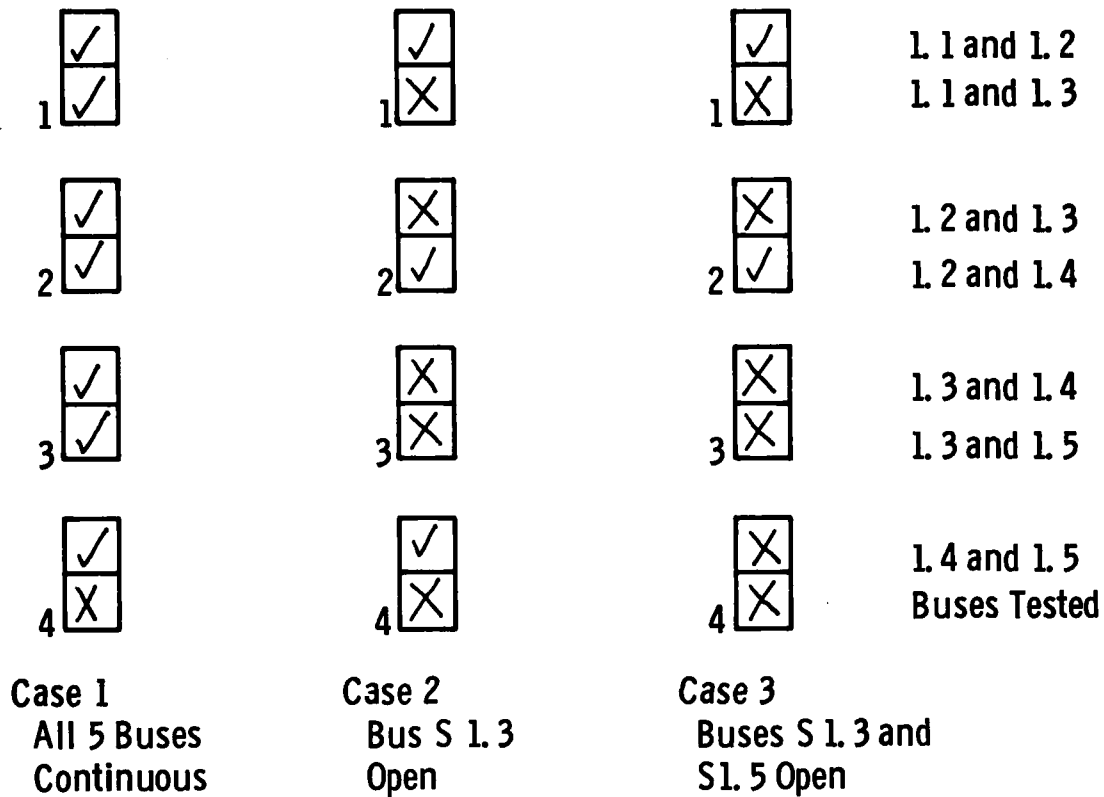


Figure 6.15 Method of testing for source bus continuity using the Electroglas prober.

TABLE 6.2 PROBE LOCATIONS AND SOURCE BUS BARS  
CHECKED FOR THE FIRST TWELVE PROBE SETTINGS

Probe Setting	Bus Probed By			Source Bus Continuities Checked	
	1	2	3	Switch Position 1 Probes 1 & 2	Switch Position 2 Probes 1 & 3
1	1.1	1.2	1.3	1.1 and 1.2	1.1 and 1.3
2	1.2	1.3	1.4	1.2 and 1.3	1.2 and 1.4
3	1.3	1.4	1.5	1.3 and 1.4	1.3 and 1.5
4	1.4	1.5	-	1.4 and 1.5	Always Open
5	1.5	-	-	Always Open	Always Open
6	-	-	2.1	Always Open	Always Open
7	-	2.1	2.2	Always Open	Always Open
8	2.1	2.2	2.3	2.1 and 2.2	2.1 and 2.3
9	2.2	2.3	2.4	2.2 and 2.3	2.2 and 2.4
10	2.3	2.4	2.5	2.3 and 2.4	2.3 and 2.5
11	2.4	2.5	-	2.4 and 2.5	Always Open
12	2.5	-	-	Always Open	Always Open



Key

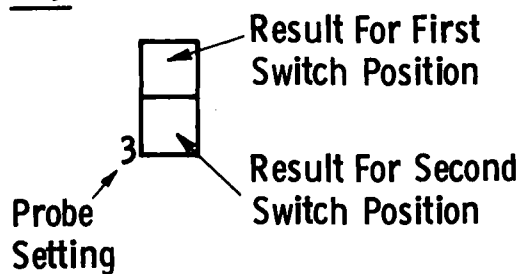


Figure 6.16 Some possible response sequences for first four probe settings in source bus continuity test.

itself in Figure 6.10) and checks those of the decoding squares corresponding to the second digit of the "buses tested" across from the positive responses. In case 3 of Figure 6.16, we have the first switch position of the first probe setting indicating buses 1 and 2 (for this character) are continuous and the second checkmark of the second probe setting indicating that bus 2 (which is known already) and bus 4 are continuous. The decoding squares, corresponding to these buses, and they alone, are therefore checked and the others blacked out by default, thus providing a ready reference as to the open or discontinuous bus lines as shown in Figure 6.17. The actual source bus continuity test chart for sample 9-151-4 is shown in Figure 6.18, indicating a single source bus open at S10.5. This is a somewhat lower count than typical recent experience.

The recording of horizontal gate and ground opens is best described by the few differences between it and the source opens. These are due to the 7 active/3 blank line vertical as opposed to the 5 active/2 blank line horizontal format. By necessity, the coding chart is different although the one shown in Figure 6.6C serves for both types of horizontal bus-bars. Conductive cementing of only the gate fingers are necessary since the ground lines are joined reliably at the main bus-bar. The actual marked up charts for our sample 9-151-4 are shown in Figures 6.19 and 6.20.

Overall, this bus-bar open detecting procedure is highly effective, particularly when compared to the only former alternative of working across each and every bus line with a manually-held pair of probes attached to an ohmmeter. As far as productivity is concerned, a "hit-and-miss" four-hour or longer process has been reduced to less than a twenty-minute one. However, what we have done can only be regarded as stop-gap compared to what could be done with a few further pattern modifications. For example, one could easily fabricate the source buses all shorted to one another opposite the ends from the fingers; such shorts could be quickly scratched or fused out after the test. In this way, the open test could be conducted from the fingers



Buses  
Tested

1 2

1 3

1



2 3

2 4

2



3 4

3 5

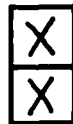
3



4 5

4 -

4



Responses For Tube  
Setting 5, 6, and 7  
(Always negative  
For Both Switch  
Positions) Omitted  
Here

1



2



3



4



5



"Decoding Squares"

Figure 6.17 Decoding Case 3 responses in Figure 5.12 indicating source bus-bars 1.3 and 1.5 are open.

**SOURCE BUS CONTINUITY TEST**

DATE 6-2-79

CHARACTER COLUMN NO. 151

SUBSTRATE NUMBER. 4

CHAR. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
12	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
13	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
23	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
24	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
34	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
35	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
45	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
46	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
56	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
57	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
67	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
68	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
78	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
79	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

CHECK 1 ☒ IF 2 ☒ 3 ☒ 4 ☒ 5 ☒  
 OK

Figure 6.18 Actual post-anneal source bus continuity test for circuit 9-151-4.

### HORIZONTAL BUS CONTINUITY TEST

POSITION	LR	LR	LR	LR	LR	LR
NO. 1	12.13	23.24	34.35	45.46	56.57	67.-

DATE: 6-2-79

DO NOT CHECK THESE PROBE PLACEMENTS

CHECK IF OK. ROW NO. 1 2 3 4 5 6 7

ROW NO.	1	2	3	4	5	6
1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
6	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
7	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
8	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

OPENS REPAIRED (ENTER ROW NO.'S)

TIME	DOT	DATE	CHAR	DOT	DATE

SUBSTRATE NO. 9 1 5 1 4

CHECK ONE ☒ GATE ☐ GROUND

COMMENTS

Figure 6.19 Gate bus open test results for sample 9-151-4.

**HORIZONTAL BUS CONTINUITY TEST**

IN POSITION L R L R L R L R L R

LOW NO. 12.13 23.24 34.35 45.46 56.57 67.-

L ROW NO.

DATE. 6-2-79

DO NOT CHECK THESE PROBE PLACEMENTS

CHECK IF OK. ROW NO. 1 2 3 4 5 6 7

1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	7	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	17	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	37	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	47	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
6	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	57	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
7	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	67	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
8	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	77	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

**OPENS REPAIRED (ENTER ROW NO.'S)**

ROW	DOT	DATE	CHAR	DOT	DATE

SUBSTRATE NO. 9 1 5 1 4

CHECK ONE ☐ GATE ☒ GROUND

COMMENTS

Figure 6.20 Ground bus open test results for sample 9-151-4.

themselves and, more importantly, in the same set-up we now use for short testing. The same thing holds for the gate open test. If, however, one were to go a step further and adopt the modified layout introduced in the Eleventh Quarterly Report and shown here again in Figure 6.21, then up to 90% of the bus-bar complex defects we observe could be rendered inconsequential electrically, in addition to being immediately detectable. The picture that emerges is one in which a raw circuit is installed in a fixture, scanned with intelligent electronics, and a comprehensive defect analysis performed with no mechanical probe movement, or the like.

Ordinarily, we make a go/no-go decision at this point as to whether to continue further testing. If the total open count exceeds about 20, the circuit is considered unusable. This usually only happens if something extraordinary has happened during fabrication; for example, an electric power failure, malfunction of the mechanical systems, EB gun shorting, vacuum failure, etc. Such "unusual" events have lately affected up to about 50% of the circuits processed during the last two months of the program. On the other hand, with "normal" operating vacuum system behavior, we test the transistors on just about all the circuits.

The special test transistors incorporated into the new layout are located to the lower right of all characters except the 16th column and the eighth row. A logic and a power transistor are fabricated at each of these  $15 \times 7 = 105$  locations. They are electrically isolated from each other, have oversize electrode pads, and are made exactly the same way as the circuit transistors, as shown in Figure 6.22. They can be quickly and conveniently accessed for electrical evaluation by the Electroglas prober, thereby providing an indication of the performance of the circuit transistors. This differs from former practice wherein the only transistors available for test were those incorporated into the circuit lines between the characters reserved for the graphics display format. However, in most respects we have retained the earlier

Dwg. '699'02

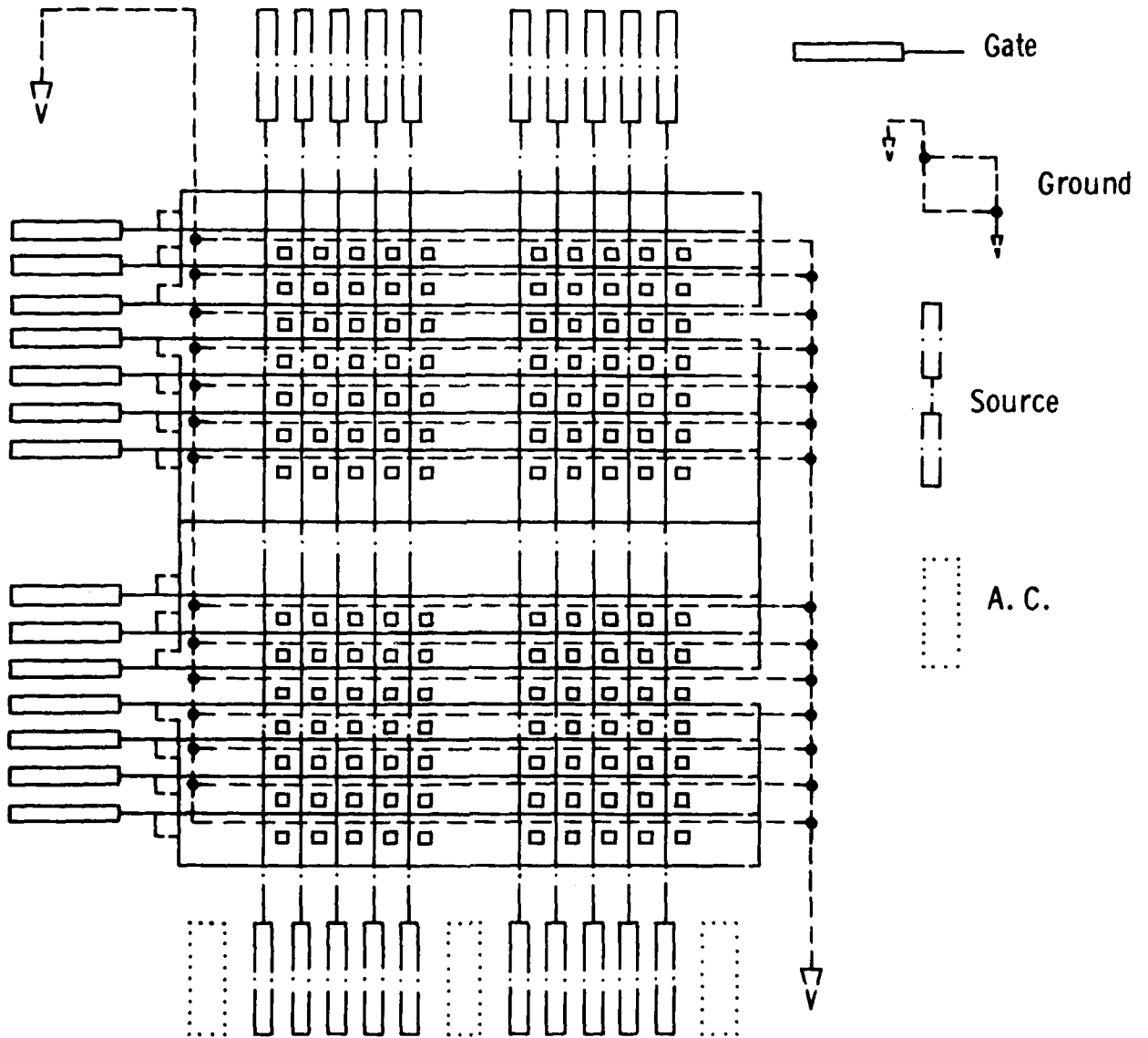


Figure 6.21 Basic features of the layout used in Program Phase III with no provision for fault tolerance.

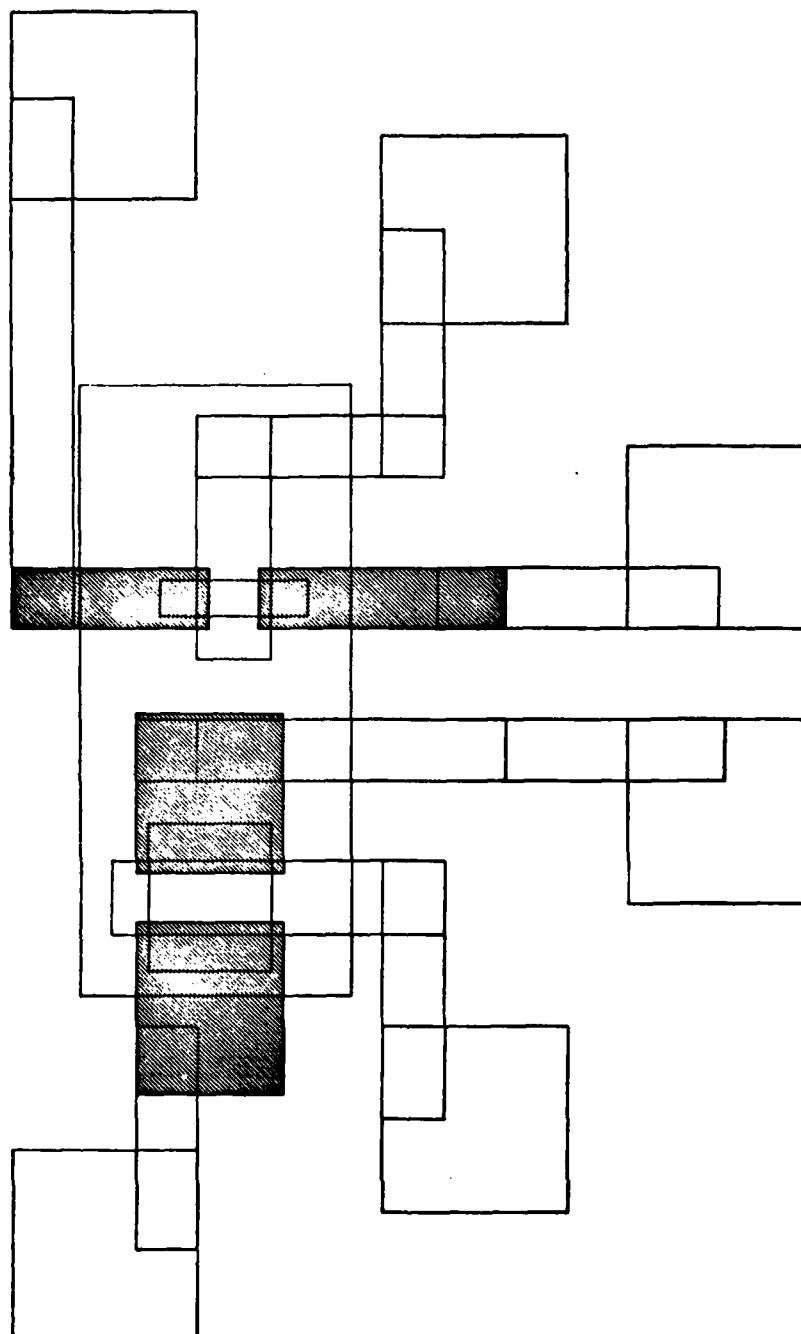


Figure 6.22 The special test transistor layout featured at 105 locations in the new pattern design.

test sequence. Now, as then, it is not clear how close this test procedure comes to simulating the circuit transistors in end-use. Certainly, one would expect different, hopefully even more favorable, requirements with excitation by the new exerciser circuitry discussed in Section 9. The test sequence for each power transistor is the following:

(1) Quiescent Source-Drain Leakage ( $I_0$ )

This is steady state source drain leakage with  
 $V_{gs} = 0$ ,  $V_{sd} = 15$  volts.

Objective:  $< 50$  nA

Maximum:  $1000$  nA

Recent

actual:  $\sim 10$  nA

(2) Dynamic Source-Drain Leakage ( $I_{10}$ )

After Test 1 above is completed, gate voltage  $V_{gs}$  is reduced to  $\sim -10$  volts for 10 seconds. Gate voltage is then returned to zero and the source drain current ("dynamic leakage") is remeasured.

Objective:  $< 35$   $\mu$ A

Maximum:  $100$   $\mu$ A

Recent

actual: }  $\sim 10$   $\mu$ A

(3) ON Current ( $I_{ON}$ )

Set  $V_{gs} = 20$  volts,  $V_{ds} = 15$  volts. Measure source-drain current.

Objective:  $> 500$   $\mu$ A

Minimum:  $50$   $\mu$ A

Recent

actual: }  $\sim 1$  mA



(4) ON Ratio "Stability" (S)

Measures ON current (at  $V_{gs} = 20$  volts,  $V_{ds} = 15$  volts) immediately after 10 second application of  $V_{gs} = -20$  volts at time zero and after time (zero + 10) seconds. Compute ratio of ON currents.

Objective: 1.0

Maximum: 1.5

Recent  
actual: } 9/5

(5) Source Drain Voltage Standoff ( $V_{BD}$ )

Apply source-drain voltage at  $V_{gs} = 0$  through 1.5 M $\Omega$  series resistance. Increase voltage until transistor fails (destructive test). Measure voltage.

Objective: > 300 volts

Minimum: 200 volts

Recent  
actual: } 90% in range 300-650 volts

The tests for the logic transistors are conducted in the same manner. Only the objectives and actual measurements differ, as shown in Table 6.3. The exclamation mark in Table 6.3 serves to direct attention at a major weakness in the testing procedure: transistor operating characteristics required to drive the display are really not presently known in the sense that the existing "limits" can be widely violated and the display continues to function even with the "obsolete" drive circuitry we still use. When the new drive electronics are applied, this whole testing procedure should obviously be widely reassessed and reformulated. Of course, the exceptionally high "ON" current experience of the logic transistors shown in Table 6.3 can only be beneficial. Actual test data for sample 9-151-4 is shown in Figure 6.23. As indicated in Figure 6.23, ordinarily only five transistors of each type are tested. Their character-coordinates are entered in the first two "location"

TABLE 6.3 OBJECTIVE, LIMITING AND RECENT  
ACTUAL TEST CHARACTERISTICS OF  
THE LOGIC TRANSISTORS

		<u>Objective</u>	<u>Limit</u>	<u>Recent Actual</u>
Quiescent leakage	$I_o$	<10na	100na	5na
Dynamic leakage	$I_{10}$	<50na	500na	10 $\mu$ a (!)
On Current	$I_{on}$	>75 $\mu$	10 $\mu$ a	400 $\mu$ a
Stability	S	<9/5	12/5	9/5
Voltage Standoff	$V_{BD}$	>100V	50V	400-650V

columns. Only on those rare occasions when the characteristics were more widely scattered than shown here did we inspect a larger sample.

As in the case of short and open testing discussed previously, there is much need for procedural revision here. Whereas the transistors in almost all cases perform as intended, measuring their test characteristics is labor-intensive and slow, and hence costly, even after enlisting the services of the quasi-automatic locating mechanism of the Electroglas prober. Since, with the new pattern, all of the constraints

# DMD TRANSISTOR TEST

9 151 4  
CIRCUIT NUMBER

6-2-75  
DATE

## POWER DEVICE

LOCATION		LEAKAGE		$I_{ON}$	S	$V_{BD}$
SOURCE	CATE	$I_o$	$I_{io}$			
3	2	5u	10 $\mu$	1mu	9/5	400
3	7	8u	12 $\mu$	1mu	9/5	500
8	4	5u	12 $\mu$	1mu	9/5	550
14	2	8u	10 $\mu$	1mu	9/5	450
14	7	5u	10 $\mu$	1mu	9/5	500

## LOGIC

LOCATION		LEAKAGE		$I_{ON}$	S	$V_{BD}$
SOURCE	CATE	$I_o$	$I_{io}$			
3	2	3u	5 $\mu$	400 $\mu$	6/4	550
3	7	5u	6 $\mu$	400 $\mu$	7/4	500
8	4	3u	4 $\mu$	400 $\mu$	6/4	550
14	2	3u	1 $\mu$	400 $\mu$	6/4	500
14	7	2u	1 $\mu$	400 $\mu$	5/4	500

Figure 6.23 Actual transistor test data for sample 9-151-4.

leading to the earlier failure of the totally automatic data-logging system have been lifted, its software should be re-programmed to receive relevant data, to record, and to analyze it. Although this task requires special skills, it is not difficult. However, we presently are not able to do it. The second way in which the transistor test procedure should be reformulated relates to the inadequacy of the scope and criticality of the various operating characteristics. It generally seems that our existing test "requirements" may be substantially tougher than what is needed to modulate the display phosphor dot matrix, certainly with the "new" drive electronics.

Going on to the next stage in the circuit evaluation procedure depends on whether the bus-bar open and short counts are "manageable". (As described in the Eleventh Quarterly Report, we have seldom had to reject a circuit on the basis of inadequate transistor performance ). In the case of sample 9-151-4, the defect count is quite acceptable (so far) for repair. However, before the actual repair procedure can begin, certain further information must be acquired as shown in Table 6.4. In this table we know, for example, that certain bus-bar lines are open but we do not know exactly where. Likewise, in the case of Type V defects, we know which sources are shorted to ground without knowing to what ground lines. Here again, the Electroglas prober is used to quickly and precisely locate each defect. Defect addresses so determined are then assembled on the Circuit Repair Schedule as shown in Figure 6.24. Needless to say, with appropriate reprogramming of the automatic test system software, this operation too could be very effectively completed totally automatically. The final step before initiating repair proper is to "map" the defects so as to assess their criticality, and the best way to undertake the repair procedure. In some cases, for example, certain defects which affect only an edge or corner character, or part of same, are not repaired or are otherwise surgically isolated for fear of creating other defects in the fault clearing procedure. The defect map for sample 9-151-4 is shown in Figure 6.25. The instructions in the margin of the chart are self-explanatory. One draws continuous lines

TABLE 6.4 STATE OF KNOWLEDGE OF BUS BAR  
DEFECTS AT THE CONCLUSION OF  
THE OPEN AND SHORT TESTS

<u>Defect Type</u>	<u>Description</u>	<u>Detected?</u>	<u>Defect Precise Location Known?</u>
I	Source Opens	Yes	No
II	Gate Opens	Yes	No
III	Ground Opens	Yes	No
IV	Source-Gate Shorts	Yes	Yes
V	Source-Ground Shorts	Yes	No

CIRCUIT

9

154

4

6-7-79

DATE

REPAIR SCHEDULE

BEFORE EL

AFTER EL

SOURCESGATESGROUNDS

S	G/C	✓
9.5	4.2	✓

O  
P  
E  
N  
S

G	S	✓
4.2	9.5	✓
6.2	7.5	✓

O  
P  
E  
N  
S

C	S	✓
4.2	9.5	✓

repairs completed 6-8

BUS BAR SURGERYSOURCE-GATESOURCE-END


NEW OPENS

No appearance  
after 15 hr up  
6-10

S	G	✓
15.4	2.2	✓
14.1	3.7	✓
5.4	2.1	✓
5.5	2.1	✓
8.4	7.2	✓
5.4	7.2	✓

S  
H  
O  
R  
T  
S

S	C	✓
3.2	5.5	✓

Figure 6.24 The defect repair schedule for sample 9-151-4.

# REPAIR ANALYSIS CHART VI 5-11

MARK SOURCE DEFECTS USING RED

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
11	1																
	2																
	3																
	4																
10	5																
	6																
	7																
	8																
35	9																
	10																
	11																
	12																

GATES  
 USE  
 GREEN

3 GROUND  
 (COMMON)  
 4 USE  
 BLACK

5 INDICATE  
 CUTS  
 WITH  
 BROKEN  
 LINES  
 OF  
 7 PROPER  
 COLOR

1 INDICATE  
 OPENS  
 INDICATE  
 SHORTS

2 ARE  
 TA RE  
 REPAIRED  
 WITH  
 BLUE + (CIRCLE WHEN FIXED)

3 SUBSTRATE  
 9-151-4  
 6-06-79  
 DATE

Figure 6.25 The defect map for sample 9-151-4 prior to any repair.

from bus-bar opens across those pixels affected by opens, and broken lines across those affected by shorts.

The map shown in Figure 6.25 has an important lesson to teach. As far as sample 9-151-4 itself is concerned, we see open bus-bars in all three directions emanating from the pixel at S9.5, G4.2. A single defect, namely a "cracked insulator", at this location has resulted in the "de-readability"(!) of no fewer than 20 characters. If, however, we had the opportunity to implement the bus-bar scheme shown previously in Figure 6.21, this defect would in no way affect readability. In fact, simply routing the open gates at 4.2, 9.5 and 6.2, 7.5 along the floating "spare" gate buses in Figure 6.21 and judiciously cutting the shorted bus lines would quickly provide a defect-free bus-bar pattern. As it is, we now have to use the kind of brute force procedure detailed in the next section. In spite of this, however, sample 9-151-4 was considered a relatively "easy fix". One final note concerning the defect map in Figure 6.25 should be kept in mind when viewing less than perfectly readable displays. Here we have a situation in which a total of only 8 bus-bar defects at a total of 8960 intersections, that is  $\sim 0.1\%$ , result in the de-readability(!) of 93 of 128 characters. In other words, a 0.1% defect rate results in a 73% drop in viewability! The real tragedy is that whereas our new mask design made a major contribution to testability, time circumstances, and foresight failed to allow consideration of a comprehensive fault tolerant design. In retrospect, this also might have been incorporated and would have had orders of magnitude impact on the presently limiting display manufacturability within the scope of the present program, namely, bus-bar complex yield.

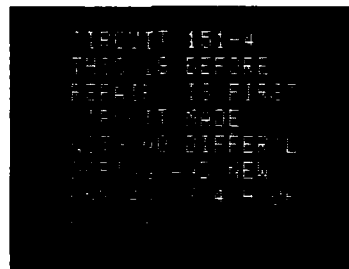
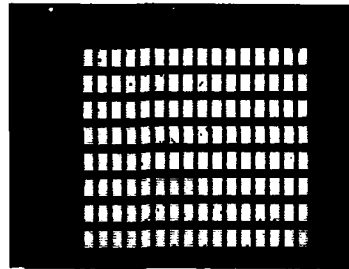
After repair and phosphor application, including top electrode and Krylon protective layer described in Section 7.6, the sample is again tested for shorts as it was tested initially. In this case, sample 9-151-4 had no new shorts but two of the previously cleared ones reappeared. Their effect is shown in Figure 6.26 which also illustrates post-phosphor display classification. Photographs in the all-dots-ON and all-dots-OFF mode are made, together with one of a printed message. In Figure 6.26 note the



# VIEWABILITY TEST SHEET

Substrate 9151-4

Date 6-11-79



Bias	5+	5-	6+	6-	EL
Volts	5	2	14	17	100

Figure 6.26 Completed viewability test sheet for circuit 9-151-4.

entry of drive bias conditions. For the sake of completeness, the final form in repair docket is illustrated with the coding of the display message in Figure 6.27.

Source	
	C I R C U I T I S I - 4
	T H I S I S B E F O R E
	R E P A I R : <del>I S</del> <del>R</del> <del>P</del> <del>T</del> R S T
GATES	C I R C U I T M A D E
	W I T H N O D I F F E R ' L
	D O P I N G A N D N E W
	O N E A N D 3 / 4 H O U R
	P R O C E S S .
EL	

Figure 6.27 The message coding to demonstrate the viewability of the phosphor dot matrix driven by circuit 9-151-4.

So far we have dealt exclusively and rather exhaustively with evaluation. We now discuss repair only briefly. There are several reasons for this:

Productivity: At the outset of the last quarter, we rapidly determined that 90% of the effort consumed in evaluation and repair was in evaluation, i.e., determining the scope and precise nature of defects in raw circuits. Only 10% was attributable to the actual act of repair.

Repair Technique: Although our practice in this respect remained somewhat primitive, it was more or less effective.

New Mask Design and Process Revision: Our intentions have been fulfilled in designing a layout with which relatively fault-free circuits can be made. Ultimately, we would expect this design to routinely provide entirely fault-free circuit bus-bar complexes. Whereas this has relieved the repair burden, and could be expected to continue to do so in the future, it is difficult to imagine how testing and evaluation per se could be eliminated. In other words, one could reasonably anticipate higher yields, but one would have to continue in-process test and evaluation to control and/or develop his process.

The repair procedure we use has three phases:

- (1) Clear bus-bar shorts.
- (2) Fix bus-bar opens.
- (3) Scratch out "permanently ON" dots.

The order in which the first two are undertaken depends on the relative frequency of the defects of the two broad classes. Only after phosphor application and post-phosphor bus-bar repair is the third phase undertaken. This is more for cosmetic purposes than to render non-functional pixels operational.

Our present short-clearing procedure is mechanically similar but electrically different from earlier practice. If the short is due to a dust speck, for example, this is readily cleared by discharging as low a capacitor at as low a voltage as possible through it using the circuit and set-up shown in Figure 6.28. If the short is more severe, for example, if it is caused by partial insulator pad absence resulting from a blocked mask aperture, capacitor discharge will sometimes burn out and open up one or both bus-bars in the immediate vicinity of the intersection which is shorted. In such cases, one judiciously elects to sever the shorted bus-bar and apply sequentially layers of non-conducting and conducting epoxy to render the severed bus-bar again continuous.

Almost all the open bus-bar defects we have observed with the new masks occur at crossovers. Figure 6.24 earlier showed an excellent example of this wherein no fewer than three open bus-bars originated at the same single defective insulator pad. These are repaired with the same technique used for re-uniting bus-bars cut deliberately to isolate the more severe shorts as described above. On those rare occasions when bus-bar opens are caused by mask aperture occlusions in relatively "open" pattern areas, local application of conducting epoxy alone is sufficient to correct the situation. Finally, when source bus-bar opens are cured by insulator underspray, continuity can be simply formed with the shortclearer.

Dwg. 7699A47

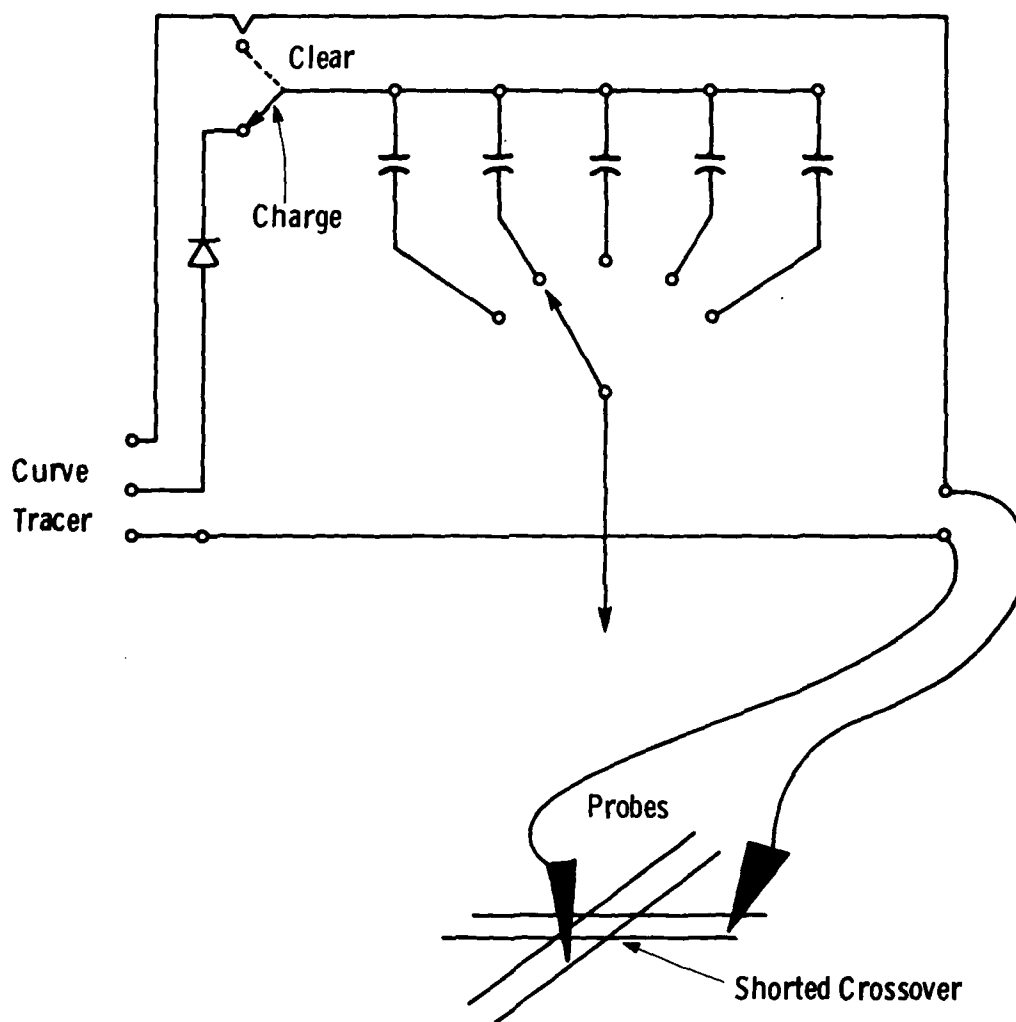


Figure 6.28 Procedure used to clear very local shorts at bus-bar crossovers.

Whereas we seemingly have never had time to implement the third phase of repair, i.e., scratching out permanently on pixels, our procedure calls for severing the connection between the power transistor and the corresponding EL pad. We typically observe 25 or so such defects and it therefore requires not much more than a few minutes.

Finally, we would, of course, prefer not to have to make any repairs at all. As far as the all important bus-bar complex itself is concerned, we have observed no opens in several of the more recently fabricated circuits. We have made only one or two entirely short free. We have never made a circuit entirely free from both opens or shorts. Statistically, however, only a modest projection from our recent progress would suggest the likelihood of this happening for the first time in the near future were the program to continue. Needless to say, such an achievement would be a technical oddity for a while. It is not conceivable with the present layout that a display with every last, properly functioning pixel could be made.

## 7. PHOSPHOR LAYER DEVELOPMENT

### 7.1 Theory of Electroluminescence

The wide bandgap II-VI compounds are very efficient phosphors even as pure materials. Many different impurities can be incorporated in them resulting in a wide variety of colors. Zinc sulfide has been found to be particularly efficient — a fact which as Fischer<sup>(21)</sup> points out is due to the existence of many stacking faults in the crystallites. These faults arise as a result of the closeness of energy of the hexagonal and cubic phases of ZnS and because the phase transition occurs below the firing temperature of the phosphor. Precipitation of impurities is enhanced along the stacking faults resulting in the development of conducting filaments. In the case of green emitting ZnS:Cu,Cd, the powders are doped at levels higher than the solubility limit of copper and excess copper filaments have been observed to decorate the stacking faults.

Used as an electroluminescent material, ZnS powder is embedded in a high dielectric constant organic material. The electric field is applied by electrodes added to both sides to form a capacitor. When an ac field is applied to the cell, the light, which appears to be emitted uniformly from the powder particles, is seen, under careful microscopic examination, to be coming from slender needle-like zones or "comets." The term "comet" (coined by Fischer) is appropriate because of the luminous bulb on one end of the needle. Furthermore, the comets appear to be distributed in pairs and they, in turn, are distributed in sets with 60° between the orientation of the different sets. Fischer places the surface brightness of the comets in the range  $10^5$ - $10^6$  foot lamberts with the average crystallite containing about 20 comets.

Under ac excitation, the light is seen to be emitted in pulses. Each member of a comet pair lights up on alternate half cycles with the light coming at any half cycle from the comet closer to the positive going electrode.

The observed dependence of the emission on the ac voltage depends upon whether one is looking at an individual comet or at the total amount of light coming from the particle or the phosphor layer

as a whole. Each comet has a brightness,  $B$ , that depends upon voltage according to

$$B = B_0 e^{-a/V}$$

where  $B_0$  is the saturation value of the brightness and  $a$  is a constant for each particle. Lehmann<sup>(20)</sup> showed that a superposition of a weighted average over the particles in a phosphor layer produces a characteristic which goes as:

$$B = \bar{B}_0 e^{-\left[\frac{\omega}{a/V}\right]^{1/2}}$$

in agreement with experiment over two orders of magnitude in  $V$  and as much as twelve orders of magnitude in  $B$ .

Both the intensity of the light and the spectral distribution depends upon the frequency of the ac excitation. In addition, the appearance of the comets is much broader at low frequencies  $\sim 1$  kHz, whereas at 10 kHz, they are narrower. The low frequency emission is green and the color shifts toward the blue at high frequency. When the spectral distribution of the light emission from a single comet is plotted as a function of time, one notices that the color starts out blue and moves toward the green at low frequency but remains blue at higher frequency. These observation can be accounted for on the assumption that the copper precipitate in the stacking fault is in the form of a copper enriched copper sulfide. The copper concentration decreases as one moves away from the needle. Holes are injected into the ZnS by the copper sulfide and the diffusion rate of holes is very much slower than the electron diffusion rate. The distance traveled by the holes during a half cycle will determine the volume of activated phosphor during that half cycle. On the reverse cycle, electrons are injected into the charged region and these recombine with the trapped holes. The electron-hole recombination energy is then transferred to the light emitting center. It is well known that isolated copper emission in the emission of ZnS:Cu is blue whereas the (Cu,Cd) center is green. As noted above, it is expected that the copper concentration is high near the needles so that one would



AD-A096 635

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FEB 80 M W CRESSWELL, P R MALMBERG, J MURPHY DAAB07-76-C-0027

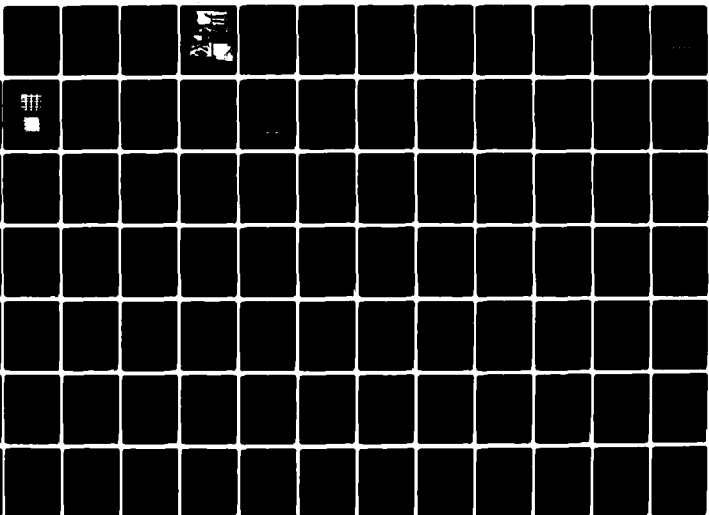
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80-9F9-DISPL-R1

DELET-TR-76-0027-F

NL

5 of 8  
SUB  
SCHEMATIC



expect there to be a high proportion of unpaired copper ions in that region, giving the blue light. As the holes have a chance to diffuse out in to the bulk, where the copper concentration is lower, not only does the needle appear fatter, but the emission looks green. This accounts for both the frequency dependence of color since at high frequency the hole diffusion is interrupted by the injection of electrons, and the early time behavior at lower frequency where progressive half cycle pulses get greener because some holes survive the electron onslaught to continue the diffusion into the low copper regions.

The integrated intensity of the emitted light shows a peak at high frequencies and the peak frequency increases with increasing voltage. If we continue the argument above and include concentration quenching of the copper emission, one can see that the higher frequencies will limit the hole diffusion to regions of ever-increasing copper concentration so that when the copper concentration quenching becomes dominant, the intensity will peak out. If the voltage is increased, field migration of the holes will pull them further into the lower copper region forcing the frequency peak out to higher values.

## 7.2 Phosphor Application: Prior State of the Art

The purpose of this section is to review the process wherein the circuits, whose fabrication has been described previously, were packaged into viewable displays throughout program Phase II. During this time, the severe inadequacy of the process with reference to the high temperature (72°C) maintenance requirements of the program was discovered. An ambitious process development program initiated during Phase II was carried over into Phase III and demonstrated about two orders of magnitude improvement in high temperature maintenance. The present section discusses prior state-of-the-art to serve as a background for subsequent discussion of this phosphor application process development. However, before beginning, two points should be made. First, the description "packaging" was used originally to describe comprehensive coverage of all activity wherein circuits were assembled into encapsulated displays. This terminology is featured in the present section. However, due to the nature of the technology, we subsequently divided the activity into the sequential operations of "powder phosphor application" and "encapsulation". This separation is then featured in the remaining sections of the present chapter.

Secondly, the customer indicated much later in the program that, due to parallel advances in thin film electroluminescent phosphor technology, an obviously superior medium for military applications, the powder phosphor technology we had developed so far could be frozen in its existing, but much improved, state.

During the early part of the present program, the powder phosphor technology Westinghouse had developed did the following:

- (1) Provide a passivating inert coating over the active portions of the thin film circuit.
- (2) Insulate the thin film circuit, except the actual pad of the lit area of each cell and the edge contacts, from the high frequency ac phosphor drive voltage.

- (3) Coat the circuit with electroluminescent phosphor in a simple but reliable method.
- (4) Provide a top electrode that was continuous, transparent, and had a suitable external connection.
- (5) Provide hermetic packaging of the phosphor and environmental stability by a final seal process.

After the thin-film circuit fabrication, the process consisted of four main steps:

- (1) the thin film circuit insulation
- (2) the phosphor deposition and related areas
- (3) top electroding
- (4) the final seal

These steps are described in the following paragraphs. Each of these is now discussed sequentially.

During thin film circuit insulation the photoresist laminator is first set up as shown in Figure 7.1, with the temperature set to 210°F. The thin film circuit is cleaned with ionizing air and a brush, and is laminated with laminar photoresist material between the pressure rollers. Extraneous material is trimmed and the coated circuit examined for ripples, bubbles and other imperfections. If not passable, the photoresist material can be peeled and the circuit relaminated. This process has proved reliable and is capable of production rates far in excess of our needs. The major study variables here involved establishing fixed parameters for roller pressure timing. Our present optimal material is DuPont Riston 110F; other materials may also be used.

The photoexposure unit shown in Figure 7.2 is used wherein a photoplate is placed over the circuit, aligned to it, and clamped with a vacuum pull-down. The plate is exposed and developed in 1,1,1 trichlorethane. The spray developer shown in Figure 7.3 consists of



Figure 7.1 The photoresist laminator.

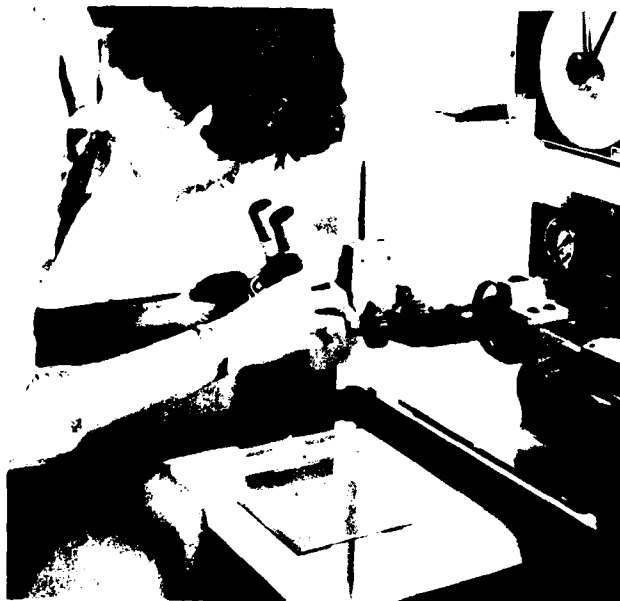


Figure 7.2 The exposure unit.

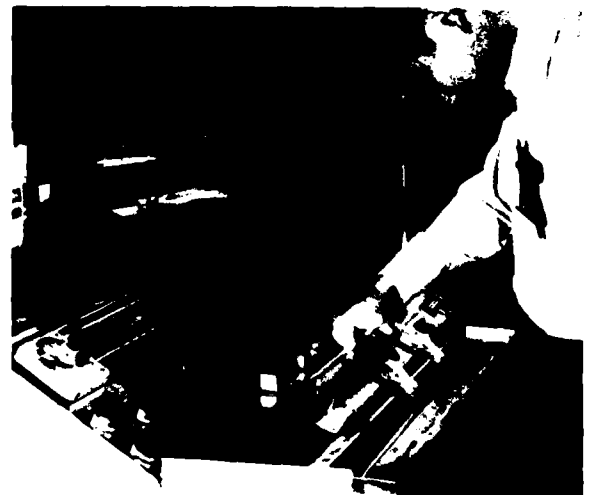


Figure 7.3 The developer.

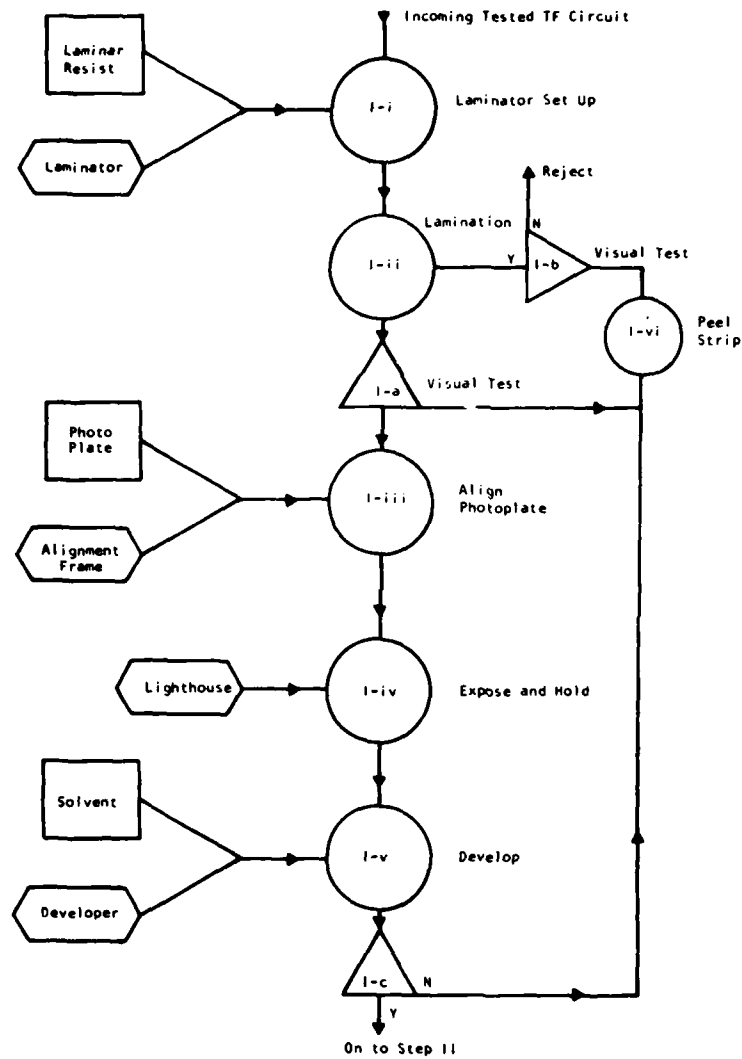
three stages: a spray for coarse developing, an isolated chamber for second clean-up developing, and a final deionized water rinse.

The "opened", photoresist coated, thin film circuit is now dried with clean air and examined visually. It is examined for four criteria: complete coverage, good clean opening of the apertures over the entire area, a graduated "edge" to the aperture, and the absence of blemish and other defects. A negative test result requires recycling of the circuit after a strip and peel operation. A visual check in this step is made for residual resist and for integrity of the thin film deposits. Any failure here results in a reject.

The short exposure time provides fast throughput at this stage, and therefore does not represent a throughput limiting step except that alignment can be occasionally difficult. Figure 7.4 summarizes the process sequence at this stage.

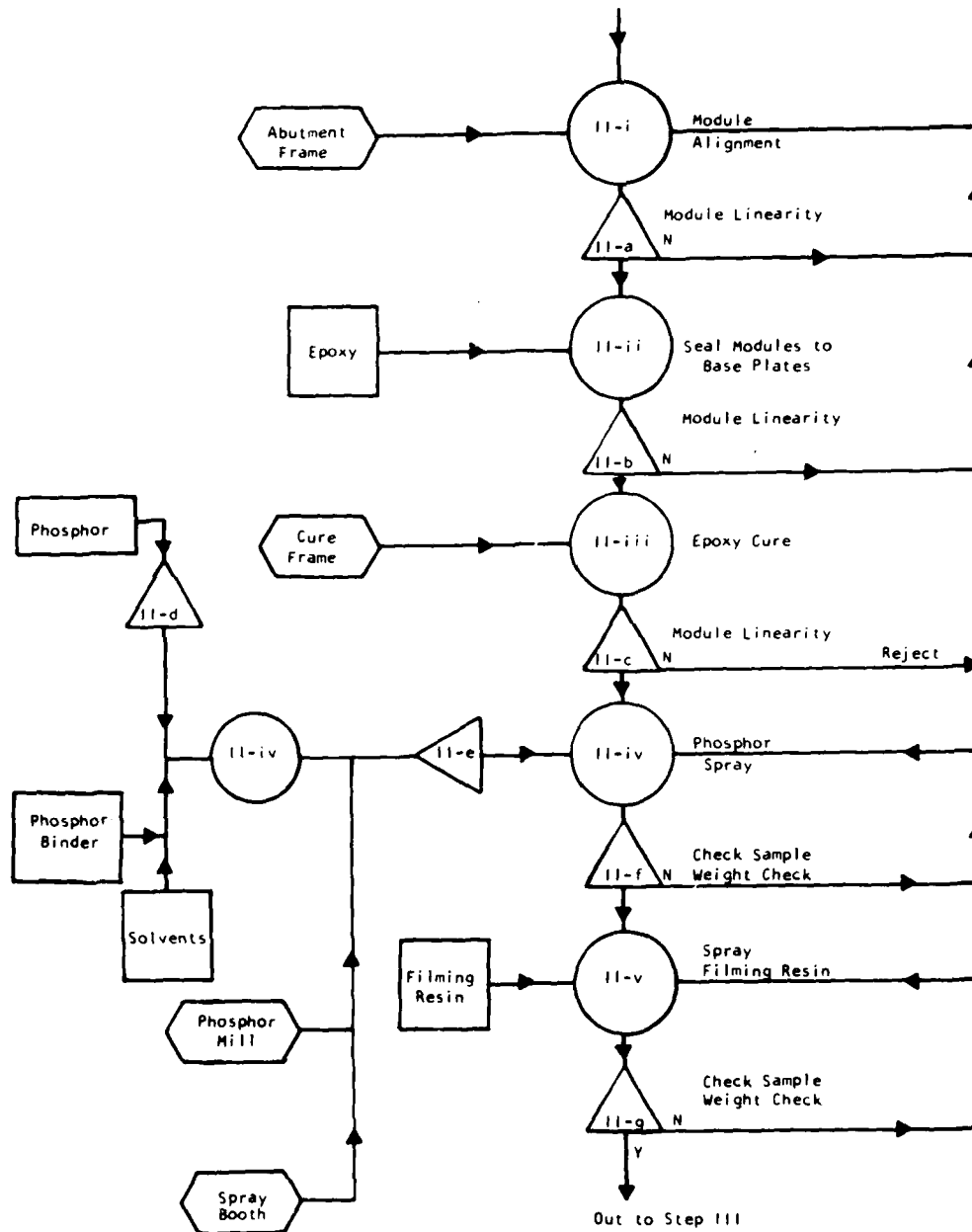
The phosphor screening process includes important material preparation and control procedures. These are therefore considered separately. The process specified in Figure 7.5 will be discussed first.

The accepted circuit plates are loaded onto a movable support that is moved back and forth with a geared drive. A phosphor/binder spray mix, described later, is prepared and a controlled spray procedure employed. A six-layer sequence was employed with a 135°C air bake between steps to ensure that each layer was dried. This method had been found to result in smooth, consistent, and uniform coatings. The substrate makes several automatic passes across the spray gun, which is fixed in location. All procedure parameters such as throw distances, angles, time of spray are fixed to ensure reproducibility. After completion of the phosphor spray, the surface is treated with methylmethacrylate, a resin, to ensure a smooth top electrode surface. This is accomplished with an aerosol spray of commercial "clear coat" for a controllable time, followed by a final 135°C bake.



Step 1 - Thin Film Circuit Insulation

Figure 7.4 Riston application flow chart.



Step II - Phosphor Screening and Module Assembly

Fig. 7.5 Phosphor screening flow chart.



The influence of this process on the phosphor maintenance is significant. The practice called for rigorous drying of all equipment and materials, and the multiple bake steps to ensure adequate dryness. The test procedure at this stage featured a check sample. This was the procedure used to maintain process standards. An acceptable screen weight from this sample was the go-ahead indicator for the next step. Failure at this step was generally not irretrievable, and respraying was possible.

The following describes the synthesis of the Westinghouse phosphor.

The ingredients of a typical batch are:

ZnS	95 mole-%
CdS	5 mole-%
Cu-acetate	1 mole-%
NH <sub>4</sub> Br	2 mole-%
sulfur	about 2-3 grams

which are thoroughly mixed.

The mix is then fired in capped quartz tubes surrounded by slowly flowing H<sub>2</sub>S at 800°C for 1 hour. This pre-fired phosphor is then powderized and the same amounts of NH<sub>4</sub>Br and sulfur specified above are added once again. A second firing is made in capped quartz tubes surrounded by stagnant N<sub>2</sub> at 600°C for 1/2 hour followed by rapid cooling to room temperature.

About 30 grams, but no more than this, of the phosphor is then baked in open boats in stagnant air at 600°C for 2 hours. The hot boats are then pulled out of the furnace and rapidly quenched to room temperature by exposing phosphor and boat to a stream of cold air. Finally, the phosphor is powderized, washed in hot cyanide solution, then in water, dried again, and sifted through 200 mesh.

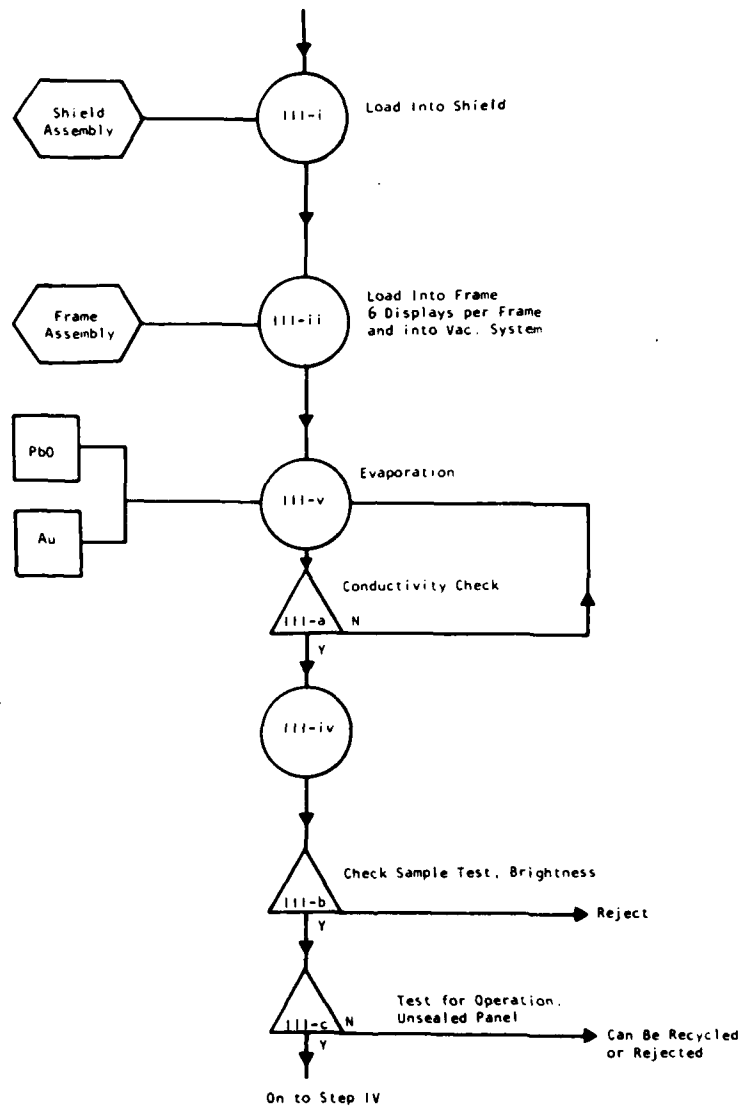
The phosphor is now ready for use. It is a free flowing powder of particles in the 5-10  $\mu$ m range. Its body color is olive-green. Its luminescence under excitation by ultraviolet is yellow-green.

This batch type process can be scaled up without loss of product quality, and since the total phosphor quantity required by the display is only about 1 gram per display and only "good" circuits reach the stage of being sprayed, the need to convert to a continuous type process is not major. In addition to the phosphor, a slurry for spraying is also required; this process has also been developed over several years for several earlier programs.

The procedure now involves two further steps. The first is formulation of a plastic binder solution and then the suspension of the powder phosphor in it. The plastic binder is made first by mixing cyanoethylated sucrose and cyanoethylated starch in dimethyl formamide (DMF) and acetonitrile. It is placed in a jar on a milling machine for three to four hours. After adsorbent molecular sieve is added, it is filtered and stored in a tight bottle.

The phosphor spray mixture is synthesized by mixing the Westinghouse hypermaintenance electroluminescent phosphor powder to the plastic solution, and forming a thin slurry ultrasonically for five minutes. This slurry is what is actually used to spray the Riston coated circuits. Care should be taken to shake the slurry immediately before each layer is applied. The high dielectric binders formed this way had previously exhibited considerable variability depending on the source of materials but in general the process was believed reliable for room temperature display excitation.

The final step in assembling an unencapsulated but viewable display is top electrode evaporation. Phosphored displays were electroded following the procedures shown in Figure 7.6. First a layer of lead oxide is evaporated on the phosphor binder layer with a display-source separation of about eighteen inches. This is followed by a transparent but conductive coating of evaporated gold. The evaporation is monitored by measuring the resistance of the deposited layer on a microscope slide or by using a quartz crystal thickness monitor. The evaporation is stopped when this resistance on the microscope slide is



Step III Top Electrode Deposition

Figure 7.6 Top electrode application process.

about 50 ohms/square. Prior to this operation, an edge connector shield is placed around the display periphery that keeps the busbar contacts clear but connects to the top electrode. The small check sample that follows the display through phosphoring is electroded simultaneously to the display. It is then used in the approval test at this step.

In order to increase the active or percent "lit" area of the display a so-called "second level" process was developed. This involves extension of the elemental circuit pad used for electroluminescent layer contact over the thin film circuit area. Electrical isolation is maintained using the laminar photoresist already used in the process and an appropriately dimensioned photoplate. Figure 7.7 illustrates the concept. A major problem has always been obtaining clean apertures in the contact area. Optimum methods based on Riston recommended procedures were used and largely solved this problem.

A second major difficulty was forming and maintaining reliable contact at the edge of the aperture. This problem resulted from the inability of the evaporated thin films to effectively penetrate around corners with continuity. If the resist is properly developed, that is if no residual material is left, then the edge of the aperture is overhung as shown in Figure 7.8. In depositing the electrode it can fail to bridge and no contact is made. If the aperture is underdeveloped, then of course the overall contact is poor. An attempt to solve this problem with rf sputtering was unsuccessful; although better edge contact could be achieved it was difficult to get uniform distribution of top electrode metallization, consisting aluminum, over this relatively large area.

To resolve the electrical continuity problem, evaporation at an acute angle was attempted. That is, the circuit covered with an isolation layer of Riston was placed at a sharp angle to the aluminum evaporation source. The substrate is then turned 180° to pick up the other side. This method proved difficult to adequately implement and gave very non-uniform thicknesses.

Dwg. 6358A19

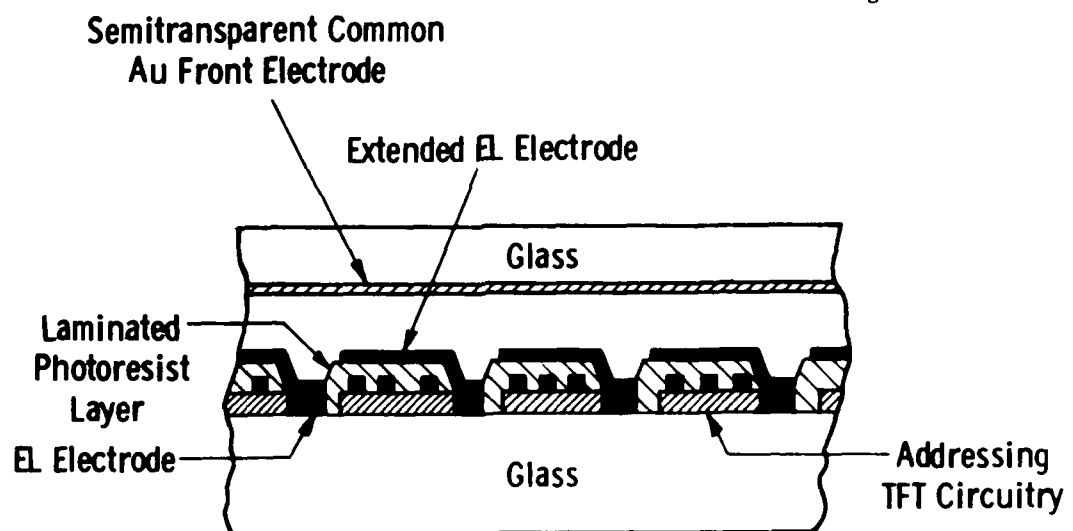


Figure 7.7 Second level concept for increased lit area.

The eventual optimal approach was the simplest. The phototool for isolation aperture exposure was fabricated in the X-Y mask fixture with less than a hard vacuum, for example,  $10^{-5}$  torr. This resulted in slightly fuzzy edges to the pattern. This was then contact printed onto high quality film and used as a master phototool. Although it was only partially successful initially, when combined with a careful optimization of exposure intensity, developing time, developing temperature and, after much experimentation regarding holding times on the resist, it resulted in near 100% first to second level contact. Figure 7.8 shows the resulting electroded apertures at various magnification levels and Figure 7.10 shows a close-up of some operational elements. Subjective examination of the resulting displays shows that the increased lit area, now  $\sim 75\%$  of total available, had a dramatic effect towards improving the overall legibility and area brightness of the device. After optimization the process worked well and reliably.

The final seal and packaging process originally used in this program was based on methods that had been used on similar electroluminescent phosphor radiographic image converters, produced for several years by the Westinghouse Industrial and Government Tube Division. This process is best performed on an individual basis since it is not readily automatable and is relatively labor intensive. Two factors, however, tend to alleviate this potentially restricting operation. First, only displays that pass the test sequences and the initial "non-sealed" operational test are sealed. Second, the process has proven to be reliable and routine in most instances, and has been described previously in Section 3.4.

Whereas the performance of displays assembled from circuits by the procedures described had demonstrated brightness maintenances of up to one thousand hours at room temperature, no testing at  $72^{\circ}\text{C}$  according to Item 4.5.9 in Performance Specification Sheet SCS501 had been performed until midway through Program Phase II. When such testing was attempted, average phosphor brightness typically decreased to 10% of a 10 foot lambert starting level within four hours. The

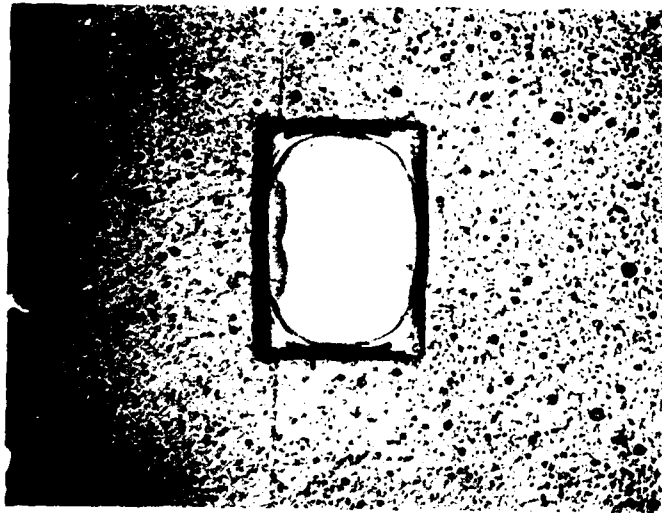


Figure 7.8 Overhung aperture in second level process.

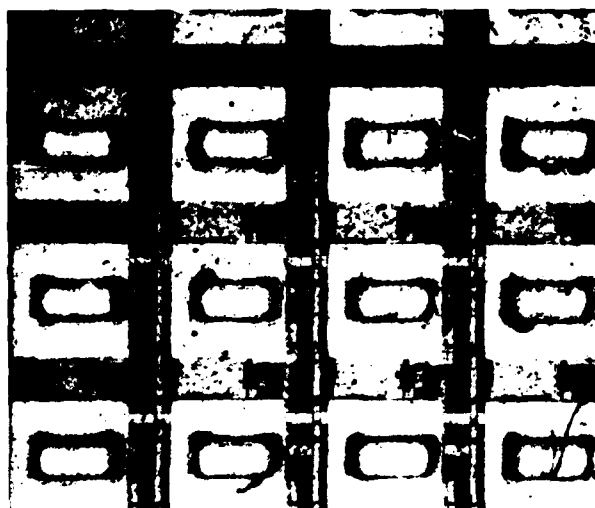


Figure 7.9 Actual second-level electrode pads.



Figure 7.10 Second level operation.



source of the problem was quickly traced to the phosphor-binder-encapsulant system. The thin film transistor circuit showed absolutely no sign of degradation. This discovery led to an intense "72°C phosphor development" subprogram of activity which terminated with impressively substantial but less than total successive prior to the end of the overall program.

Remaining sections in this chapter review the technical activity, describe a newly developed powder phosphor application technology so devised, and characterize its performance vis-a-vis 72°C maintenance.

### 7.3 The Powder Phosphor Layer Development Strategy

Confronted with the disappointing performance of displays encapsulated by the technique in the previous section, we realized from the start that intense and probably prolonged effort would have to be applied to phosphor layer development if anything approaching program requirements were to be met. Consequently we decided to continue using the existing method strictly as a circuit evaluation medium while parallel activity focussed on the phosphor layer as a subsystem. A critical issue was whether the phosphor powder itself under any circumstances was inherently able to provide the required maintenance, regardless of method of application and encapsulation. Experience prior to submission of the program proposal had indicated that indeed the phosphor itself was up to the task and so a preliminary tactic was simply to confirm this. A second separable element of the strategy was to determine the effect of the chemistry and physics of the binder and the method whereby the phosphor was embedded in it. It was decided to conduct related experiments in vacuum in order to separate out inherent deficiencies of the structure from its subsequent vulnerability to exposure from the environment. Having optimized the binder and the structure of the phosphor layer in vacuum, our strategy called for subsequent environmental 72°C testing with alternative encapsulants. The execution of this overall strategy was to be supplemented by design of special test vehicles to obviate the need for a copious supply of working circuits and the institution and maintenance of a computer-based information system to cope with the anticipated voluminous test data. In retrospect, this strategy proved remarkably successful and the execution of its various facets are described in the next section.

#### 7.4 Implementation of the Development Strategy

##### 7.4.1 The "Postage Stamp" and Test Chip Vehicles

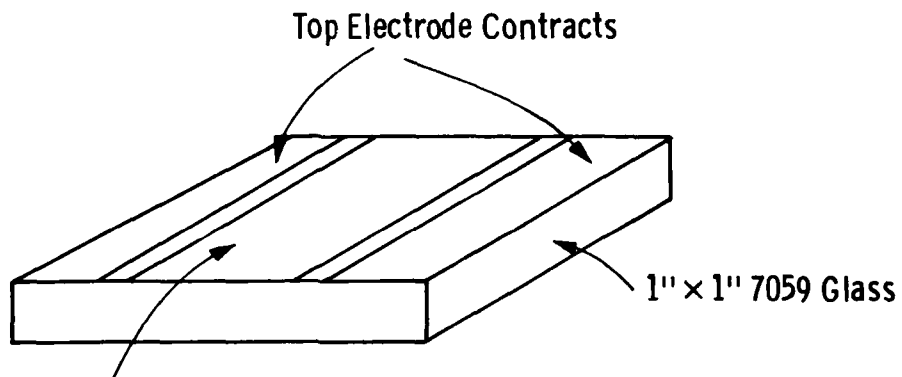
The postage stamp test vehicle is a one-inch piece of glass which is metallized on one side to simulate a parallel assembly of elemental circuit EL pads. Riston is applied exactly as in the DMD phosphor application process described in Section 7.2. Holes are opened in the Riston, the phosphor layers are applied, and a top electrode, consisting of layers of oxide and gold, is applied again exactly as in the case of the display process. With separate contact to the top and bottom electrodes, and optional application of encapsulation materials, such as epoxy and/or a cover plate and/or an edge seal, the resulting structure provides simulation of the display for life testing as far as the phosphor and encapsulation subprocesses are concerned. The typical composite structure without any encapsulation processing is shown in Figure 7.11.

A second test vehicle we have used is called a test chip. This is simply a small NESA-coated substrate onto which the phosphor layers are applied directly with no Riston. The NESA serves as a bottom electrode and an opaque aluminum film constitutes the top electrode.

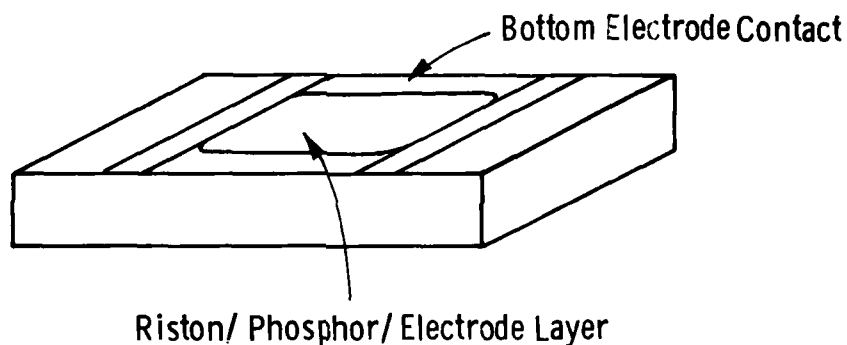
##### 7.4.2 Maintenance Figure-of-Merit

Since the phosphor layer development activity was to feature a raft of different postage stamp and test chip configurations, it was mandatory to have a consistent figure-of-merit with which would objectively be used to compare their performances. An important parameter one uses in a life test is, of course, the applied voltage (root mean square) and its frequency. The obvious approach is to select some voltage, ideally compatible with the capability of the power transistors in the thin film circuit, and observe the decay in brightness with time. With maintenance to spare, there is nothing wrong with this approach. For example, let's consider a first postage stamp which initially emits 60 ft-L at 100 V<sub>rms</sub> and after, say forty hours has decayed to 10 ft-L. The 10 ft-L maintenance is said to be forty hours, as shown by the unbroken line in Figure 7.12. However, a second

I Patterned  
Cr-Au  
Evaporation



II Application  
of Riston &  
Phosphor



III Top Electrode  
Deposit &  
Contact

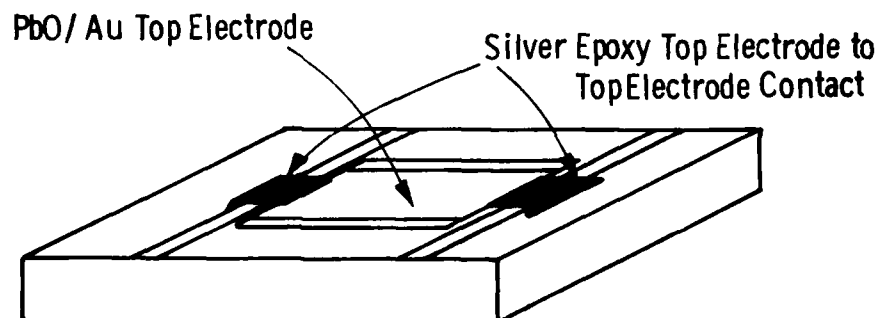


Fig. 7. 11 — "Postage Stamp" test vehicle fabrication and structure.

identical postage stamp was observed typically to behave as shown by the broken line in Figure 7.12 when excited first by 70  $V_{rms}$  for fifty hours and then by 90  $V_{rms}$  for fifty hours. The second sample, structurally identical to the first, under these conditions can claim one hundred hours maintenance at 20 ft-L instead of only forty hours at 10 ft-L. In the ultimate case, wherein the voltage is constantly upward adjusted, our sample might well exhibit 20 ft-L for up to, say, two hundred hours.

In the interest of providing meaningful comparisons of maintenances between differently configured samples, we adopted the constant brightness as opposed to the constant voltage life testing mode. This so-called "life testing by voltage ratcheting" had the additional advantage of providing substantially longer maintenances, ceteris paribus, simply because, on the average, the sample ran cooler and optical emission limiting chemical and physical reactions were thereby inhibited. The reader will recall our phosphors displayed maintenances of typically thousands of hours at room temperature. Only at elevated temperatures did sustained emission become increasingly jeopardized.

With the voltage ratcheting approach, lifetime is terminated when the voltage required to sustain some predetermined brightness exceeds some particular level; in this case, the latter is meaningfully the voltage capability of the power transistors in the thin film transistor circuit. Typical behavior of a postage stamp sample under constant brightness voltage ratcheting is shown in Figure 7.13. With reference to Figure 7.13, we always observe three characteristic time periods as shown.

1) The "burn-in" period: Drive voltage required to sustain constant brightness increases rapidly at first, eventually becoming linear with time. The burn-in period is considered part of the lamp fabrication procedure. For this reason, and because behavior during burn-in tended to be erratic at best, the threshold voltage,  $V_T$ , is defined from now on by linear extrapolation as shown in Figure 7.13.

Curve 720664-A

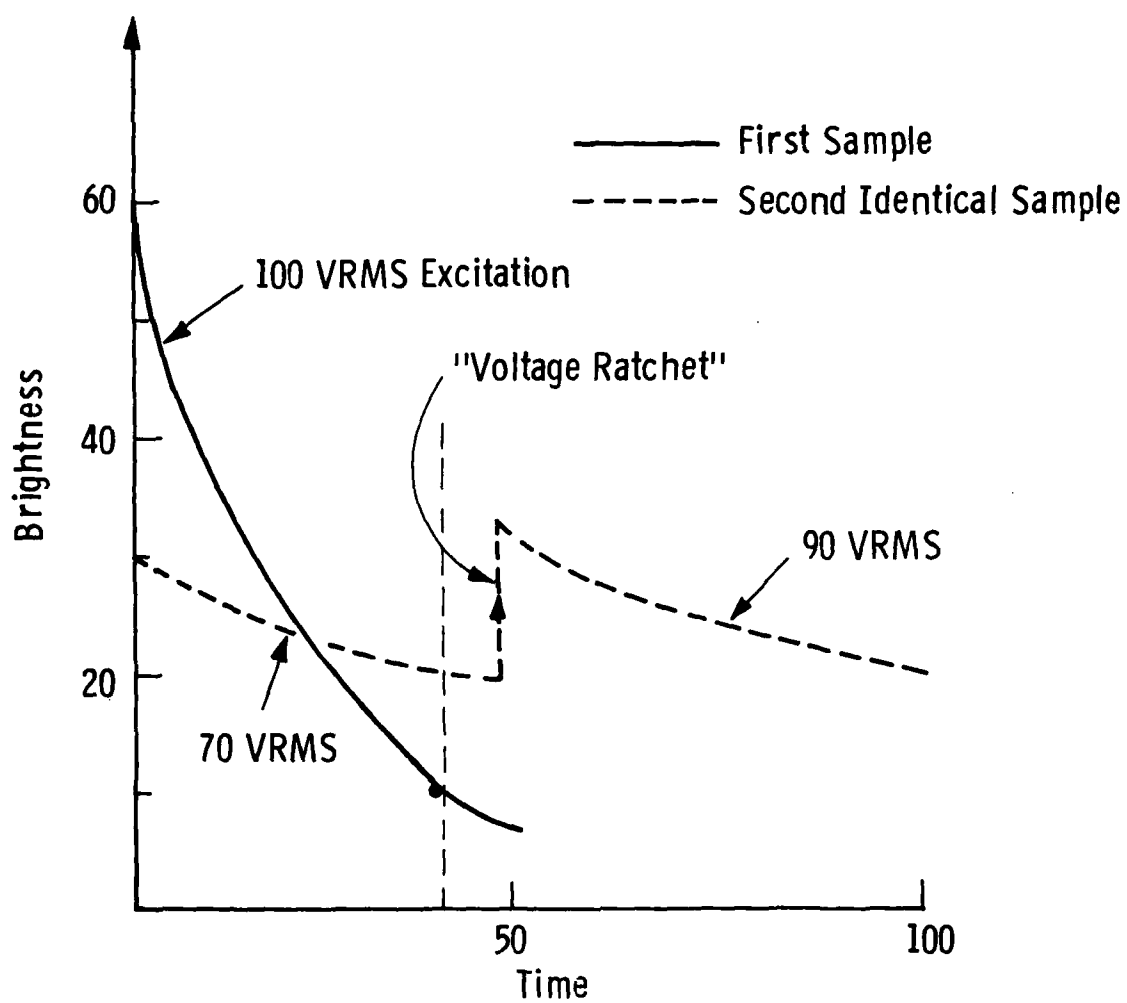


Figure 7.12 Typical behaviors of the Westinghouse phosphor under 100  $V_{rms}$  constant excitation and 50-72°C.

Curve 720666-A

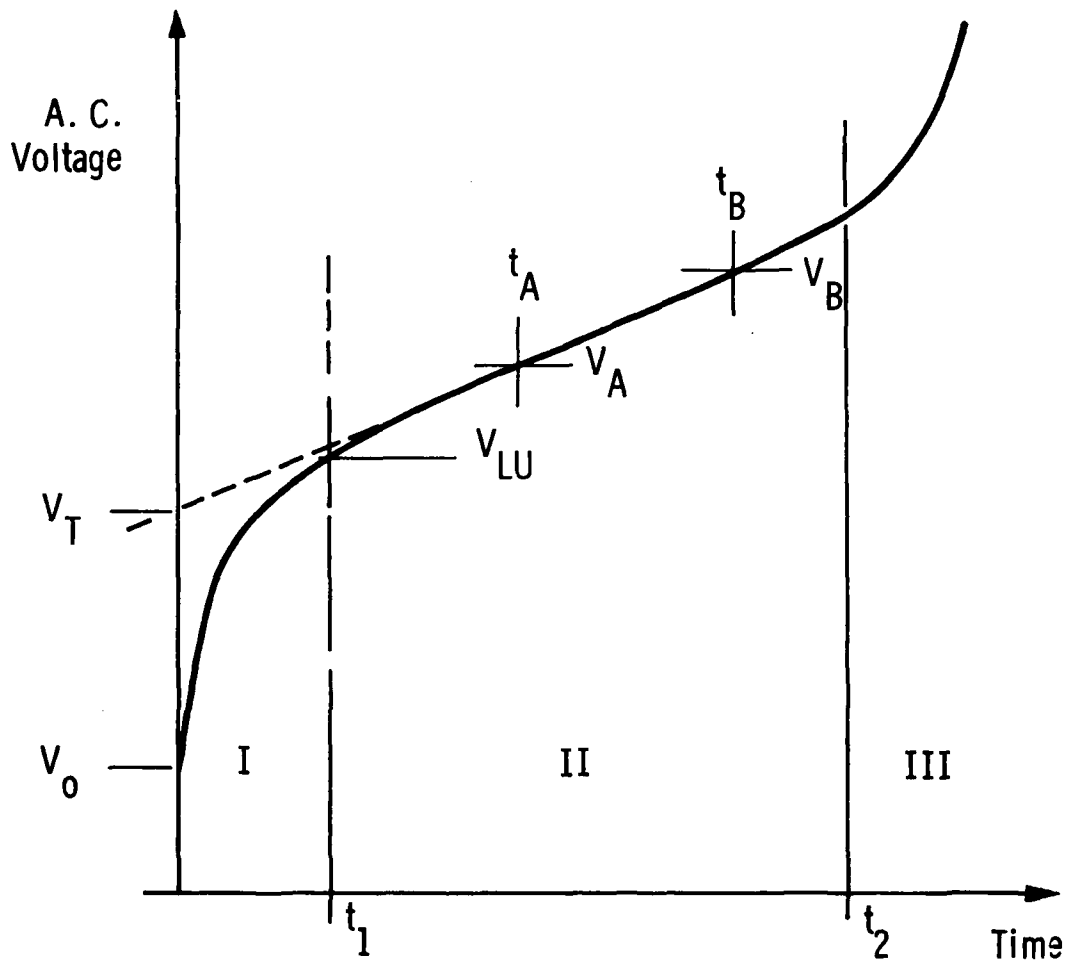


Figure 7.13 Typical curve of voltage versus time at constant brightness for a powder phosphor lamp.

otherwise, explicitly specified. The quantity,  $V_0$ , shown in Figure 7.13 will be referred to as the "initial voltage".

2) The "normal maintenance" period: Drive voltage required to maintain constant brightness increases remarkably linearly with time. The inverse slope of this line (in hours per volt) is the number used to characterize lamp performance. The higher this number, the better the "maintenance" the lamp is said to have.

3) The "burn-out" period: Due to physical and/or chemical deterioration of the lamp, brightness at constant voltage begins to degrade even more rapidly. Consequently voltage required to maintain brightness begins to increase super-linearly. Total failure of the lamp usually follows in the next 20-50 hours.

Within this context, the ideal lamp has low light-up voltage,  $V_{LU}$  in Figure 7.13. It then degrades at a low rate characterized by a very high hours per volt figure. It is meaningful therefore to speak of a lifetime only in conjunction with a particular maximum allowed voltage. Referring again to Figure 7.13, if the maximum allowed voltage is  $V_A$ , the lifetime is  $t_A$ , if  $V_B$  the lifetime is  $t_B$ , etc. For the present application, upper voltage limits  $V_A$  and  $V_B$  have a very real meaning. The power transistors of each elemental cell of the display circuit have can typically withstand only 150  $V_{rms}$  as shown earlier in Table 5. 16. Therefore our mission was one way or another to manipulate the maintenance curve so that the ordinate at 500 hours is less than this amount. Towards the end of program activity we could only do this with unencapsulated NESAs chips tested in vacuum. Our best encapsulated postage stamps, as we shall see, usually reached the 12 ft-L, 120  $V_{rms}$  points after about 300 hours. However, even at the termination of technical activity, this number was continuously increasing as we managed the fabrication process and changed the materials used.

#### 7.4.3 Computer-Based Information System for Measurement Data

At the beginning of the phosphor development effort we correctly anticipated acquisition of extensive test data from up to



one hundred samples making systematic data recording and analysis mandatory and for which a computer-based system was ideal. An excellent example of why systematized data logging was so important is implied by the scope of testing indicated in Figure 7.14 which illustrates only one part of the total testing setup. This section will briefly describe a custom engineered scheme which proved extremely simple to use and maintain, and which was designed for this purpose.

The fundamental task was to systematically record voltage levels to which a particular sample was ratcheted to maintain a prescribed brightness. Typically, but not necessarily, once a day the brightness of each test lamp was recorded ("old brightness"), and the excitation level ("new volts") was increased until emission reached the predetermined test level. These numbers were entered on the test sheet shown in Figure 7.15. The operator was also required to enter the date and time the voltage ratchet took place and to manually evaluate the "hours", that is, the duration into the test. Other data called for in the top half of the test sheet was always provided at the initiation of the test.

At his convenience, the operator later either opened a new computer file for each sample or updated an existing one. This operation was extremely easily implemented using component routines of the software package described in Appendix I. Another part of this software package was a program which identified the linear region II of the voltage versus time curve exemplified in Figure 7.13. The algorithm features least square fitting to selections of data points and systematically searching for a best fit selection to exclude the effects of burn-in and burn-out regions, I and III. The same program computed the maintenance characterizing the linear region of interest in terms of hours per volt and projected or interpolated lifetime at the brightness featured in the experiment. It presented also a graphical portrayal of the analysis whereon these numbers were printed as exemplified in Figure 7.16. (The operator was responsible for drawing in the fit to the linear region denoted by the line printer by plus signs shown!).

# PHOSPHOR MAINTENANCE TEST SHEET

PAGE    OF   

130	SAMPLE NO. 585-1	USE CTS COMMAND <u>CALL HEADING</u>	
140	SAMPLE TYPE <u>STAMP</u>	TO START NEW FILE & ENTER THIS DATA	
150	OVEN NO. 4		
160	BRIGHTNESS 3.6	260	BASE COAT WEIGHT .71
170	FIG. BOOK REF. —	270	TOP COAT 1 .28
180	DATE MADE 4-2-79	280	TOP COAT 2 .52
190	AMBIENT VAC	285	PHOSPHOR WEIGHT 4.32
200	TEMPERATURE 72 °C	286	SHEET RESISTANCE 120-2

210	SUPPLEMENT 584	USE CTS COMMAND CALL U TO ENTER <u>PURPOSE</u> , COMMENT AND/OR OTHER INFORMATION ABOUT THIS SAMPLE
220	SERIES WITH 6 KHZ	
230	LIFE TEST. SAME	
240	AS 586-1 :	
250	586-2	

USE CTS COMMAND CALL E						TO ENTER MEASUREMENT DATA					
LINE	MEASUREMENT		HOURS	OLD BRIGHT	NEW VOLTS	LINE	MEASUREMENT		HOURS	OLD BRIGHT	NEW VOLTS
	DATE	TIME					DATE	TIME			
300	4-02	16:00	00.0	3.6	64.4	420					
310	4-3	10:00	18.0	2.2	84.5	430					
320	4-4	10:00	42.0	2.3	100.6	440					
330	4-5	10:00	66.0	2.6	113.6	450					
340	4-6	16:00	96.0	2.4	128.9	460					
350	<hr/>					470					
360						480					
370						490					
380						500					
390						510					
400						520					

Figure 7.14 The phosphor maintenance test sheet into which voltage ratcheting test data was entered in the laboratory.

UPDATE 6-5-79

● SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

POSTAGE 589-8  
STAMP 2  
3.6

FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-25-79  
VAC  
25C

SAME AS 589-7

BASE COAT WT .59  
TOP COAT 1 .19  
TOP COAT 2 .18  
PHOSPHOR WEIGHT 4.17  
SHEET RESISTANCE 160

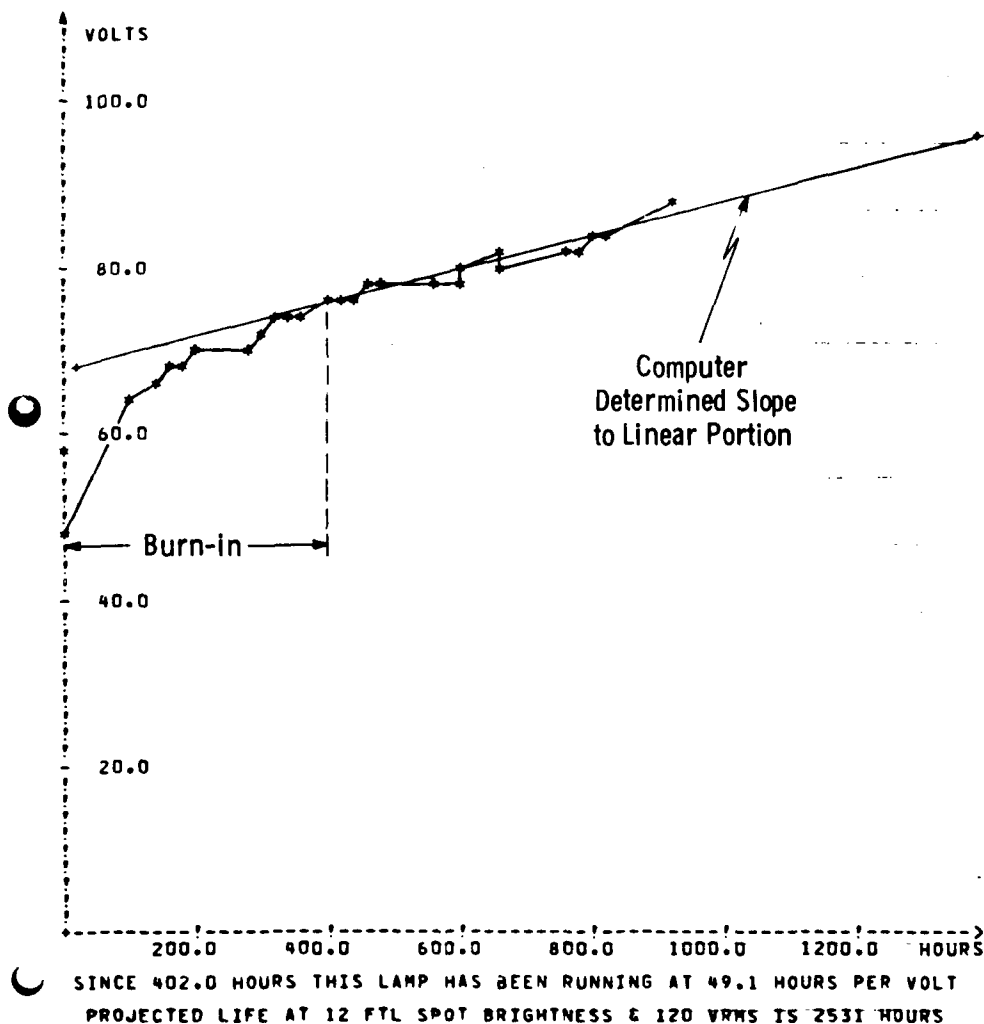


Figure 7.15 Example of the graphical output and numerical analysis of the computer-based software package written to support the phosphor maintenance investigation. (Refer also to Figure 7.14.)

Curve 720672-A

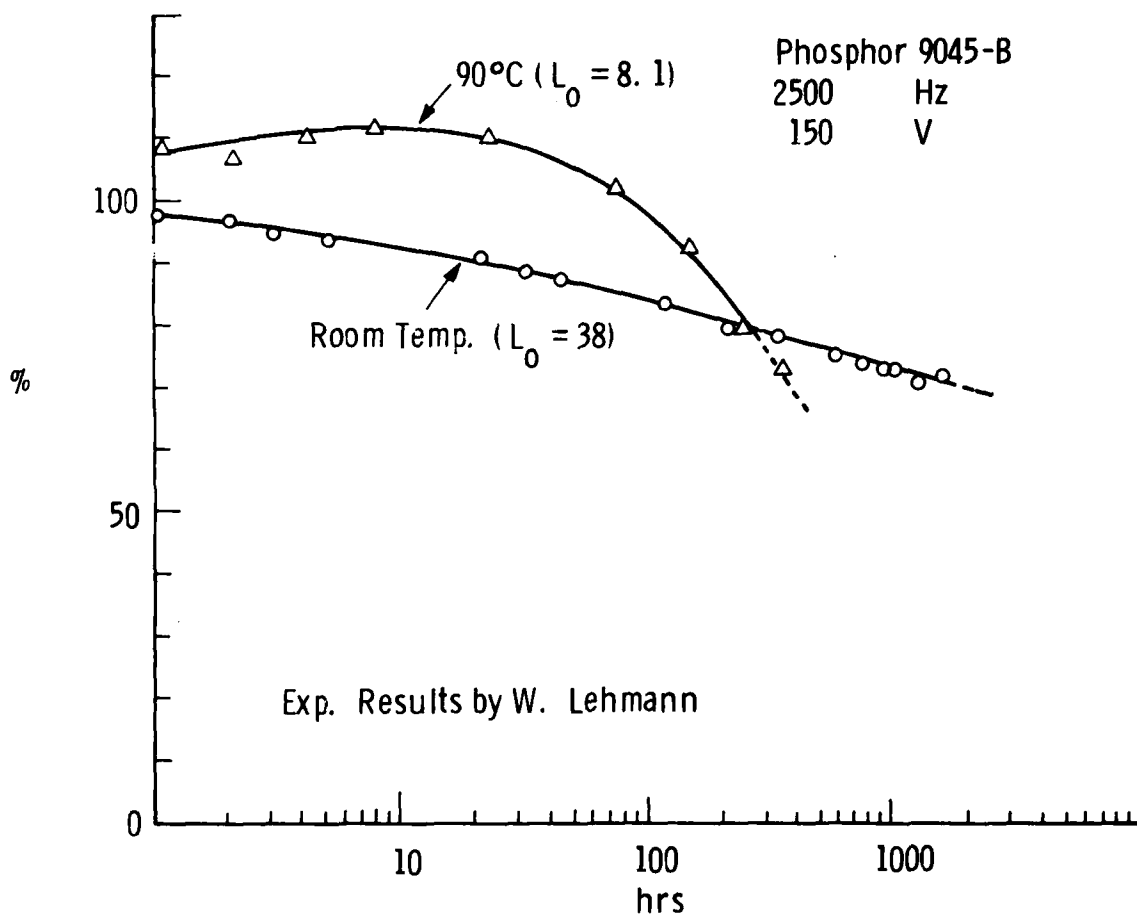


Figure 7.16 Westinghouse Phosphor 9045-B under life test at constant voltage and elevated temperature prior to program activity.

Having thus discussed the tools we developed for the study of 72°C phosphor maintenance, we described the following subsections results derived from varying the phosphor application technique, the binder chemistry, the electroding, and encapsulation.

#### 7.4.4 Intrinsic Phosphor Life at 72°C

As indicated in the discussion of technical strategy provided in Section 7.3, it was of paramount importance to determine whether the abysmal 72°C maintenance we observed with the spray starch technique was due to the phosphor itself or to other factors relating to its application and/or composition. In other words, it was important to determine whether, under optimal conditions of excitation, for example in a 72°C vacuum, the phosphor could be maintained for the program-required 500 hours.

At the time the subject program was proposed, we had firm evidence that the Westinghouse phosphor was capable of meeting the 500 hours 72°C life test specified. The pertinent data is shown in Figure 7.16. Here we observe two samples being driven at constant voltage at 25°C and 90°C over a period of 1000 hours. However the test cells used here were entirely differently constructed from our display, as noted in Table 7.1. They actually featured the "test chip" structure described in Section 7.4.1.

TABLE 7.1 Comparison of features of the high maintenance test lamps whose performance is shown in Figure 7.4.7 with the DMD display which failed after four hours at 72°C

	Temp.	Maintenance at Elevated Temperature	Binder	Drive Voltage	Freq.	Appli- cation Method	Electrode
DMD Display (Section 7.2)	72°C	< 4 hrs	cyano ethylated starch	80 V <sub>rms</sub>	5 kHz	Spray	PhO-Au
Special Test Lamps (Figure 7.4.5)	90°C	> 1000 hrs	Krylon	150 V <sub>rms</sub>	2.5 kHz	Brush	Al

Even this rough comparison suggested that the phosphor itself was not at fault. However, we felt that results similar to those shown in Figure 7. 16 should be reproduced to confirm the intrinsic properties of the phosphor more recently processed, and being used in the present program. Fate, however, interceded in that while we were trying to reproduce the Krylon binder result shown in Table 7.1, work with new binders provided a sample with an actual 743 hours maintenance with a 120 V<sub>rms</sub> drive at 72°C in vacuum. We thus adopted this result as exoneration of the phosphor proper from responsibility of the poor performance shown in line 1 of Table 7.1. The computer-generated analysis is shown in Figure 7.17. The importance of this result was that, although it was conducted in a vacuum test, it provided the direction we needed, that is, to focus on the physics and chemistry of the plastic binder and/or other factors relating to synthesis of the phosphor layer and its encapsulation.

#### 7.4.5 Reformulation of the Plastic Binder

Having exonerated the phosphor per se from responsibility for poor maintenance in the display, we focussed attention next on the binder. As indicated in Table 7.1 and in Section 7.3, this was synthesized from a mixture cyano ethylated starch and sugar. It was known to be chemically unstable at elevated temperatures and was therefore immediately subject to question in view of its good reputation at room temperature and below. In addition, the mix was also known to be hydrophylic. The adverse influence of water on phosphor performance has been discussed in Section 7.3.1. Finally, the solvents used for formulating the phosphor CE:S&S slurry were aceto nitride and DMF, and these were suspected as having a tendency to react with the Riston field isolation layer. All these factors pointed towards the desirability of discarding CE:S&S altogether and the excellent maintenances exhibited by the samples in Figure 7.16 naturally suggested using Krylon as a binder. We then rapidly found it was next to impossible to suspend the phosphor powder in the Krylon and, furthermore, subsequently to spray any slurry which was so formed. In addition, the lower dielectric constant of the

UPDATE 5-23-79

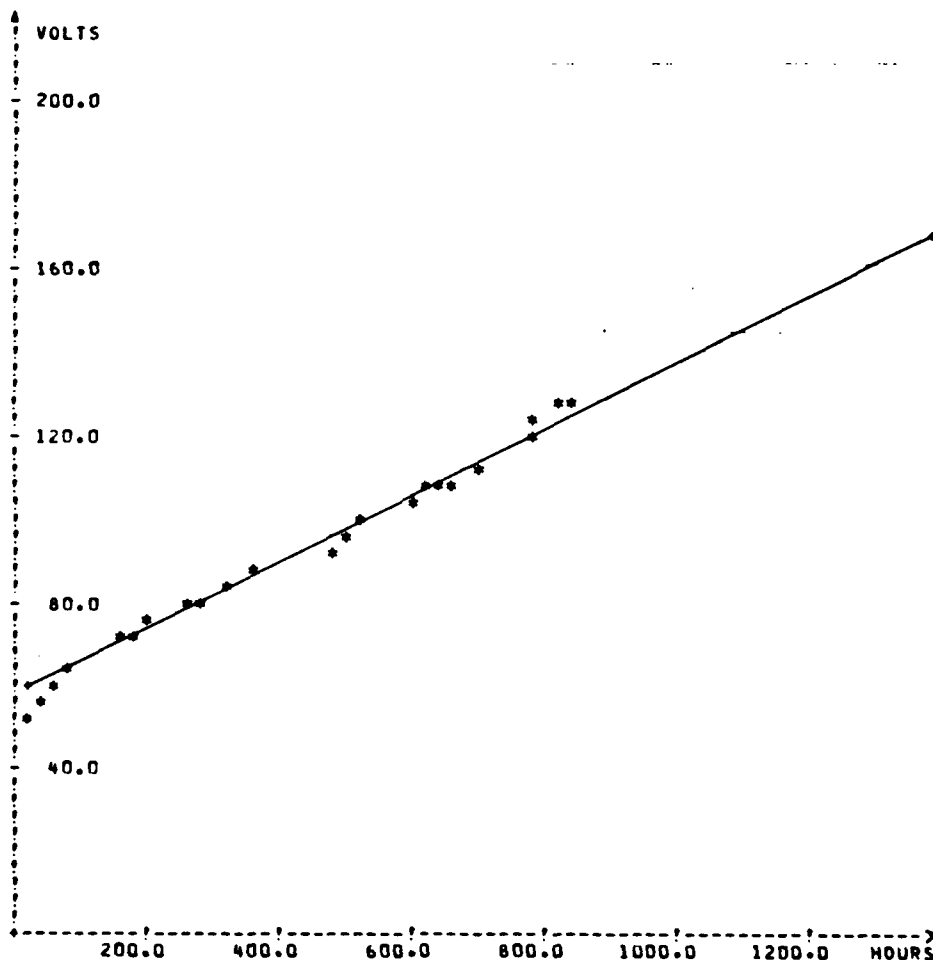
SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

POSTAGE 589-1  
STAMP 3  
3.6

FIGURING BOOK REFERENCE  
DATE FABRICATED 4-16-79  
TEST AMBIENT VAC  
TEST TEMPERATURE 72C

589-1,2 ARE TO  
MAKE DEFINITIVE TEST  
OF VALUE OF SECOND  
RINSE CLEANOUT IN  
RISTON DEVELOPMENT

BASE COAT WT .64  
TOP COAT 1 .21  
TOP COAT 2 .23  
PHOSPHOR WEIGHT 4.02  
SHEET RESISTANCE 150



SINCE 192.0 HOURS THIS LAMP HAS BEEN RUNNING AT 12.2 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 743 HOURS

Figure 7.17 Postage stamp Sample 589-1 which served to relieve the phosphor proper as a limiting factor in display maintenance at 72°C.

Krylon was likely to require higher drive voltages to secure adequate phosphor excitation.

At this point, we sought an entirely different binder and initiated work with cyano ethylated polyvinyl alcohol (CE:PVA). This material was known to have a dielectric constant of between 30 and 50 (about twice that of CE:S&S) to be relatively water clear, and was a single component material. Experiments were also initiated with a similar material, cyano ethylated polyvinyl chloride-acetate (CE:PVCA). We also were ready to study the usefulness of polymethyl methacrylate, a material chemically similar to Krylon, but fortunately CE:PVA yielded encouraging progress from the start. The cyano ethylation process was performed successfully, to about 96%, and 10% and 20% solutions in a 60-40 MEK-cyclohexanone solution were prepared for evaluation.

Preliminary results shown in Table 7.2 compare projected 72°C half lives with lamps driven at 80 V<sub>rms</sub> and 5 kHz. These measurements were taken after about 200 hours. It shows that the CE:PVA we were then using performed remarkably better at 72°C than CE:S&S, but not as well as Krylon, which alone was somewhat in excess of program requirements but, again, could not readily be used for the display application for reasons noted previously. In particular, we note the relatively low brightnesses provided by the Krylon sample, probably as a consequence of its lower dielectric constant.

TABLE 7.2 Preliminary comparison of maintenance of identical phosphors in binders of Krylon, CE:PVA and CE:S&S at 72°C in a dry air ambient. (Drive voltage is 80 V<sub>rms</sub> at 5 kHz).

Sample No.	Binder	Initial Brightness (ft-L)	Post-burn in Brightness (ft-L)	Projected 72°C Half-Life
1	Krylon	20	8	850 ± 100 hrs
2	CE:PVA	60	13	125 ± 40 hrs
3	CE:S&S	25	12	< 4 hrs



All three samples shown in Table 7.2 were prepared by brushing the phosphor onto the binder, instead of spraying, and featured the test chip configuration in which an opaque aluminum top electrode and transparent NESA-coated glass substrates through which emission was viewed. Although this was hardly a display-compatible process, it did show early progress in the right direction. We had learned from experiments like these that CE:PVA provided extraordinarily high initial brightnesses and exhibited excellent maintenances at 20°C. However performance at 72°C was not adequate, even in vacuum testing.

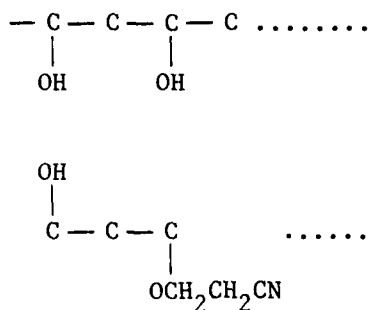
Further attention was then focussed on the CE:PVA itself. We, and an earlier worker in this field, had reported a characteristic darkening in plastic binders when exercised at 72°C. Krylon lamps, however, did not darken and neither did CE:S&S ones or CE:PVA without phosphor. We believed at the time, and in retrospect, probably correctly, that moisture reacting with the phosphor was responsible, although we have not determined the precise mechanism. Neither was it clear then, or is it now, to what extent the darkening per se was responsible for seemingly related maintenance and brightness inhibition. It probably contributes, but chemical and/or physical degradation of the phosphor grains themselves reacting to moisture originating in the binder was the prime origin.

There were two suspected sources of this moisture.

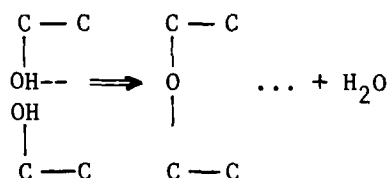
(1) Adsorbed environmental water vapor: It became increasingly clear that CE:S&S was more vulnerable than CE:PVA to this problem, and in turn imposed severe environmental constraints during phosphor application and testing. In fact, it was this feature of CE:S&S together with its lower dielectric constant (about half of that of CE:PVA) which rendered it less favorable for our purpose as a binder.

(2) Moisture produced during a condensation reaction in partially cyanoethylated materials.

A representation of the partially cyanoethylated PVA molecule is



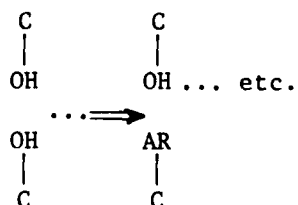
wherein the  $\text{OCH}_2\text{CH}_2\text{CN}$  chain has replaced an OH group during partial cyanoethylation. The problem arises from the OH groups. During a condensation reaction (whose likelihood is increased substantially between 20 and 72°C!), these are replaced by oxygen crosslinking which in itself is not deleterious. The problem is the release of water as implied by the transformation



Our continuing effort investigated two ways of suppressing this second source of water which was believed to inhibit light emission from the phosphor and ultimately the behavior of the display.

The first approach was to increase the ratio of cyanoethylation by longer reaction times and higher reaction temperature, thereby leaving fewer unreplaced OH groups to crosslink with the release of water.

The other approach was to "block" uncyanated OH groups with isocyanate groups adding an aromatic compound (AR):



While these aromatic compounds were not likely to match the dielectric constant produced by 100% cyanoethylation, their addition and the subsequent suppression of the release of water was likely to be much faster. In addition, the resulting binder was likely to have a higher flow temperature, rendering it less likely to distort the gold top electrode during high temperature testing.

In an effort to reduce the concentration of hydroxyl groups (OH) in the PVA, which were believed responsible for the formation of water during binder heating through a condensation mechanism followed by cross-linking, we extended the cyanoethylation reaction time to increase the cyanoethyl:hydroxyl ratio. Run LC-37087 resulted in a highly cyanoethylated PVA whose structure showed the smallest concentration through IR analysis of residual OH groups of all CE:PVA made at that time.

In order to further diminish the OH concentration, samples of LC-37087 were reacted with phenyl isocyanate, which freely reacts with residual OH groups. This compound (LC-37087 PI) showed practically no OH groups in its structure according to infrared and hydroxyl number analyses. Their dielectric constants are:

LC-37087	1000 Hz = 29.0
	5000 Hz = 26.0
LC-37087(PI)	1000 Hz = 24.5
	5000 Hz = 21.5

The introduction of phenyl isocyanate (PI) groups reduced the dielectric constant slightly, probably because they interfered with the free motion of the cyanoethyl group; on the other hand, the more rigid and encumbering PI groups tended to increase the flow temperature of the binder thus modified.

These materials were the ones finally adopted to replace the CE:S&S mixture which had been our starting point. Some of the exciting maintenances and initial brightnesses we observed using them are reported subsequently in Section 7.5. These results were not due to

the new binder formulation alone. The related developmental activity described above was conducted in parallel with work on reconfiguring the phosphor-binder layers to be described in the next subsection. However, before proceeding, it is appropriate to relate that the material presented here represents only a part of the sum total of activity undertaken. We also tried the much-heralded approach of microencapsulation, aluminum oxide isolation layers, phosphor grain, size separation and addition of barium titanate to the plastic to increase its dielectric constant. We were unable, however, to derive any significant merit from these approaches.

#### 7.4.6 The Hybrid Spray-Brush-Spray Phosphor Application Technique

We had several reasons for needing to examine the base-line phosphor application procedure involving the spraying of a slurry as described in Section 7.3. One was that this technique wasted an extraordinary amount of the precious phosphor material. Each new batch had to be properly characterized and evaluated outside the scope of our mission concerning maintenance at 72°C.

A second reason involves the comparison of the widely differing maintenances exhibited by the same phosphor under different conditions of encapsulation as shown in Table 7.1. Here we had adequate 72°C phosphor maintenance in a brushing application but totally unacceptable maintenance produced by our then standard technique of spraying. More importantly still, we had observed in a wide variety of experimental configurations that any kind of sample with superior initial brightness at a given test voltage or, conversely requiring lower voltage to generate a given brightness, in general provided higher maintenance when life-tested at a fixed brightness. A supporting analysis of this observation is provided by the data shown in Figure 7.18. Here we have ratcheted voltage measurements for a Krylon sample and several CE:PVA and CE:S&S samples. However, this happens to be a plot of the logarithm of voltage versus the square root of time at constant brightness. One experimentalist in our group had determined that this plot tended also to provide a linear fit as shown. In any event, the conclusion tends to be similar concerning the desirability, from the 72°C maintenance viewpoint, of fabricating structures with as low initial threshold voltages as possible.

With reference to Figure 7.18, we have an approximate fit given by

$$t = A \log \left( \frac{V}{V_0} \right)^2$$

where  $t$  = time

$V$  = voltage

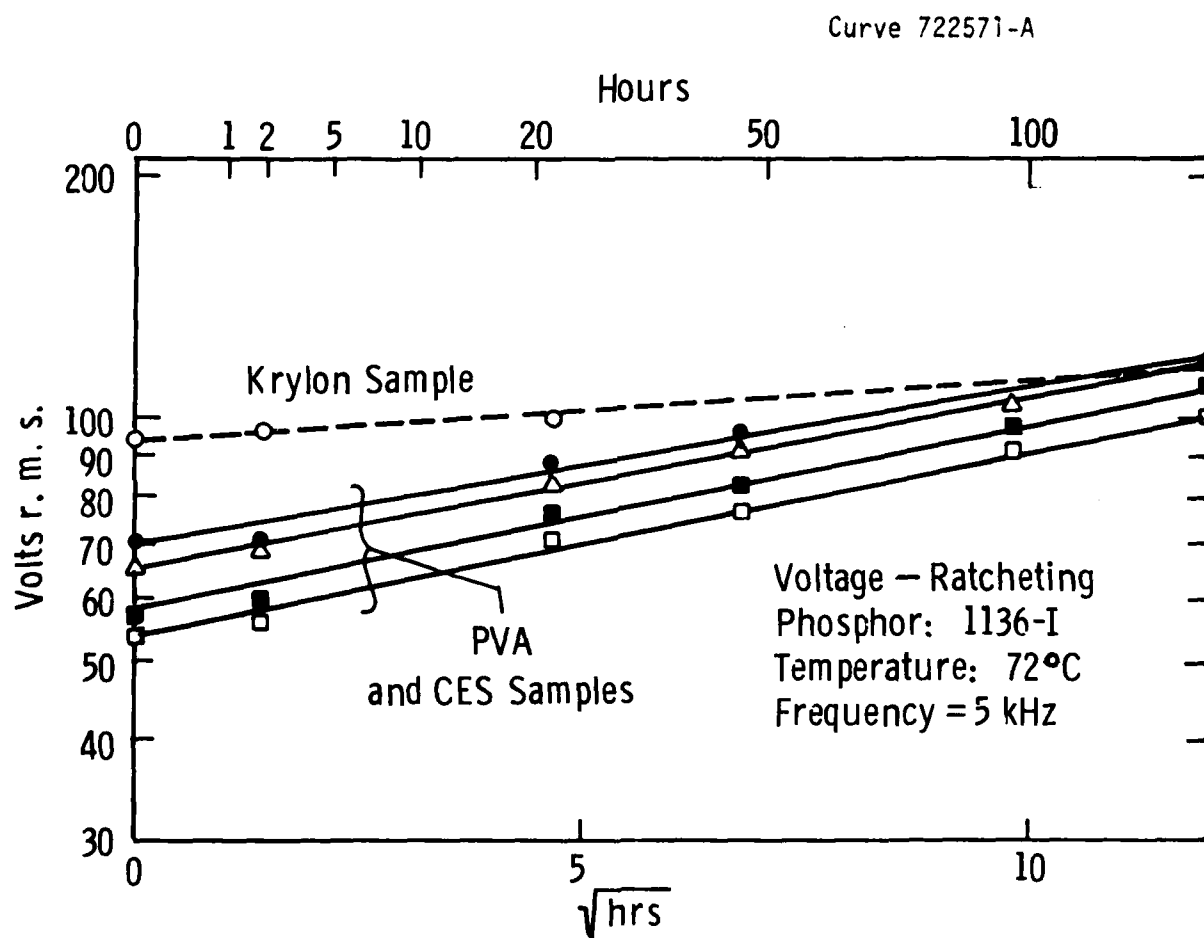


Figure 7.18 Logarithm of ratcheted voltage versus square root of time in dry box life testing at 72°C.

$V_o$  = threshold voltage

A = constant

for the four parallel straight lines. An approximate value of the constant A is 22.5 hours. This then enables us to predict what threshold voltage should be aimed for in generating any given maintenance within the scope of voltage ratcheting. For example, since

$$V_o = \exp \left( \log V_{\max} - \sqrt{\frac{T}{A}} \right)$$

where  $V_{\max}$  is the maximum allowed excitation voltage and T the maintenance, it follows that 500 hours maintenance with a maximum permissible voltage of 100  $V_{\text{rms}}$ , the threshold voltage of the structure should be about 33  $V_{\text{rms}}$ . This naturally means that the brightness for viewability should be initially observed at this figure. We had previously determined that, for our display in a 2000 ft-C ambient, this initial spot brightness had to be 12 ft-L corresponding to a geometrical average of 3.6 ft-L. Consequently, we always had a weather eye on sample configurations which tended to produce higher initial brightness, regardless of the materials featured in the lamp construction. Later in Section 7.5.1 we present some other data that confirms this hypothesis. In addition, in view of the fact that the phosphor layer technology we were developing had to respond to eventual application constraints wherein it was switched by thin film transistors of respectable but limited voltage sustaining capability, it was highly desirable to do everything possible to run the phosphor-binder composite structure at as low a voltage as possible. Figure 7.19 compares geometrical features produced by the brushing and the spraying techniques. In the straight brushing technique, the binder coats are conveniently applied by flowing the material over the substrate. The intermediate phosphor layer is formed by spilling some powder onto a heat treated bottom coat, to render it adhesive, and carefully distributing the powder with a very fine-haired brush. This technique is very economical with the supply of phosphor but, unfortunately, does not lend itself well to the situation when one is trying to

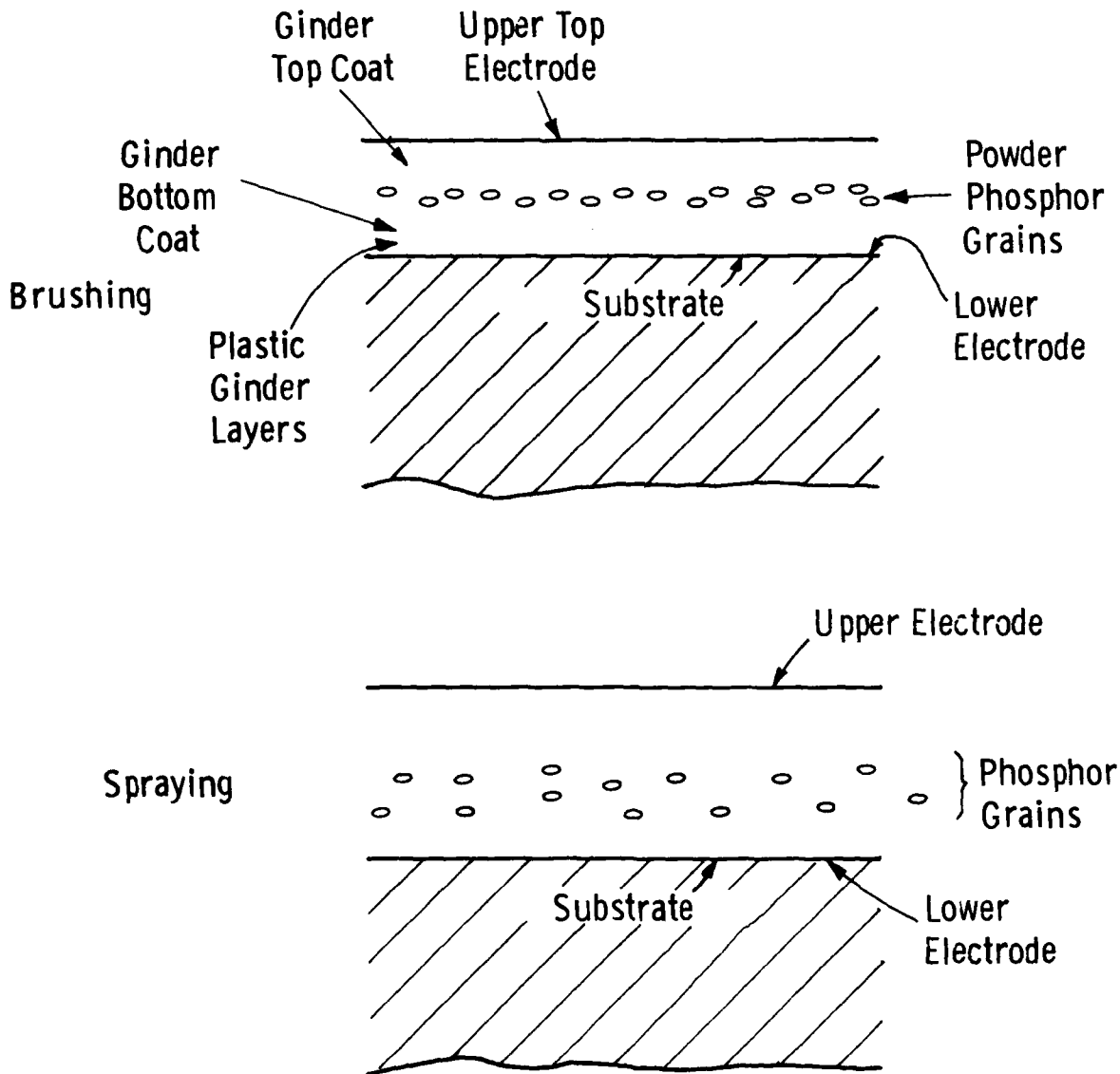


Figure 7.19 Comparison of the geometry and gross features of plastic-phosphor systems provided by the brushing and spraying techniques.



apply the phosphor to regions defined by openings in a field-isolating layer of Riston as in the case of the subject display.

With reference to Figure 7.20, we observe that the end result, wherein minimal thickness of the 'clear coat' binder layers are needed to properly isolate the phosphor and to provide adequately smooth topology for upper electroding, the composite thickness of the structure, and thus its required drive voltage, tends to be higher, all other things being equal, for phosphor application by spraying.

Consequently, we developed the so-called "hybrid" technique of first spraying on the lower level of clear coat over the Riston isolation, brushing the phosphor onto this layer, and then applying only enough top layer clear coat of CE:PVA to provide a finishing topology smooth enough for electrical integrity of the gold top electrode. This process is the one featured in our final recommended process for phosphor layer formulation described later in Section 7.6. The commonality between the structures produced by the hybrid spray-brush-spray technique and the requirements for low initial threshold voltage were determined to be the following:

- 1) A "thin" smooth layer of plastic over the bottom electrode.
- 2) A thin dense layer of small ( $< 20\mu$ ) phosphor particles which apparently can be applied only by brushing.
- 3) Vulcanization of the bottom layer of plastic.
- 4) A "thin", smooth, top layer of plastic.
- 5) A top electrode which absorbs no more than 25% of the light emitted by the phosphor.
- 6) A moisture impervious encapsulation system.

Much effort was subsequently directed towards making the top and bottom plastic layers as thin as possible, with the result of the limiting configuration shown in Figure 7.21. This limiting structure, not unexpectedly, had the following characteristics:

- 1) Low threshold voltage but inadequate voltage sustaining capability for high brightness.
- 2) Frequent top electrode failure.
- 3) Voltage for 12 ft-L, say, independent of the aggregate weight of plastic (Krylon, CE:S&S, CE:PVA, etc.) used, as indicated in Figure 7.22.

In the limiting region the phosphor particles themselves sustain all the applied voltage and increased brightness can be generated at given voltage only by decreasing the phosphor particle sizes themselves. Ultimately, our goal would be ultra-small particles and very thin (but in excess of phosphor particle size) layers of plastic of high dielectric constant. These factors have been taken into account in our recommended formulation of the final display compatible process described in Section 7.6.

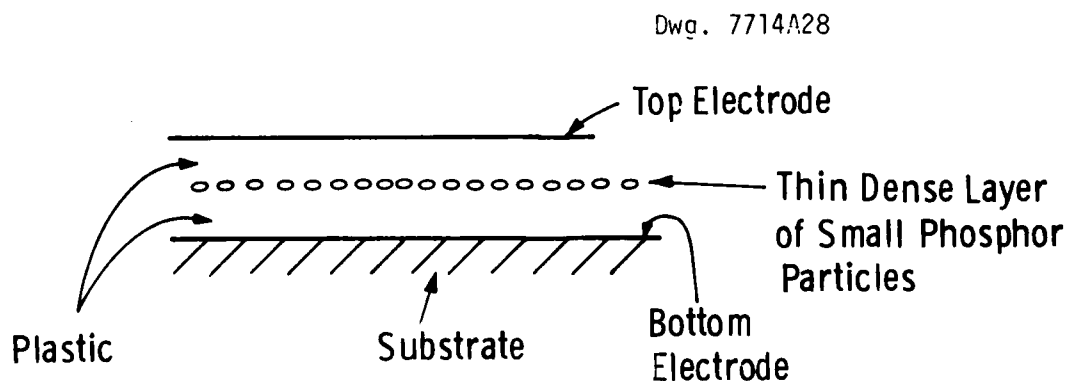


Figure 7.20 The "ideal" powder phosphor layer structure

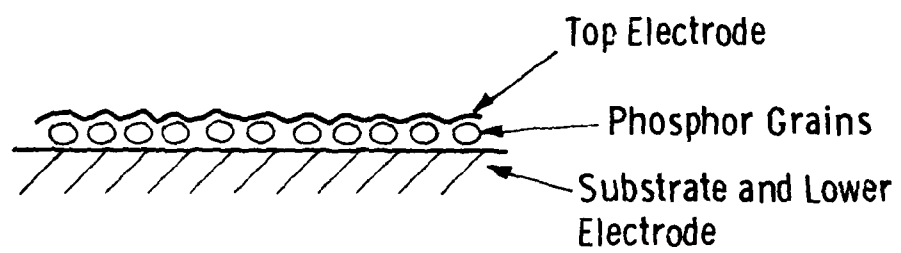


Figure 7.21 The limiting configuration for ultra low threshold voltages

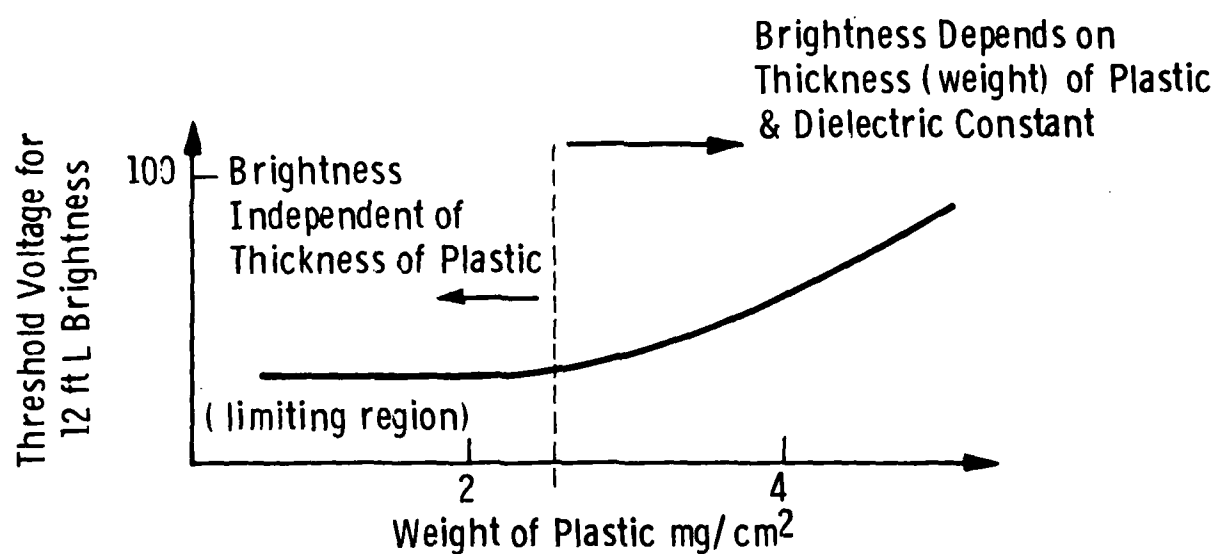


Figure 7.22 Typical behavior of threshold voltage with aggregate binder thickness (weight).

### 7.5 Selected Results of Phosphor Life Testing

The results presented in this section and the conclusions so derived are "selected", not in the sense of their being the "best", but because they alone are relevant to the phosphor and encapsulation techniques related to final recommended process formulations for the display presented in Sections 7.6 and 8.4, respectively. During this investigation, numerous other approaches were evaluated to a greater or lesser extent but without meaningful results.

The material in this section has been divided into three subsections. The first reviews results pertaining to intrinsic phosphor life, an integral part of our original technical strategy. The second contains analyses describing the impact of alternative encapsulation materials on phosphor maintenance. Results for both sections are presented within the framework of maintenance evaluation by voltage ratcheting, using postage stamp test vehicles, the computer-based data logging and analysis system, and phosphor excitation at 5 kHz to a maximum allowed voltage of 120 V<sub>rms</sub>, which seems quite conservative in view of the transistor test data we have earlier presented in Section 5.4. One could therefore argue that, to a certain extent, these are "worst case" results and conclusions.

A third subsection presents results of a variety of experiments related to phosphor performance, largely within the context of the alternative display drive and addressing scheme discussed in Section 9.5.

#### 7.5.1 Discussion of Results Pertaining to Intrinsic Phosphor Life at 72°C

In review, "intrinsic phosphor life" pertains to phosphor maintenance under optional conditions wherein ill-effects deriving from exposure to the ambient atmosphere and/or materials used in sealing and encapsulation are, as far as possible, eliminated. This was done by assembling postage stamp test vehicles only to the application of the top electrode, necessary for driving, and conducting the life test in vacuum ovens at 72°C. The purpose was to assess separating the inherent characteristics of the phosphor layer in this respect.

Pertinent data, summarizing test vehicle configurations and results are assembled in Table 7.3. The samples are identified by numbers describing the order in which they were fabricated and life tested. Six experiments were involved and their brief descriptions are listed for reference purposes. In some of these experiments, other partially or fully encapsulated samples were also tested, but Table 7.3 data is restricted only to those undergoing 72°C measurements, in vacuum, with no encapsulation. The first experiment involved "calibration" of the hybrid layer formulation featuring the new CE:PVA binder. The top electrode was applied as described in Section 7.2 by conventionally depositing lead oxide, followed by a thin transparent layer of gold onto the binder top coats. The next experiment evaluated alternative state-of-the-art encapsulants. Only two samples, 575-1 and 576-6, for this experiment are listed. These alone conformed to "intrinsic" status and were really tested only as control samples. Experiments 3 and 4 really are two different sample classifications constituting a single experiment. It was undertaken as part of the phosphor layer development activity when we read reports of work conducted elsewhere which demonstrated ultra-high maintenance of powder phosphor in lamp test vehicles featuring encapsulation with glass powder. There was one exception in which there was poor maintenance. This occurred when the glass from which the powder was ground contained lead. We reconciled this observation with our historical use of a layer of lead oxide to provide a base on the topmost clear coat of CE:PVA for the gold-evaporated top electrode. In addition, we recalled that the original high temperature maintenances Westinghouse phosphor had provided had been observed on test chips whose electrodes were NESA glass and opaque aluminum. Experiments 3 and 4 were thus formulated to compare the performances of lead oxide and cadmium fluoride, a supposedly functional alternative material, in otherwise identical test vehicles. A model for the reported and actually observed deleterious effect of lead on the zinc sulfide phosphor is described in Section 7.1.

Experiment 5 was a re-evaluation of alternative encapsulation techniques and served to verify the apparent superiority of cadmium

fluoride over lead oxide as a top electrode adhesive or base. As in Experiment 2, the postage stamps 577-1 and 577-2, listed, served as control samples.

Finally, the sixth experiment focussed on less than desirable observations made on routinely developed Riston isolation layers. A so-called "second rinse" was incorporated into the process to remove remnants of resist scum from the bottom electrode. As the results indicated, this had a profound and positive impact on high temperature phosphor to performance.

In all cases, the subject samples of Table 7.3 had the new CE:PVA binder and were constructed by the new hybrid brush-spray procedure. All were tested in vacuum at 72°C. However, random variations in lamp fabrication provided some variation of certain physical parameters. These were the weights of the clear coat binder and the phosphor itself and, also, the top electrode sheet resistance. All these were determined from special purpose process control samples otherwise simultaneously fabricated with the postage stamps.

The results in Table 7.3 were all coupled directly from the computer analysis and data presentations, extracted directly from our data logging system, and shown in Figures 7.23 through 7.36 for samples 570-2 through 577-2. Computer output for sample 589-2 is shown in Figure 7.37 and that for sample 589-1 has already been shown in Figure 7.17.

In Table 7.3 under Results, the fifth through third columns from the right tabulate respectively the so-called "inverse degradation" (which is simply the slope of Region II in Figure 7.12) the maintenance M in hours and the threshold voltage  $V_T$ . The maintenance is defined for 120 V<sub>rms</sub> maximum permissible excitation voltage. Ideally, of course, one seeks a high inverse degradation rating and maintenance.

Table 7. 3 also indicates the duration of the test. In practice, this was determined either by onset of burn-out (Region III in Figure 7.13), electrode failure, or ratcheting voltage in excess of

UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	570-2	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-09-78
OVEN NUMBER	2	TEST AMBIENT	VAC
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C
ENCAP TEST #1		BASE COAT WT	---
CONTROL SAMPLE		TOP COAT 1	---
WITH NO ENCAPSULATION		TOP COAT 2	---
(KRYLON OVER TOP ELECTRODE)		PHOSPHOR WEIGHT	---
		SHEET RESISTANCE	---

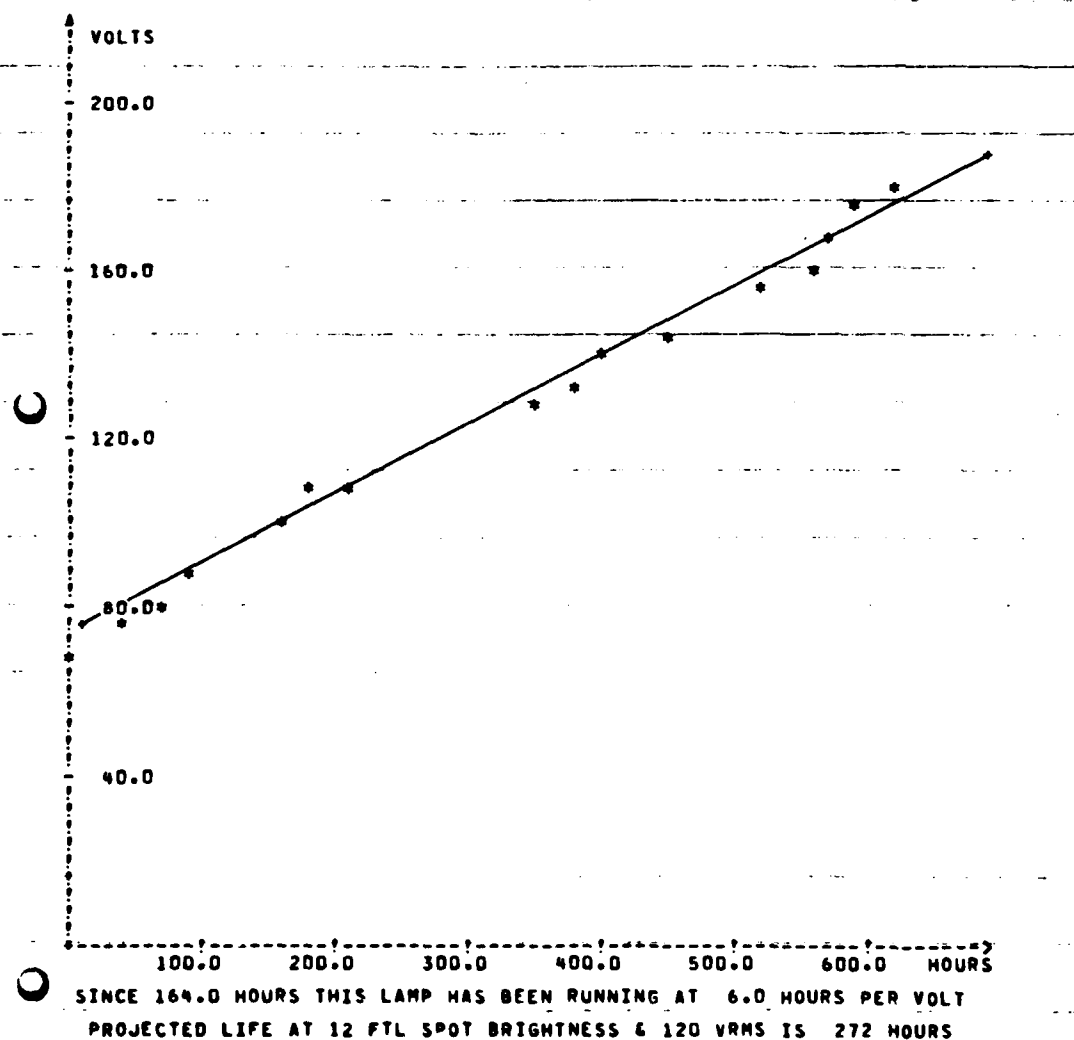


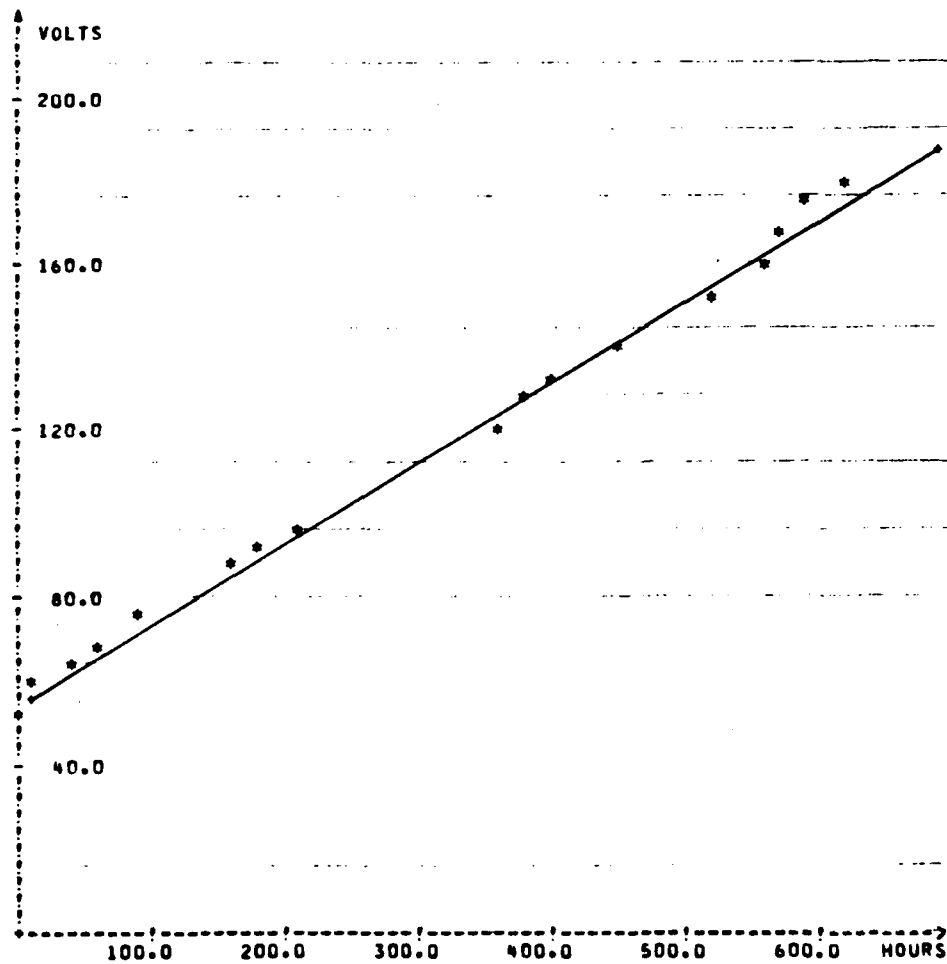
Figure 7.23

Computer analysis of life testing data for postage stamp Sample No. 570-2 participating in Experiment 1 on 72°C phosphor life in vacuum and listed in Table 7.3.



UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	574-2	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-09-78
OVEN NUMBER	2	TEST AMBIENT	VACUUM
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C
SAME AS 570-2		BASE COAT WT	---
		TOP COAT 1	---
		TOP COAT 2	---
		PHOSPHOR WEIGHT	---
		SHEET RESISTANCE	---



SINCE 91.8 HOURS THIS LAMP HAS BEEN RUNNING AT 5.2 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 324 HOURS

Figure 7.24 Computer analysis of life testing data for postage stamp Sample No. 574-2 participating in Experiment 1 on 72°C phosphor life in vacuum and listed in Table 7.3.

UPDATE

SAMPLE NUMBER 575-1  
 SAMPLE TYPE POSTAGE STAMP  
 OVEN NUMBER 2  
 BRIGHTNESS 3.6

FIGURING BOOK REFERENCE 207951-145  
 DATE FABRICATED 12-01-78  
 TEST AMBIENT VACUUM  
 TEST TEMPERATURE 72 DEG C

PREDRIED STYCAST & SILICONE  
 RTV TEST WITH KYLON  
 OTHER LAMPS IN SERIES 1 THRU 8  
 NO COVER GLASS  
 NO ENCAPSULATION

BASE COAT WT .45  
 TOP COAT 1 .22  
 TOP COAT 2 .46  
 PHOSPHOR WEIGHT ----  
 SHEET RESISTANCE ----

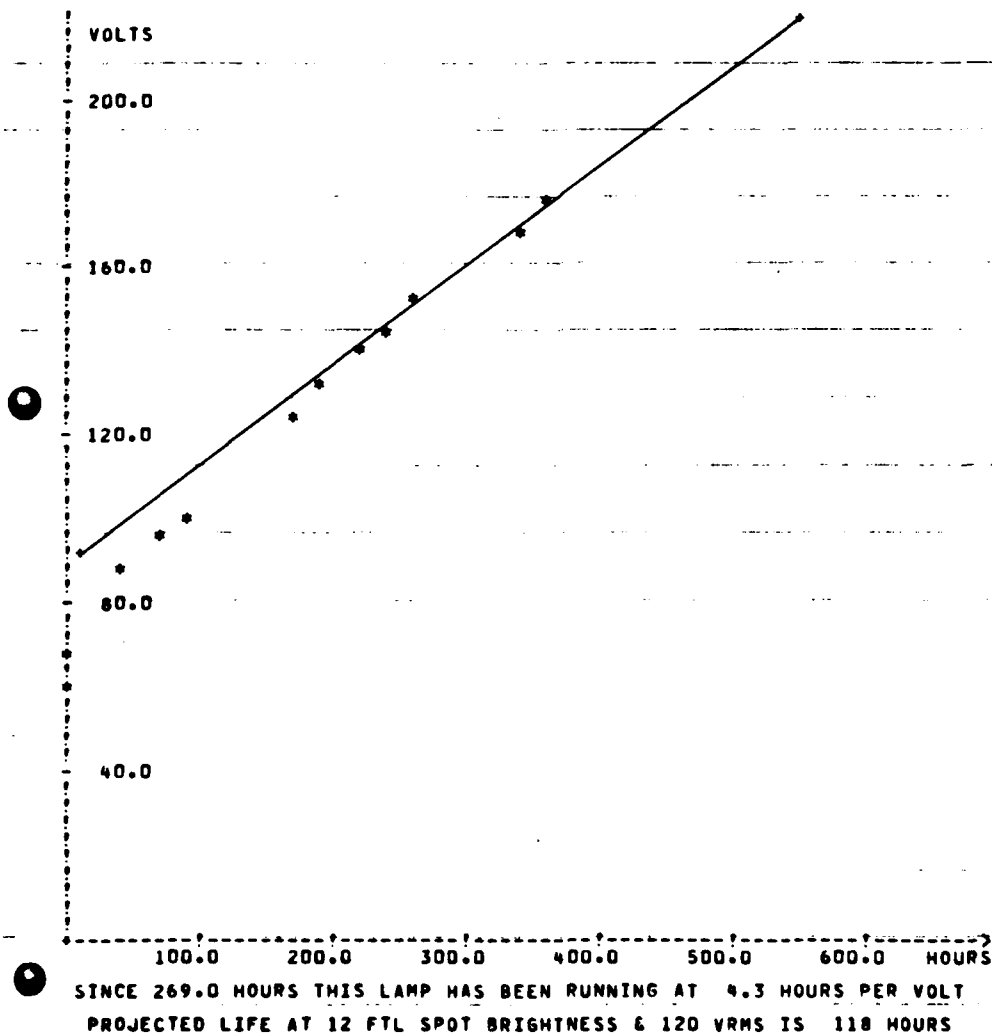


Figure 7.25

Computer analysis of life testing data for postage stamp  
 Sample No. 575-1 participating in Experiment 2 on 72°C  
 phosphor life in vacuum and listed in Table 7.3.

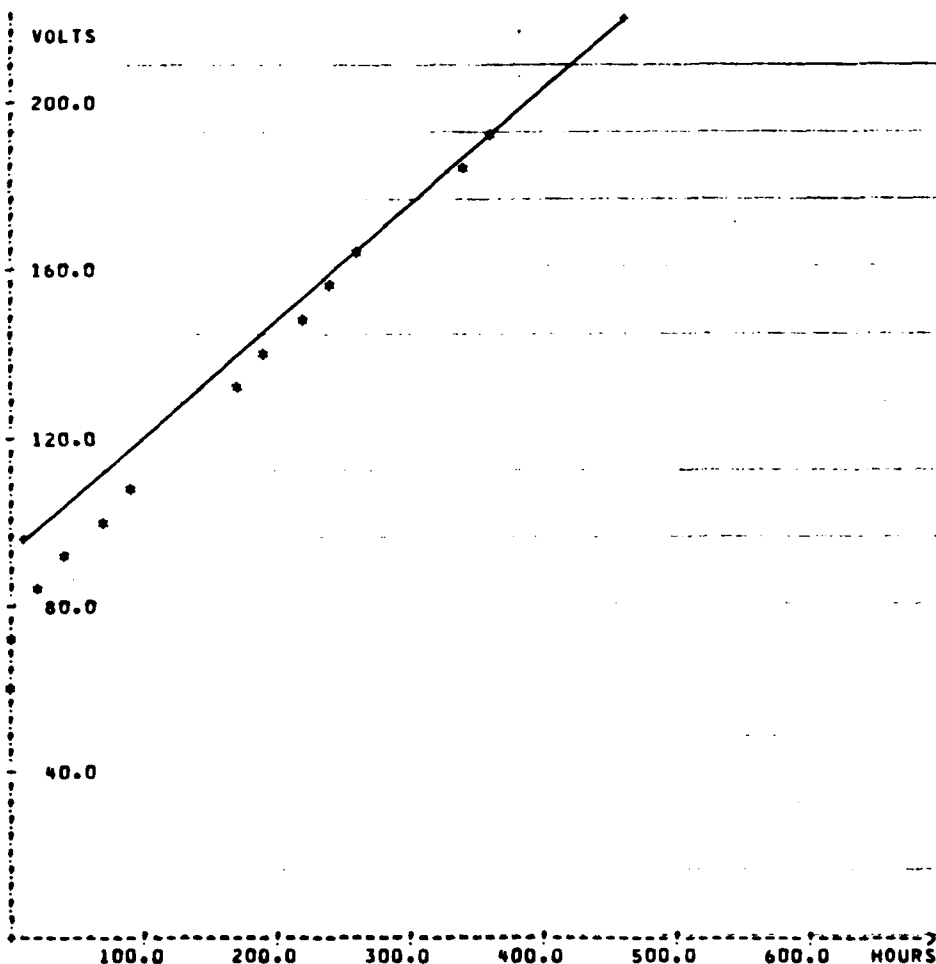
UPDATE

SAMPLE NUMBER 575-6  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT  
TEST TEMPERATURE 72 DEG C

PREDRIED STYCAST & SILICON  
RTV TEST WITH KRYLON  
OTHER LAMPS IN SERIES 1 THRU 8  
SECOND STANDARD  
SAME AS 575-1

BASE COAT WT .45  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT -----  
SHEET RESISTANCE -----



SINCE 269.0 HOURS THIS LAMP HAS BEEN RUNNING AT 3.7 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 95 HOURS

Figure 7.26 Computer analysis of life testing data for postage stamp Sample No. 575-6 participating in Experiment 2 on 72°C phosphor life in vacuum and listed in Table 7.3.

UPDATE 1-25-79

SAMPLE NUMBER 576-1  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6

ONE OF FOUR CDF2  
POSTAGE STAMPS  
SEE 576-4

FIGURING BOOK REFERENCE  
DATE FABRICATED ---  
TEST AMBIENT VAC ---  
TEST TEMPERATURE 72 C

BASE COAT WT .38  
TOP COAT 1 .12  
TOP COAT 2 .29  
PHOSPHOR WEIGHT 4.2  
SHEET RESISTANCE 82 OHM

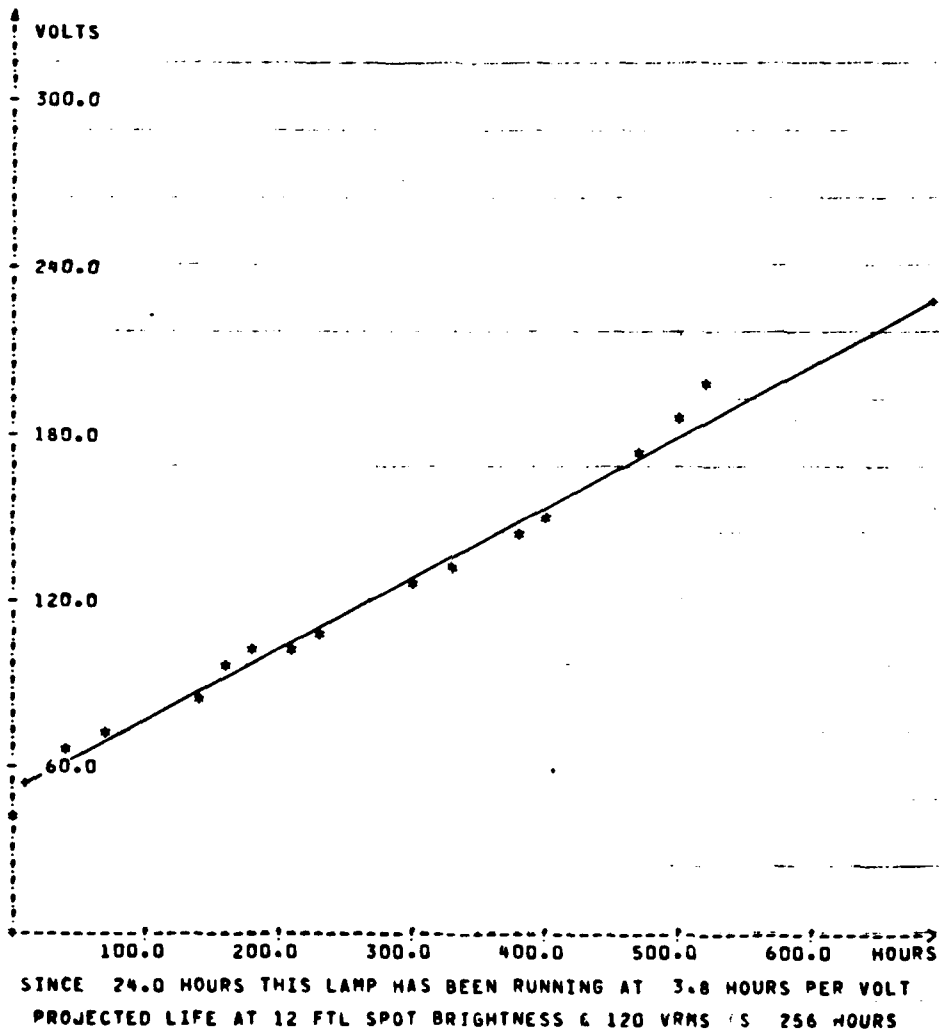


Figure 7.27 Computer analysis of life testing data for postage stamp Sample No. 576-1 participating in Experiment 3 phosphor life in vacuum and listed in Table 7.3.

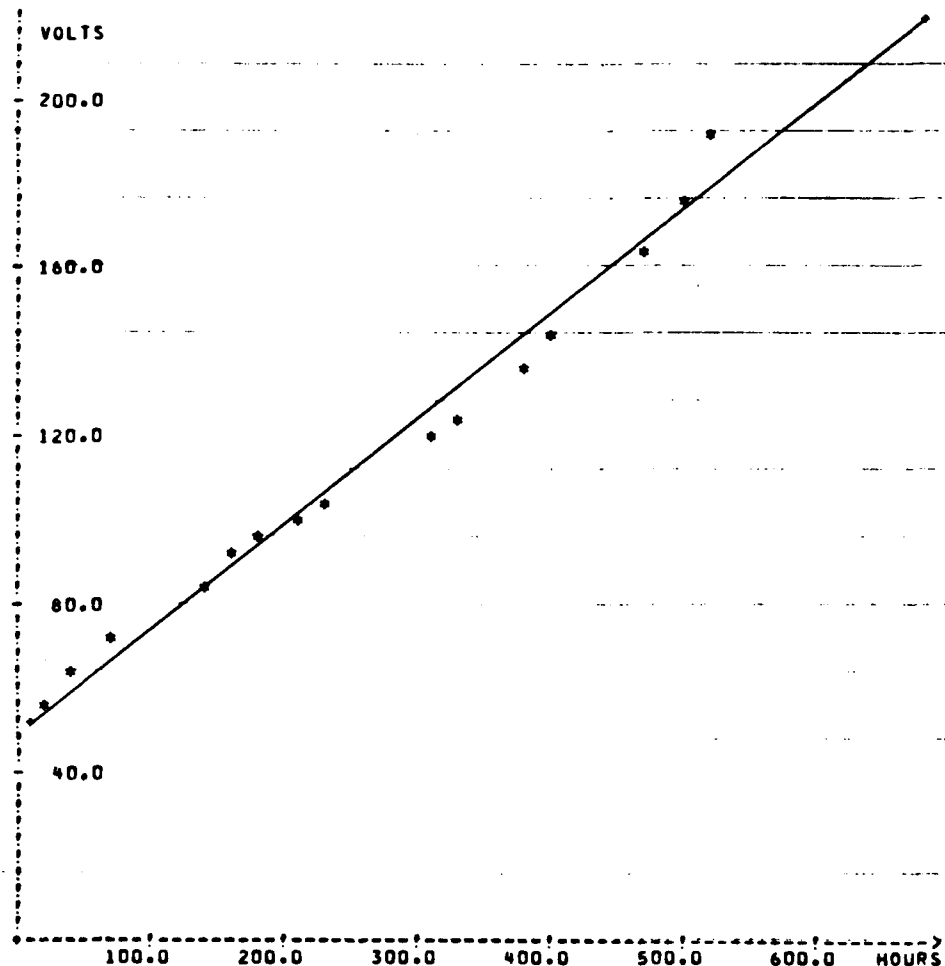
UPDATE 1-25-79

SAMPLE NUMBER 576-2  
SAMPLE TYPE PS  
OVEN NUMBER 1  
BRIGHTNESS 3.6

COMPARE PBO AND  
OF2 UNDER GOLD  
76-1 THRU 4 ARE  
HRU 8 ARE PBO

FIGURING BOOK REFERENCE NONE  
DATE FABRICATED ---  
TEST AMBIENT VAC ---  
TEST TEMPERATURE 72 C

BASE COAT WT .38  
TOP COAT 1 .11  
TOP COAT 2 .24  
PHOSPHOR WEIGHT 4.36  
SHEET RESISTANCE 58 OHM



SINCE 24.0 HOURS THIS LAMP HAS BEEN RUNNING AT 4.1 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 280 HOURS

Figure 7.28

Computer analysis of life testing data for postage stamp  
Sample No. 576-2 participating in Experiment 3 on 72°C  
phosphor life in vacuum and listed in Table 7.3.

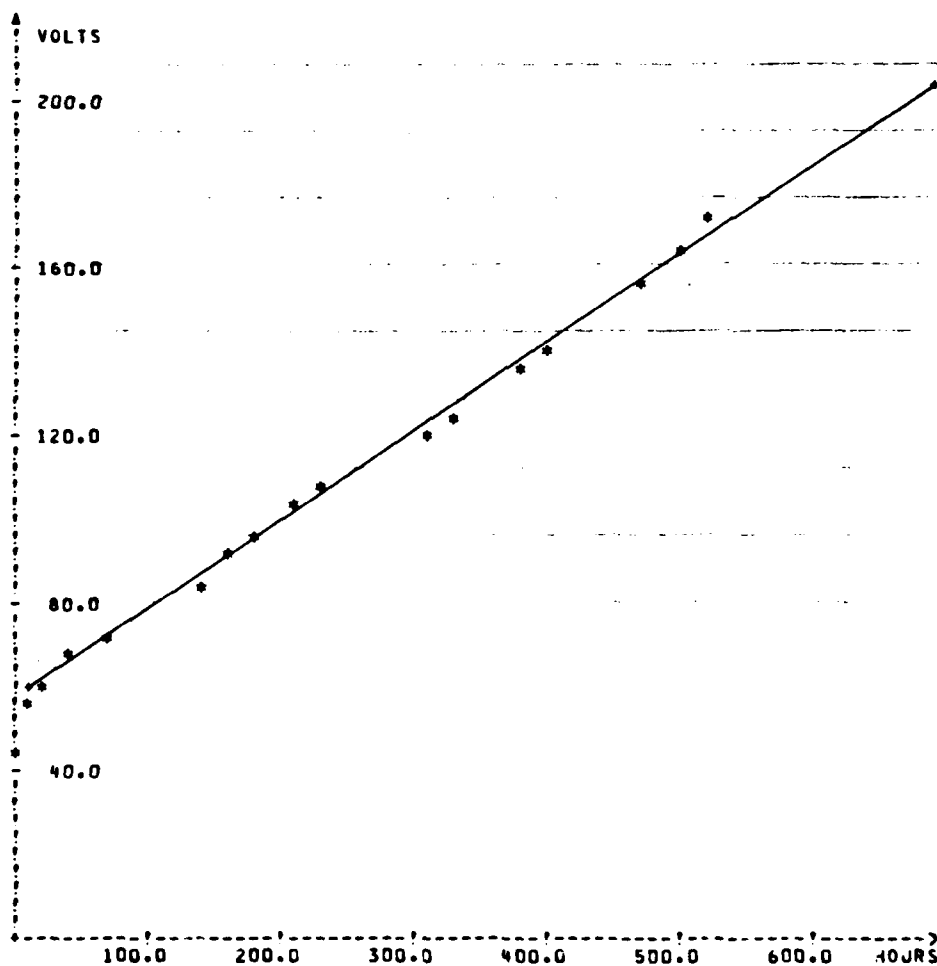
UPDATE 1-25-79

SAMPLE NUMBER 576-3  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6

FIGURING BOOK REFERENCE NONE YET  
DATE FABRICATED STEVE HAS IT  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

SAME AS 576-2

BASE COAT WT .42  
TOP COAT 1 .1  
TOP COAT 2 .28  
PHOSPHOR WEIGHT 4.36  
SHEET RESISTANCE 66 OHM



SINCE 48.0 HOURS THIS LAMP HAS BEEN RUNNING AT 4.7 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 222 HOURS

Figure 7.29

Computer analysis of life testing data for postage stamp  
Sample No. 576-3 participating in Experiment 3 on 72°C  
phosphor life in vacuum and listed in Table 7.3.

UPDATE 1-12-76

SAMPLE NUMBER 576-4  
 SAMPLE TYPE POSTAGE STAMP  
 OVEN NUMBER 1  
 BRIGHTNESS 12 FOOT LAMPERTS

FIGURING BOOK NONE  
 DATE FABRICATED -VACUUM  
 TEST AMBIENT VACUUM  
 TEST TEMPERATURE 72 C

ONE OF FOUR COF2  
 POSTAGE STAMPS  
 SEE 576-8  
 BURN OUT AT 140 HOURS

BASE COAT WT .43  
 TOP COAT 1 .11  
 TOP COAT 2 .28  
 PHOSPHOR WEIGHT 4.04  
 SHEET RESISTANCE 28 OHM

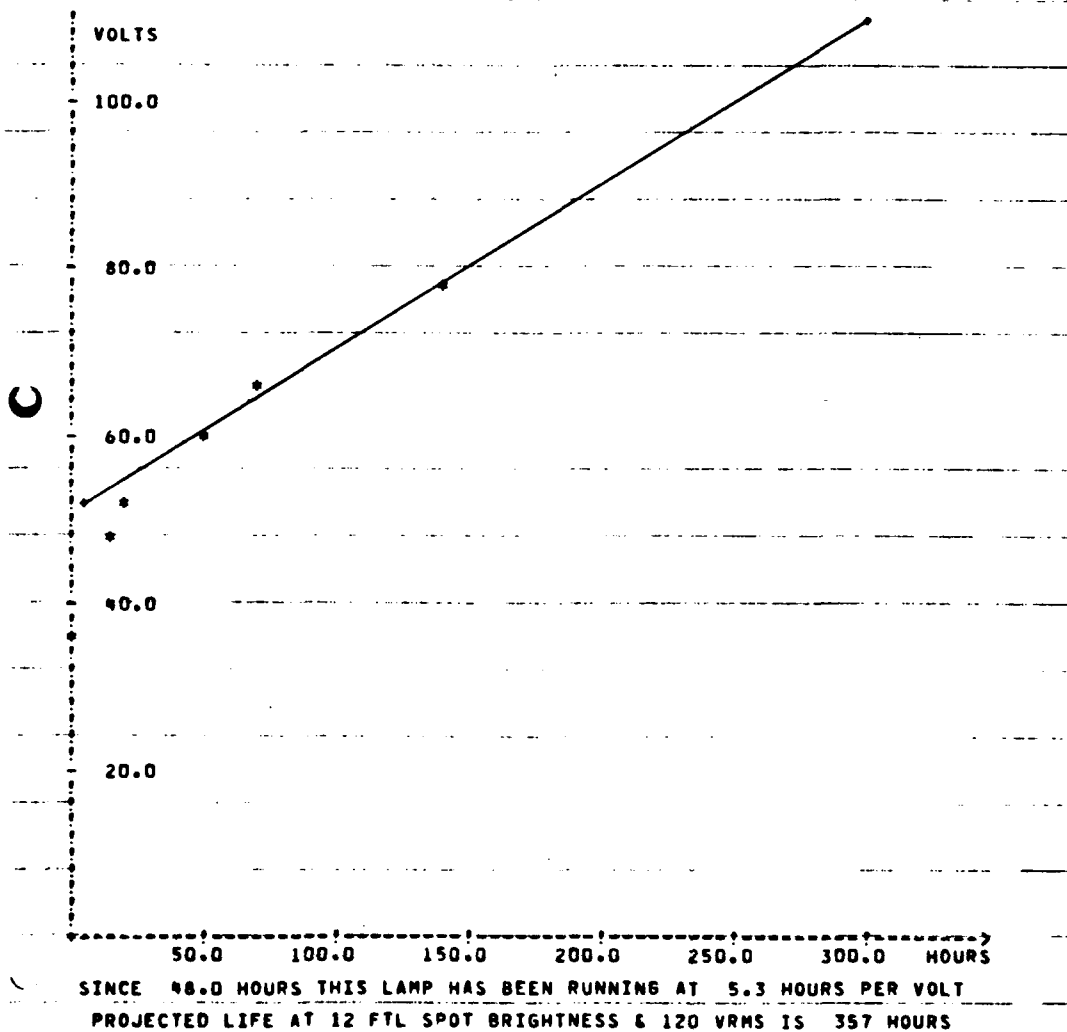


Figure 7.30 Computer analysis of life testing data for postage stamp Sample No. 576-4 participating in Experiment 3 on 72°C phosphor life in vacuum and listed in Table 7.3.

UPDATE 1-12-79

SAMPLE NUMBER 576-5  
SAMPLE TYPE POST STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6

SEE 576-2  
THIS S.  
LEAD OXIDE  
JUST TESTING

FIGURING BOOK REFERENCE NONE  
DATE FABRICATED SEE STEVE  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .43  
TOP COAT 1 .06  
TOP COAT 2 .19  
PHOSPHOR WEIGHT 4.16  
SHEET RESISTANCE 90 OHM

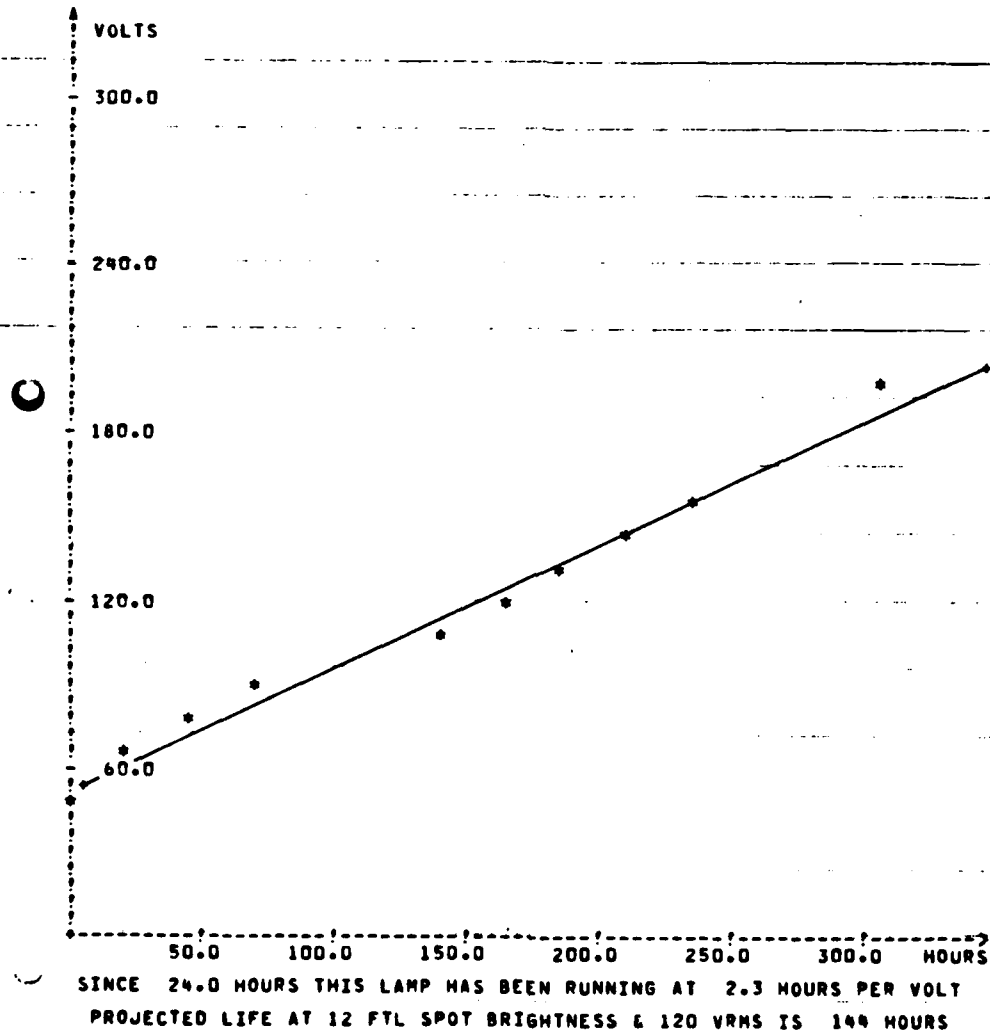


Figure 7.31

Computer analysis of life testing data for postage stamp  
Sample No. 576-5 participating in Experiment 4 on 72°C  
phosphor life in vacuum and listed in Table 7.3.



UPDATE 1-23-79

SAMPLE NUMBER 576-6  
SAMPLE TYPE POST STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6

SAME AS 576-6\*

FIGURING BOOK REFERENCE NONE YET  
DATE FABRICATED STEVE KNOWS  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .42  
TOP COAT 1 .08  
TOP COAT 2 .16  
PHOSPHOR WEIGHT 4.56  
SHEET RESISTANCE 82 OHM

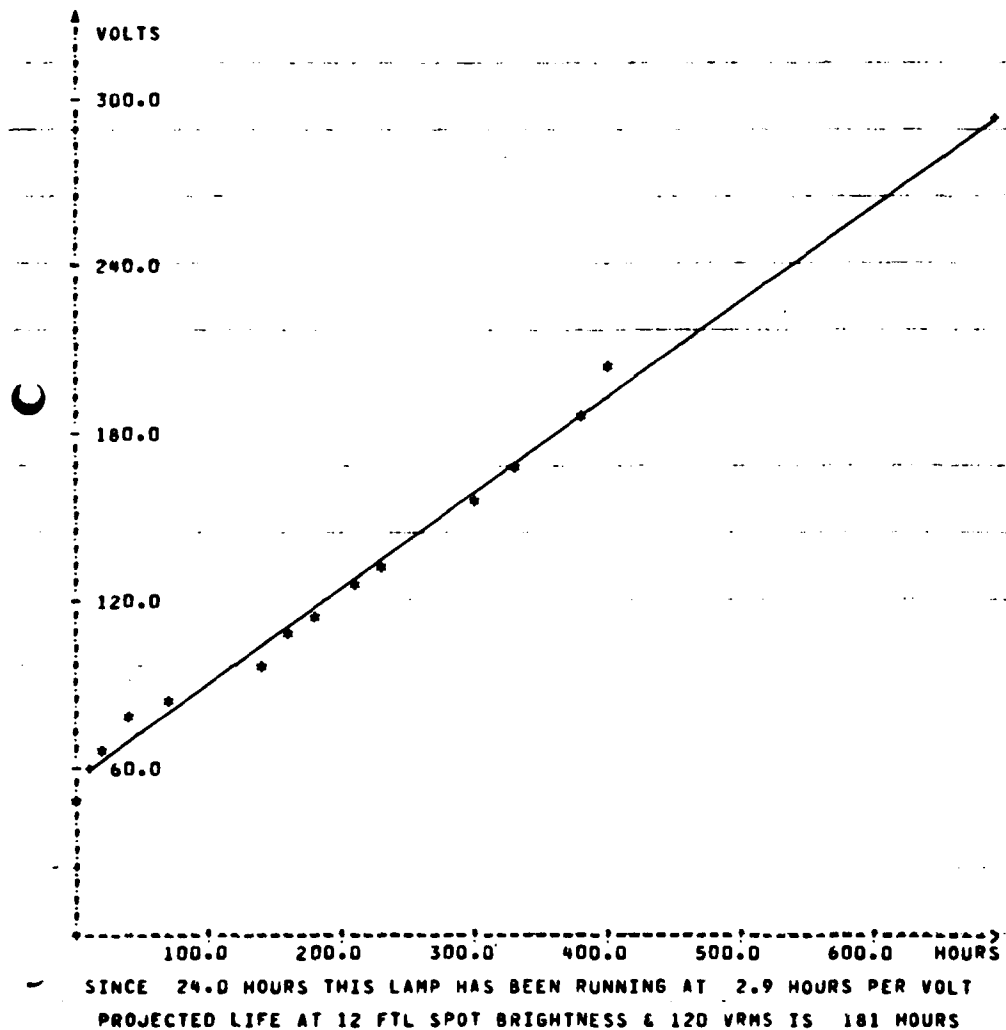


Figure 7.32

Computer analysis of life testing data for postage stamp  
Sample No. 576-6 participating in Experiment 4 on 72°C  
phosphor life in vacuum and listed in Table 7.3.

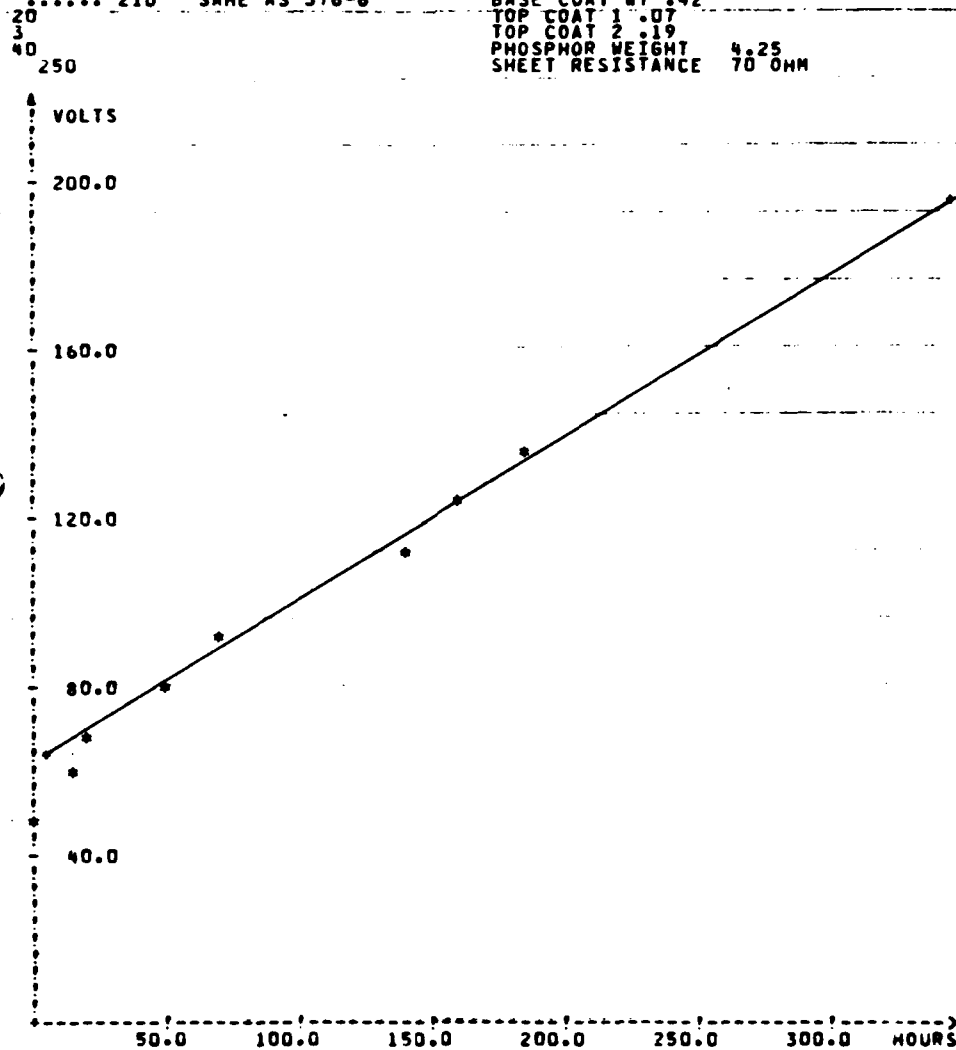
UPDATE 1-12-79

SAMPLE NUMBER 576-7  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 1  
BRIGHTNESS 12

FIGURING BOOK REFERENCE NONE YET  
DATE FABRICATED ASK STEVE  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

..... 210 SAME AS 576-6

BASE COAT WT .42  
TOP COAT 1 .07  
TOP COAT 2 .19  
PHOSPHOR WEIGHT 4.25  
SHEET RESISTANCE 70 OHM



SINCE 48.0 HOURS THIS LAMP HAS BEEN RUNNING AT 2.6 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 146 HOURS

Figure 7.33

Computer analysis of life testing data for postage stamp  
Sample No. 576-7 participating in Experiment 4 on 72°C  
phosphor life in vacuum and listed in Table 7.3.

UPDATE 1-12-79

SAMPLE NUMBER 576-8	FIGURING BOOK REFERENCE	NONE
SAMPLE TYPE STAMP WITH NO RISTON	DATE FABRICATED	NOT PRESENTLY KNOWN
OVEN NUMBER NOT SPECIFIED	TEST AMBIENT	VACUUM
BRIGHTNESS 16	TEST TEMPERATURE	72 DEG CENTIGRADE

THIS IS A PB-O STANDARD	BASE COAT WT	0.44
IDEA IS TO COMPARE	TOP COAT 1	.1
PERFORMANCE WITH CD.F2	TOP COAT 2	.19
OTHER SAMPLES IN SAME OVEN ARE	PHOSPHOR WEIGHT	5.05
576-1 THRU -7	SHEET RESISTANCE	75 OHM

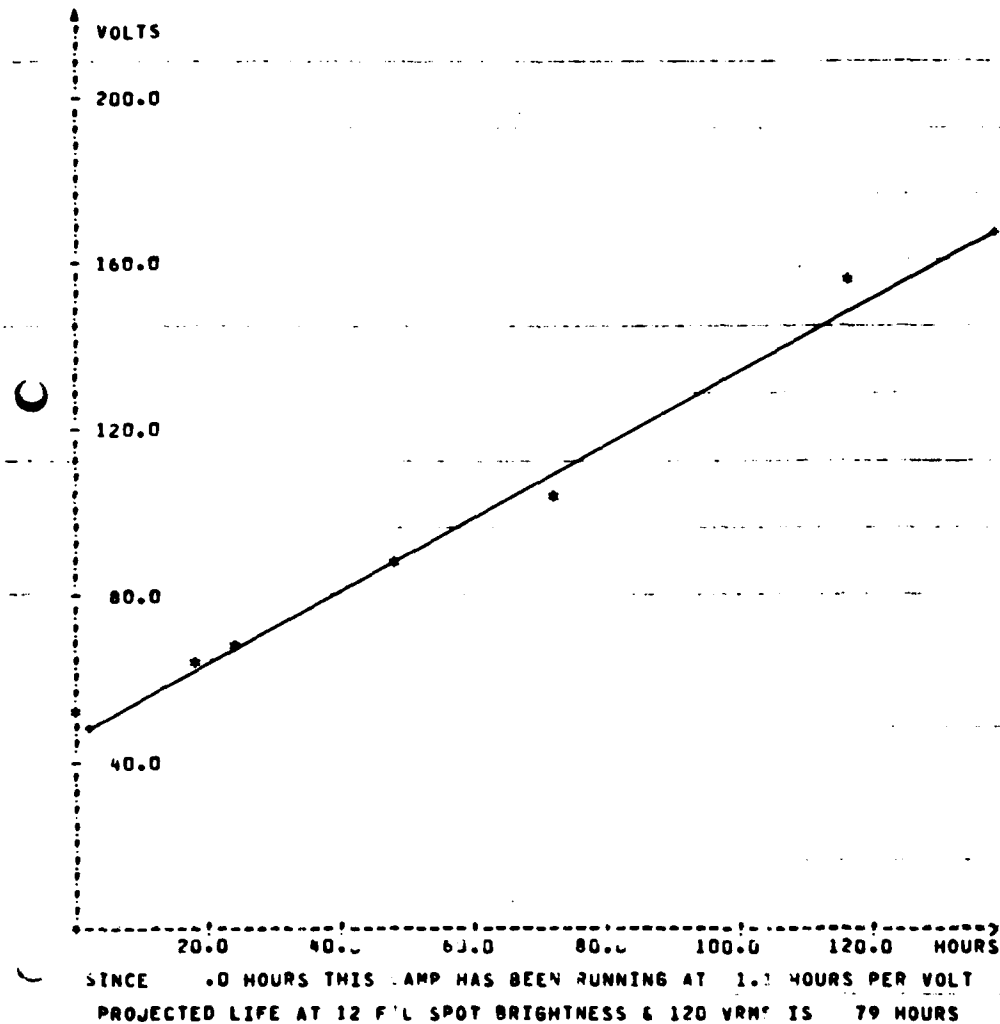


Figure 7.34

Computer analysis of life testing data for postage stamp Sample No. 576-8 participating in Experiment 4 on 72°C phosphor life in vacuum and listed in Table 7.3.

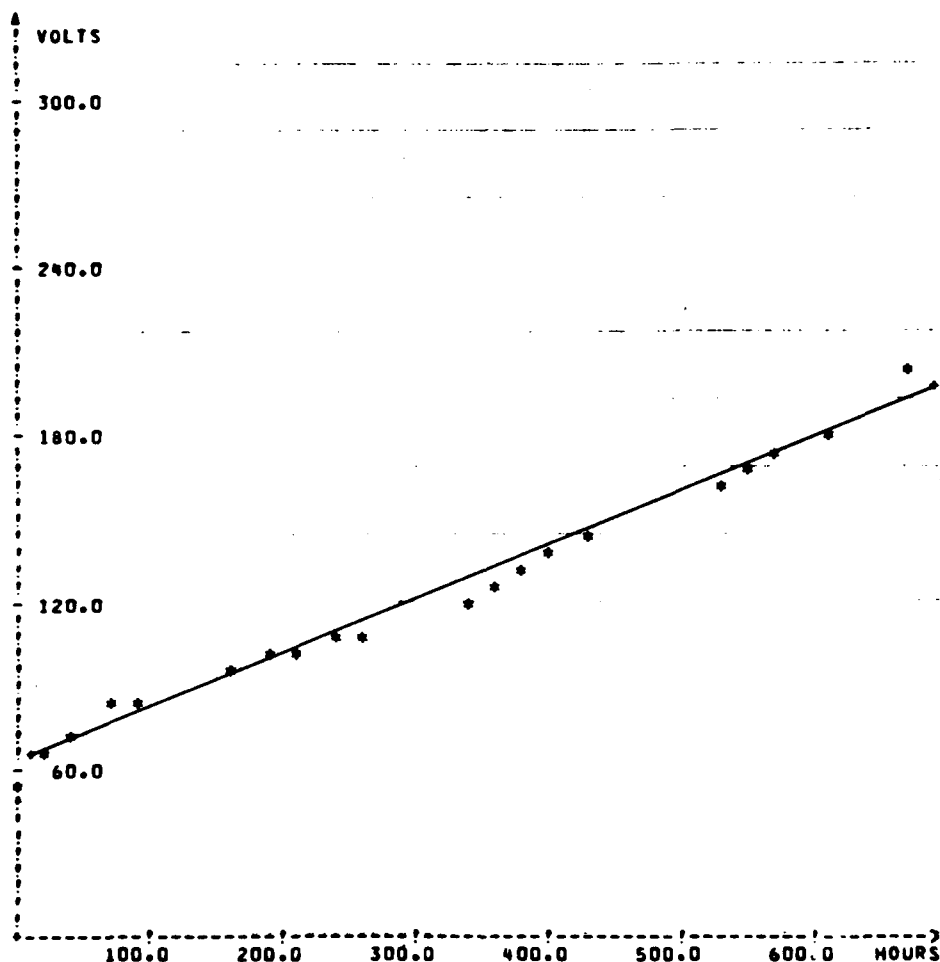
UPDATE 3-1-79

SAMPLE NUMBER 577-1  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6 FL

FIGURING BOOK REFERENCE NA  
DATE FABRICATED 1-10,11-79  
TEST AMBIENT VAC  
TEST TEMPERATURE 72C

NEW SOURCE:  
CAD FLUORIDE  
SAME AS 577-2  
CONTROL SAMPLE FOR:  
577-3 & 577-4

BASE COAT WT .44  
TOP COAT 1 .22  
TOP COAT 2 .34  
PHOSPHOR WEIGHT 4.23  
SHEET RESISTANCE 36



SINCE 24.0 HOURS THIS LAMP HAS BEEN RUNNING AT 5.2 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 283 HOURS

Figure 7.35

Computer analysis of life testing data for postage stamp  
Sample No. 577-1 participating in Experiment 5 on 72°C  
phosphor life in vacuum and listed in Table 7.3.

UPDATE 3-1-79

SAMPLE NUMBER 577-2  
 SAMPLE TYPE POSTAGE STAMP  
 OVEN NUMBER 1  
 BRIGHTNESS 3.6 FL

SAME AS 577-1\*

FIGURING BOOK REFERENCE NA  
 DATE FABRICATED 1-10,11-79  
 TEST AMBIENT VAC  
 TEST TEMPERATURE 72C

BASE COAT WT .46  
 TOP COAT 1 .18  
 TOP COAT 2 .33  
 PHOSPHOR WEIGHT 4.44  
 SHEET RESISTANCE 45

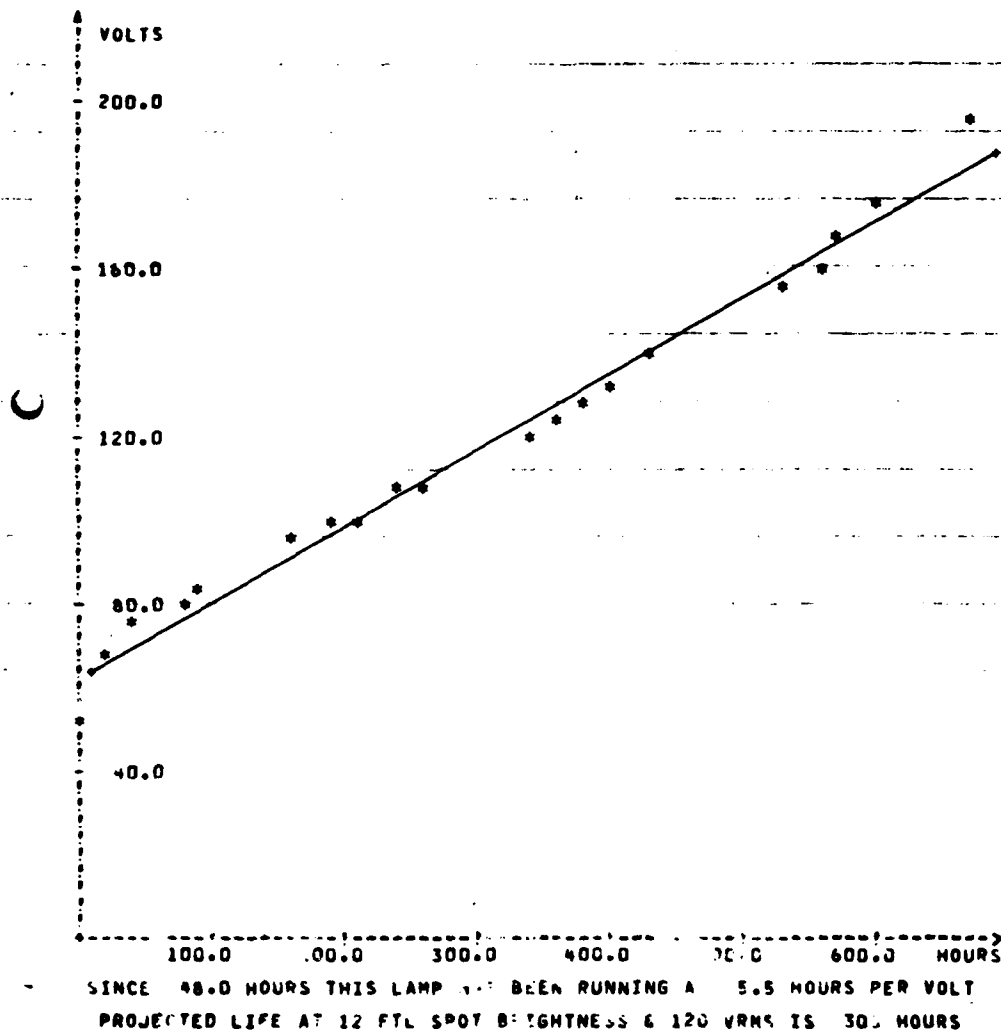


Figure 7.36

Computer analysis of life testing data for postage stamp Sample No. 577-2 participating in Experiment 5 on 72°C phosphor life in vacuum and listed in Table 7.3.

UPDATE 5-7-79

SAMPLE NUMBER	589-2	FIGURING BOOK REFERENCE	NA
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	4-16-79
OVEN NUMBER	3	TEST AMBIENT	VAC
BRIGHTNESS	3.6	TEST TEMPERATURE	72C
SAME AS 589-1		BASE COAT WT	.64
TESTED AT 5KHZ		TOP COAT 1	.21
SINE - VACUUM		TOP COAT 2	.23
72C - SHOULD GET		PHOSPHOR WEIGHT	4.02
		SHEET RESISTANCE	150

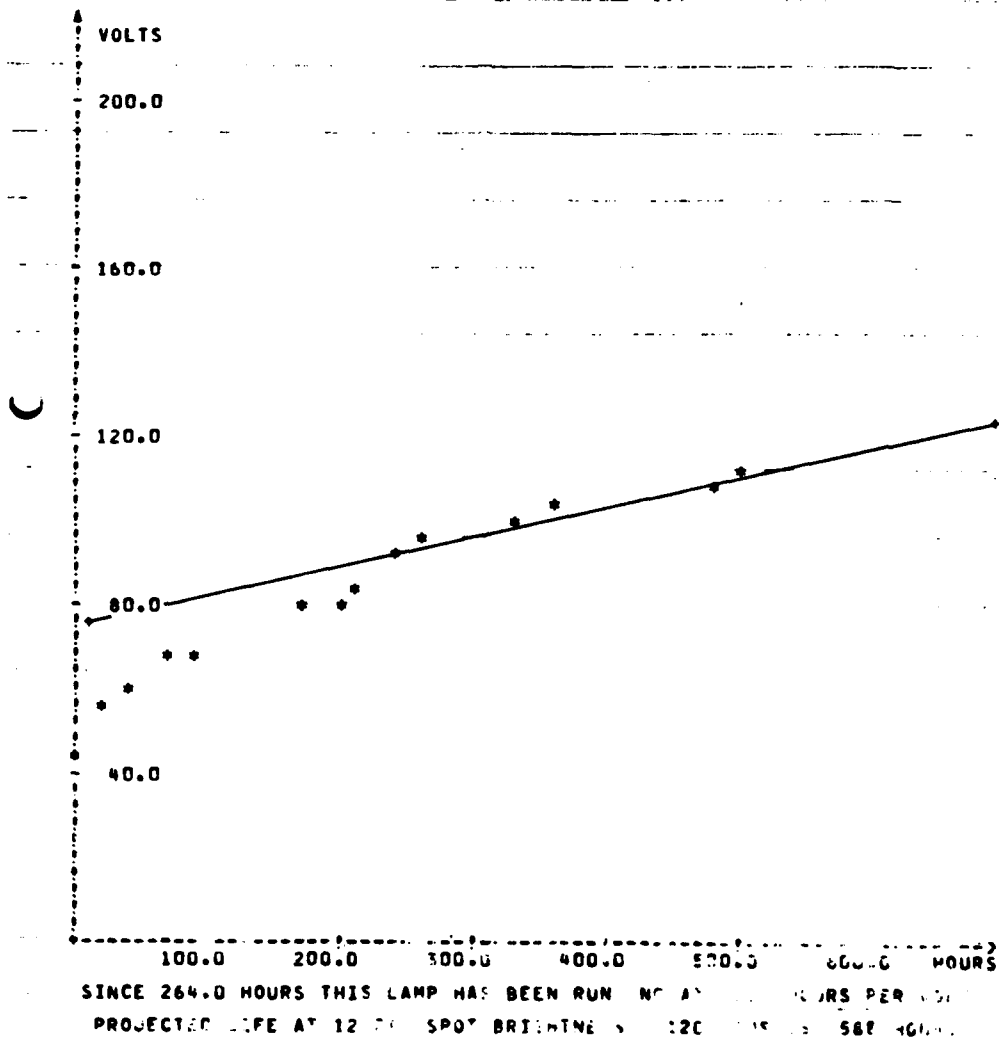


Figure 7.37

Computer analysis of life testing data for postage stamp Sample No. 589-2 participating in Experiment 6 on 72°C phosphor life in vacuum and listed in Table 7.3.

what would be provided by the excitation voltage source. Values are listed here to provide a measure of the authenticity of the test, since in cases of premature lamp failure, caused by effects other than phosphor degradation, maintenance has to be projected.

A first analysis relating to earlier discussion in Section 7.4.6 concerns the relationship of threshold voltage  $V_T$  to maintenance  $M$  of the samples listed in Table 7.3. This is depicted in Figure 7.38 for three classifications of the samples shown. The plot symbols in this and the next several figures have been tabulated in Column 4 of Table 7.3 for ready cross reference. The results fairly convincingly show that, all other things being equal, lower threshold voltage portends superior maintenance. At one time, in fact, we were thinking of using this relationship to expedite life testing measurements which typically took three to five weeks to complete.

Even within the framework of a given plastic binder, phosphor weight, and identical fabrication procedures, the operator finds it difficult to rigidly control the total weight (or corresponding thickness) of the binder. However, this has nonetheless provided us with an opportunity to investigate how maintenance and threshold voltage appear to vary with the plastic thickness. In Figure 7.39 threshold voltage is observed to increase fairly consistently with total binder thickness, as one might expect. Interestingly, the cadmium fluoride samples provide almost universally lower threshold voltage. One could argue that the proximity of the lead oxide to the phosphor grains already have deleterious consequences by the time lamp fabrication procedures and initial burn-in are complete.

The relationship between plastic thickness and maintenance is not quite as clear. To a certain extent, the lead oxide samples exhibit an anticipated enhancement of maintenance for thinner layers of plastic. There is virtually a flat relationship for the samples. Experiments 3 and 5, with cadmium fluoride, unless one includes the samples of Experiment 6, as shown in Figure 7.40. The exact casual relationships, if any, are not clear, however.

Curve 720667-A

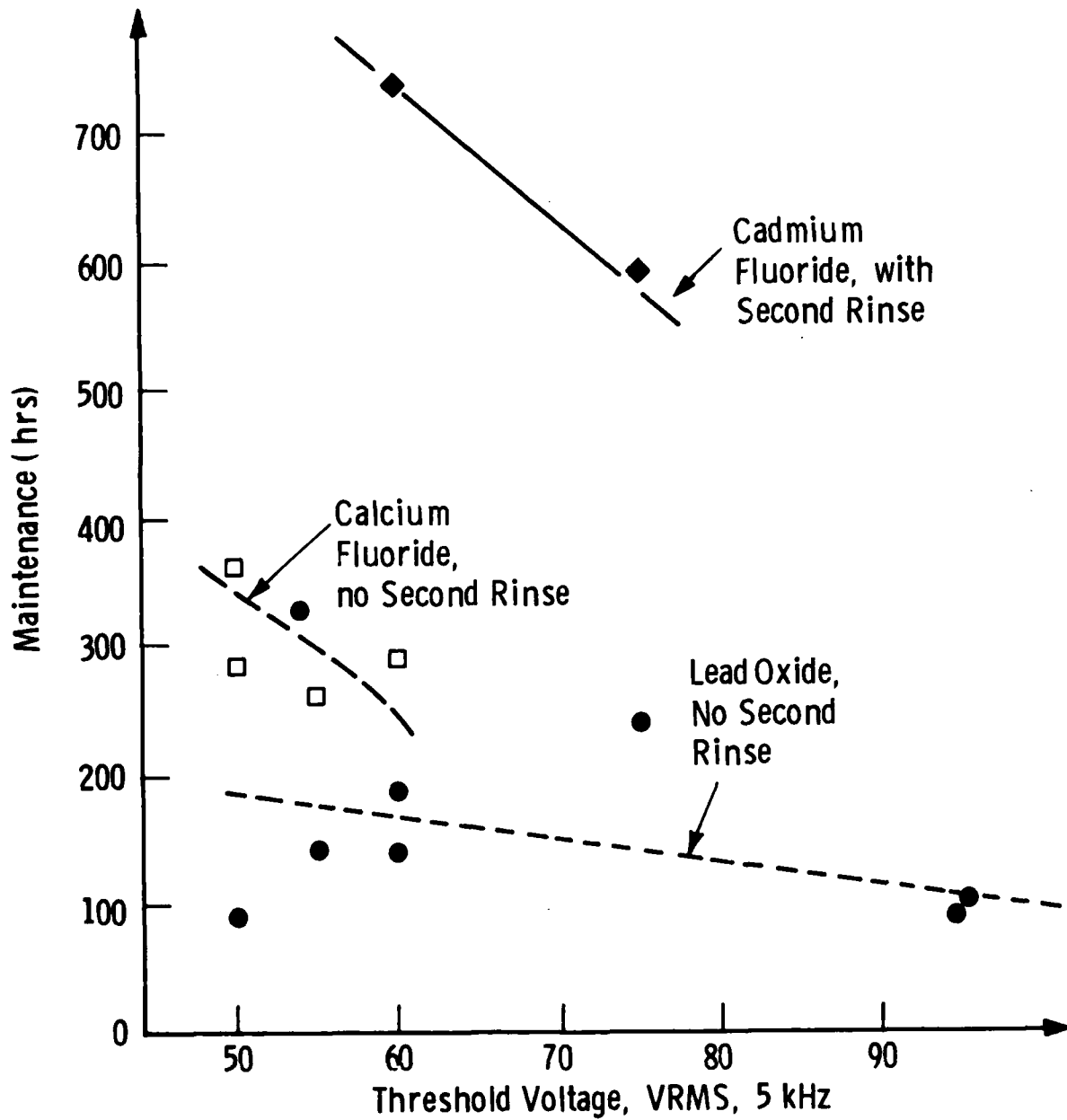


Figure 7.38

Behavior of 72°C maintenance versus initial threshold voltage for three sample classifications shown in Table 7.3 during in-vacuum life testing.



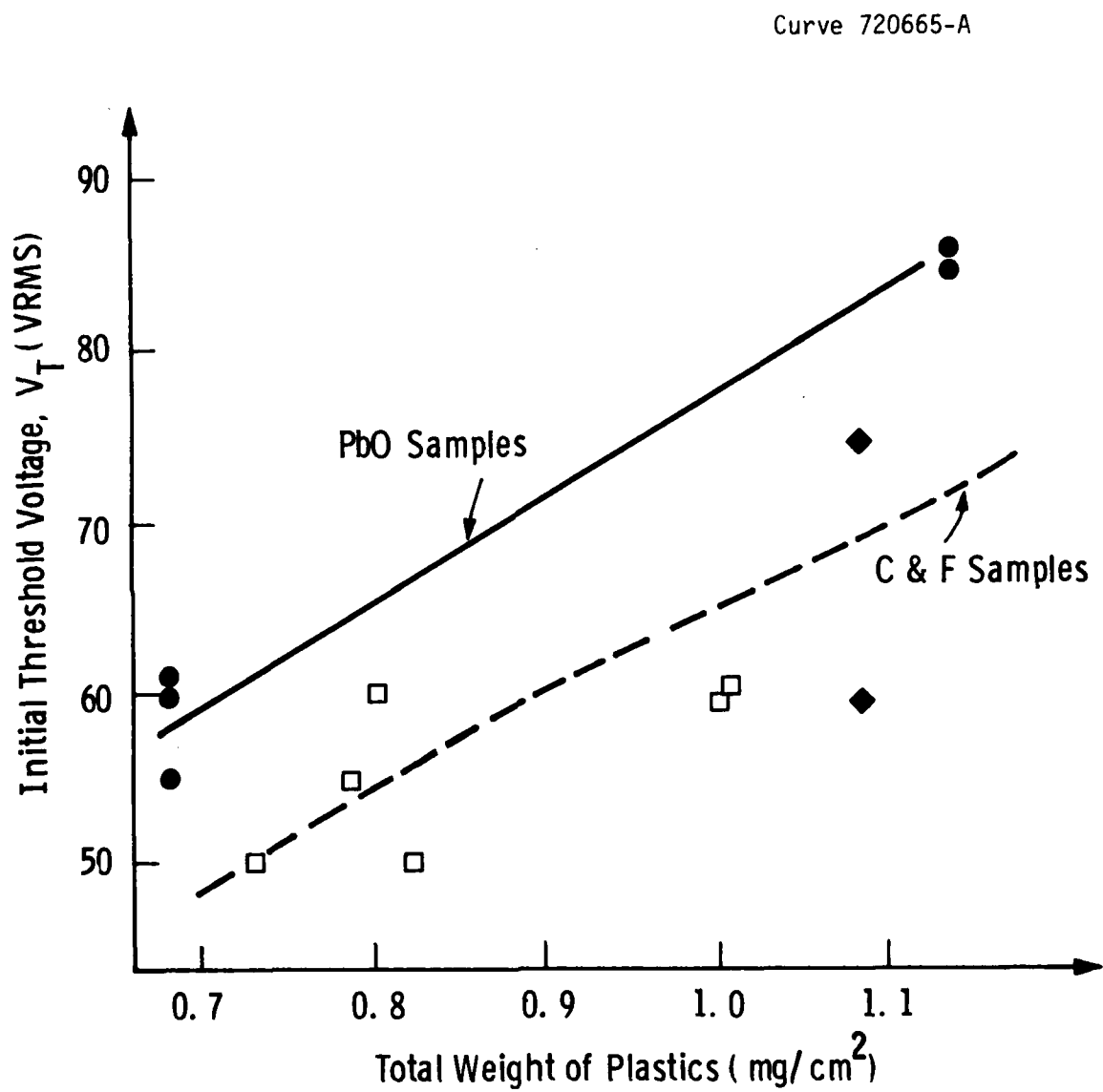


Figure 7.39

72°C initial threshold voltage versus total plastic thickness for three sample classifications shown in Table 7.3.

Curve 720671-A

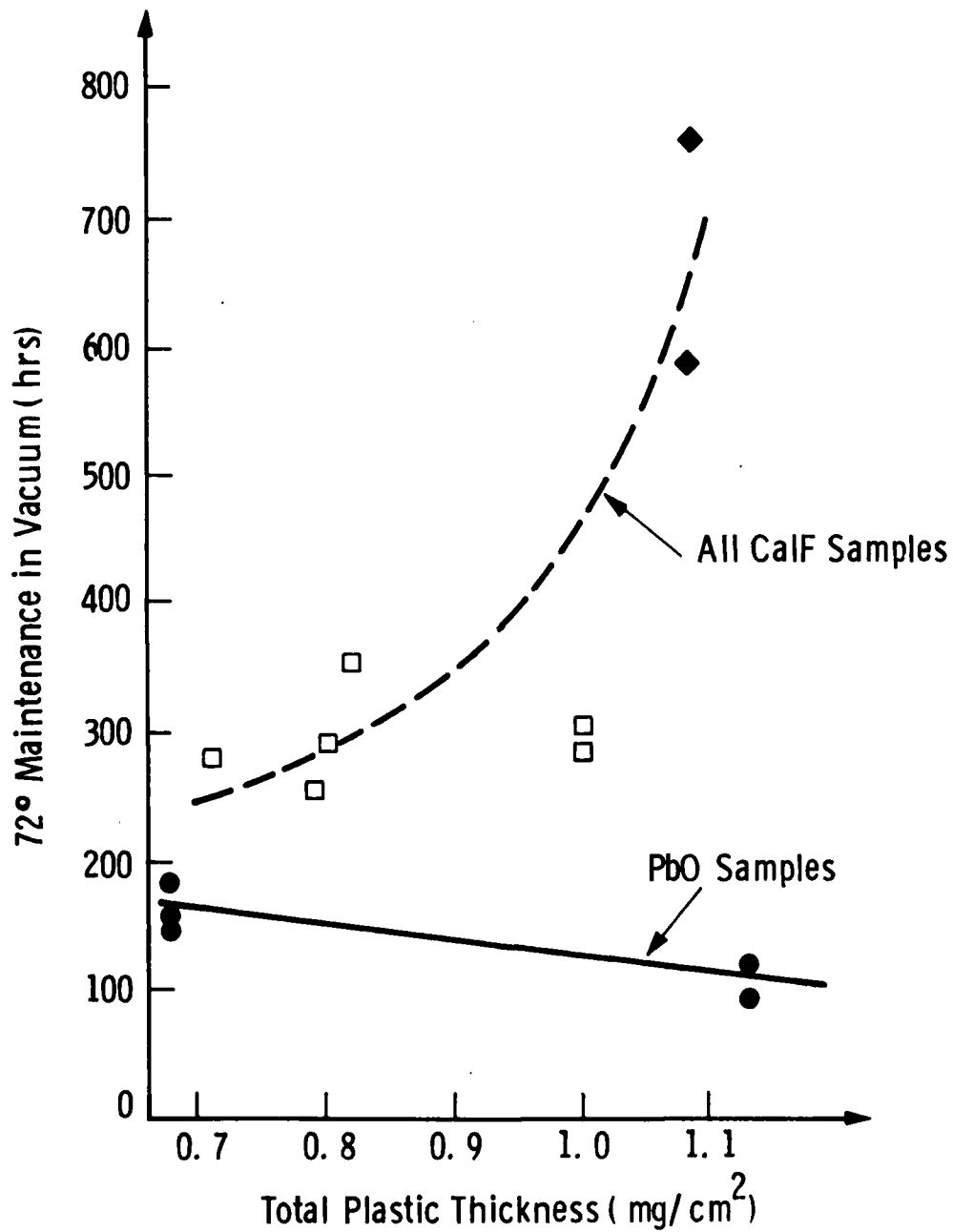


Figure 7.40

Observed variation of maintenance at 72°C in vacuum for three classifications of samples shown in Table 7.3.

Another hard-to-control processing parameter is top electrode sheet resistivity and this too bears some brief analysis. For example, one could argue that the higher the sheet resistivity, the more transparent is and consequently less voltage is required to generate a given brightness after passage through the electrode. Conversely, one could also argue that disproportionate voltage drops are sustained across the layer laterally at the same time, thereby promoting not only its own self-destruction by heating, but also nonuniform excitation of the phosphor. The results tend to confirm the resulting confusion concerning optimality, particularly regarding threshold voltage, as shown in Figure 7.41. However, in the case of maintenance versus sheet resistivity, which after all is the key parameter from a display performance viewpoint, there certainly seems to exist a definite inverse relationship between maintenance and sheet resistivity of the top electrode, as indicated in Figure 7.42. This implies that indeed excessive resistivity of the top electrode, regardless of its better transmissivity, leads to early death.

In summary, our process development activity in connection with the fundamental ability of the phosphor to sustain emission at 72°C for 500 hours within the scope of voltage ratcheting has led to the following overall results and conclusions:

1) In excess of the required, maintenance has been demonstrated commensurate with 12 ft-L emission (adequate for 2000 ft-C readability), as indicated by samples 589-1 and -2 in Table 7.3.

2) Key factors in reaching this goal have been

- A. Development of a cyano ethylated, isocyanated polyvinyl alcohol binder.
- B. Development of a hybrid brush-spray approach to the phosphor layer synthesis.
- C. Substitution of cadmium fluoride for lead oxide as the top electrode base.
- D. Extra care to remove residual photoresist scan from the lower electrode when the field isolation layer of Riston is processed and, of course,

Curve 720669-A

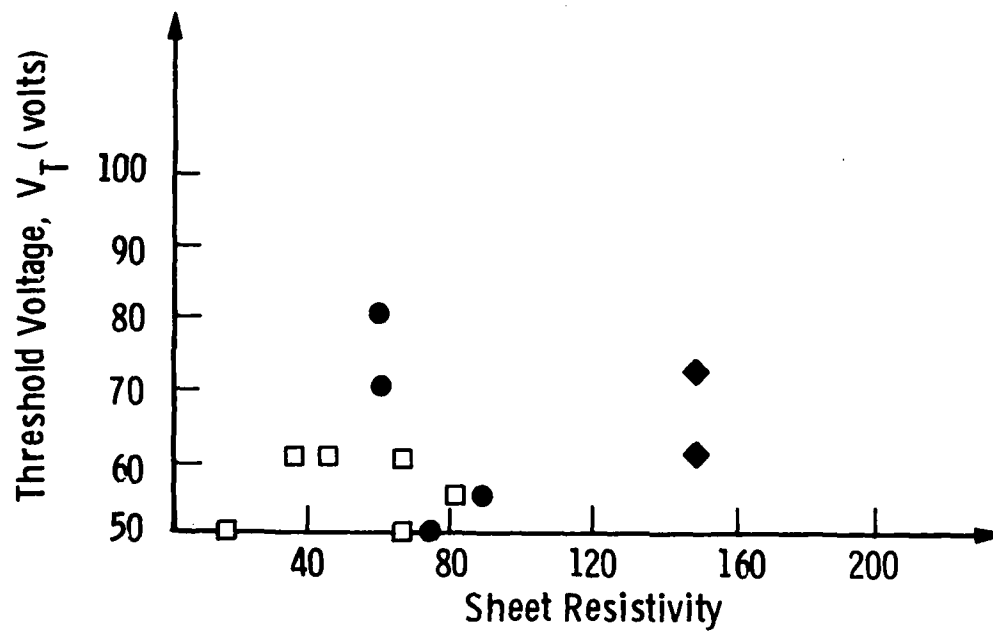


Figure 7.41 Variation of threshold voltage with top electrode sheet resistivity (Refer to Table 7.3).

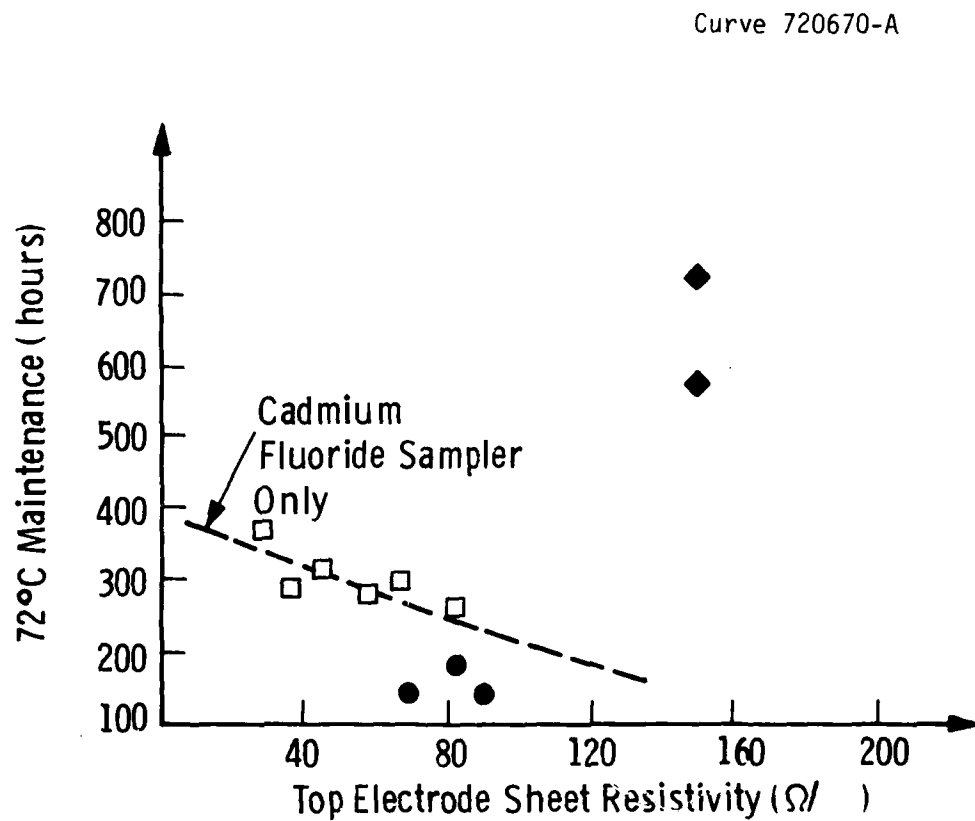


Figure 7.42 Variation of maintenance with top electrode sheet resistivity (Refer to Table 7.3).

E. Continued and reliable supply of the Westinghouse high maintenance powder phosphor from internal sources.

3) All other things being equal (as possible), higher maintenance is predetermined by lower threshold voltage.

4) Decreasing threshold voltage with binder thickness.

5) Higher maintenance with decreasing top electrode sheet resistivity.

The results and conclusions listed above were obtained under a deliberate strategy to determine whether the phosphor per se was up to the task demanded by display specifications. The next task was to determine whether commensurate performance would be derived in more demanding circumstances involving the proximity of encapsulating materials and exposure to unfriendly ambients. Development along these lines is discussed in the next section.

TABLE 7.3 Results of a Selection of Experiments Evaluating  
Intrinsic Phosphor Life in Vacuum at 72°C

Postage Stamp No.	Description of Experiment	Plot Symbol	EXPERIMENTAL DETAILS				RESULTS					
			Clear Coat Weights mg (cm <sup>2</sup> )			Phos-Weight mg (cm <sup>2</sup> )	Top Electrode Sheet Resis. $\Omega/\square$	Inverse Degradation (hrs/V)	Main-tenance M (hrs)	Threshold Voltage V <sub>T</sub> (volts)	Duration of Test (hrs)	
			Bottom	Top 1	Top 2							
												Total
570-2	First quantitative encapsulation test See Table 7.4.	•	--	--	--	--	--	6.0	272	75	600	
574-2		•	--	--	--	--	--	--	5.2	324	55	600
575-1	Revised quantitative encapsulation test See Table 7.5	•	0.45	0.22	0.46	1.13	--	--	4.3	118	95	350
575-6		•	0.45	0.22	0.46	1.13	--	--	3.7	95	95	160
576-1	New top electrode formulation (CdF)	+	0.38	0.12	0.29	0.79	4.2	82	3.8	256	55	500
576-2		+	0.38	0.11	0.24	0.73	4.4	58	4.1	280	50	500
576-3		+	0.42	0.10	0.28	0.80	4.4	66	4.7	289	60	500
576-4		+	0.43	0.11	0.28	0.82	4.04	28	5.3	357	50	140
576-5	Existing top electrode formulation (PbO)	o	0.43	0.06	0.19	0.68	4.2	90	2.3	144	55	300
576-6		o	0.42	0.08	0.16	0.66	4.6	82	2.9	181	60	400
576-7		o	0.42	0.07	0.19	0.68	4.25	70	2.6	146	60	200
576-8		o	1.44 ?	0.10	0.19	1.73	5.05	75	1.1	79	50	110
577-1	Confirmation of new top electrode process (CdF)	+	0.44	0.22	0.34	1.00	4.23	36	5.2	283	60	650
577-2		+	0.46	0.18	0.33	1.00	4.4	45	5.5	303	60	700
589-1	Revised isolation layer developing	◆	0.64	0.21	0.23	1.08	4.0	150	12.2	743	60	850
589-2		◆	0.64	0.21	0.23	1.08	4.0	150	13.8	588	75	500

### 7.5.2 Encapsulated Phosphor Life Testing at 72°C

We have shown in the previous subsection how a technology for fabrication of the phosphor layer, consisting of patterned isolation Riston, a plastic binder, the powder phosphor and a top electrode, was developed to meet a 500-hr maintenance requirement at 72°C, as specified by the program. This was one separable facet of the technical strategy presented in Section 7.3. The next and final task, to be described here, was to take the phosphor layer technology we had so developed and to find techniques whereby it could be encapsulated for protection from the ambient. In practice, the two separable approaches, phosphor layer development and its subsequent encapsulation, were undertaken somewhat in parallel, partly because of limited time, but partly, as we discovered, the materials used in encapsulation, like the binder, also affect performance with respect to 72°C maintenance.

In previous Sections 2.3 and 3.4 we have reviewed aspects of the encapsulation procedure practiced during program Phase II, which had historically been used at Westinghouse in the fabrication of thin film transistor displays. The new factor we had to address in program Phase III was the demonstration of maintenance at 72°C, as opposed to traditional testing which had only ever been executed at room temperature. The events which precipitated all the activity being described here were the tests referred to previously. The so-called ON-OFF Tester, described in Section 9.4, was used late in program Phase II to evaluate the performance of the then existing encapsulation and phosphor layer synthesis techniques, using an actual panel fabricated to meet the confirmatory sample requirement.

All elements of the panel were turned on and off in a 30-second cycle while the panel was mounted in a 72°C oven with an air ambient. The excitation voltage was set at 150 volts peak-to-peak. The average starting brightness of the phosphor elements was 10 ft-L. After 4 hours at 72°C, the average brightness decreased to 10% of the original level. In the ON state the panel elements were barely visible in normal room lighting. Subsequently, postage stamp test vehicles were



encapsulated with different candidate materials and used to provide further preliminary simulation of display behavior in a 72°C air ambient.

Figure 7.43 shows test results of several samples. Sample #1, with a Stycast epoxy encapsulant, decreased in brightness by a factor of 9 in 2 hours at 72°C. The materials and processing used to prepare this sample were the same as those used to fabricate the confirmatory sample subjected to ON-OFF testing described above. The rapid decreases in brightness are commensurate. Samples #2 and #3 were encapsulated with a specially formulated epoxy (#332) and a GE silicone, Sample #3 with the silicone encapsulant was significantly more stable. Sample #4 had no encapsulant and was tested in a vacuum oven and exhibited the best maintenance characteristics. The phosphor layers of all samples were prepared with the old sprayed CE:S&S technique described in Section 7.2 and we now know that both the phosphor layer synthesis and the encapsulation techniques were contributing to the very discouraging results. However, at that time it was concluded that moisture was being trapped in, or otherwise being admitted to, the sealed assembly, consistent with later conclusions.

Further preliminary tests illustrated in Figure 7.44 and conducted at 72°C with postage stamp samples showed that a vacuum bake-out step improved phosphor maintenance by a factor of 2 to 3. This provided important clues to the origin of the overall problem and contributed to final procedure formulations presented in Sections 7.6 and 8.2.

We now begin discussion of how progress in phosphor layer technology, established by 72°C testing in vacuum, was merged with encapsulation development to provide respectable 72°C performance in air.

A first test was performed to determine how existing encapsulation alternatives fared in conjunction with the new hybrid CE:PVA phosphor layer, as opposed to the former spray CE:S&S fabrication technique, already illustrated in Figures 7.43 and 7.44. A batch of postage stamps, with as far as possible identical structures was divided into two groups. One group was tested in air at 72°C and the other in vacuum. The test, like those described in the previous section, was

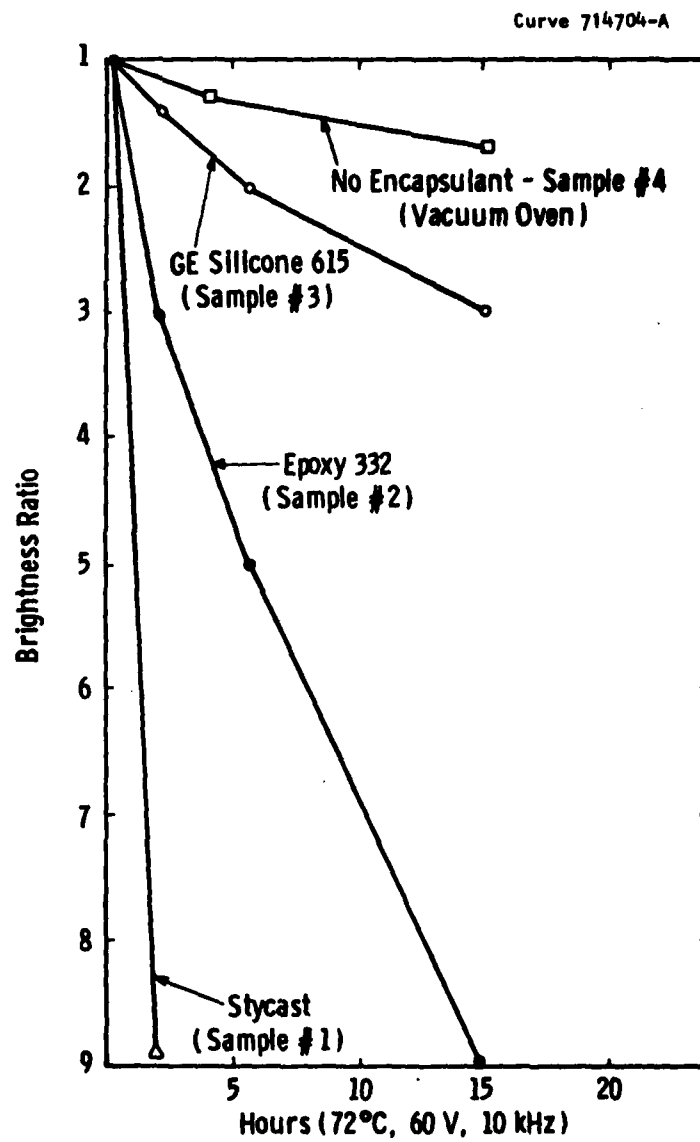


Fig. 7.43 Preliminary Simulation of Display Behavior with Respect to Maintenance at 77°C Using Materials and Techniques as Practiced During Program Phase II.



conducted at a constant 12 fL spot brightness (3.6 fL geometrical average) on postage stamps. The AC voltage was ratcheted as necessary. The sample configurations and test results are shown in Table 7.4. The control samples, 570-2 and 574-2, have been discussed previously in conjunction with the results presented earlier in Table 7.3. These alone were not fitted with a cover glass. All the others simulated fully assembled displays. Unfortunately, no records are available on the binder and phosphor weights and top electrode sheet resistance. However, their effects were almost certainly not consequential in this test. All samples were fabricated with a lead oxide, and not cadmium fluoride, top electrode base. The respective graphical performance analyses for samples 568-6 through 566-3 are shown in Figures 7.45 through 7.52.

With reference to Table 7.4. , the variations in the "results" columns are so gross, the following conclusions can immediately be drawn:

- (1) The proximity of the Stycast encapsulant seems to be inherently hostile towards the phosphor layer system. The somewhat remarkable thing is, however, that the samples with Stycast tested in vacuum (568-6, 568-3) perform even worse than those tested in air (568-7 & 8, and 568-4 & 5). We have no explanation for this.
- (2) The samples without Stycast, but with a polysulfide edge seal, perform respectably in vacuum and only marginally less so in air. This material seems therefore to have little or no incompatibility with the phosphor layer system but, at the same time, not totally capable of preventing ill effects originating in the air ambient. One might venture to argue that un-encapsulated vacuum testing ordinarily removes undesirable reaction products from the phosphor layer system. This beneficial transfer may be impeded somewhat by the presence of the polysulfide edge seal.

Table 7.4 Comparative Performances of the New CE:PVA Binder under Different Conditions of Encapsulation and Exposures to Ambients at 72°C Constituting the First Encapsulation Test.

Sample Number	Figure Number	Configuration		Test Ambient (72°C)	Inverse Rate of Degradation hrs/volt	Results		
		Encapsulant	Edge Seal			Main-tenance hrs. (to 120 vrms)	Thresh-old Voltage vrms	Duration of Test
570-2	7.23	none	none	Vacuum	6.0	272	75	600
574-2	7.24	"	"	"	5.2	324	55	600
568-6	7.45	Stycast	none	Vacuum	0.2	11	60	22
568-3	7.46	Stycast	Polysulfide	Vacuum	<0.2	12	58	22
566-4	7.47	none	Polysulfide	Vacuum	5.3	215	80	560
568-7	7.48	Stycast	none	Air	2.2	82	80	95
568-8	7.49	Stycast	none	Air	1.2	70	59	45
568-4	7.50	Stycast	Polysulfide	Air	.7	41	55	38
568-5	7.51	"	"	"	.6	36	55	39
566-3	7.52	none	Polysulfide	Air	5.4	106	100	510

UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	568-6	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-06-78
OVEN NUMBER	2	TEST AMBIENT	VAC
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C

ENCAP TEST #1	BASE COAT WT	---
STYCAST AND RISTON	TOP COAT 1	---
NO POLYSULFIDE	TOP COAT 2	---
**DID NOT LAST 24 HOURS**	PHOSPHOR WEIGHT	---
	SHEET RESISTANCE	---

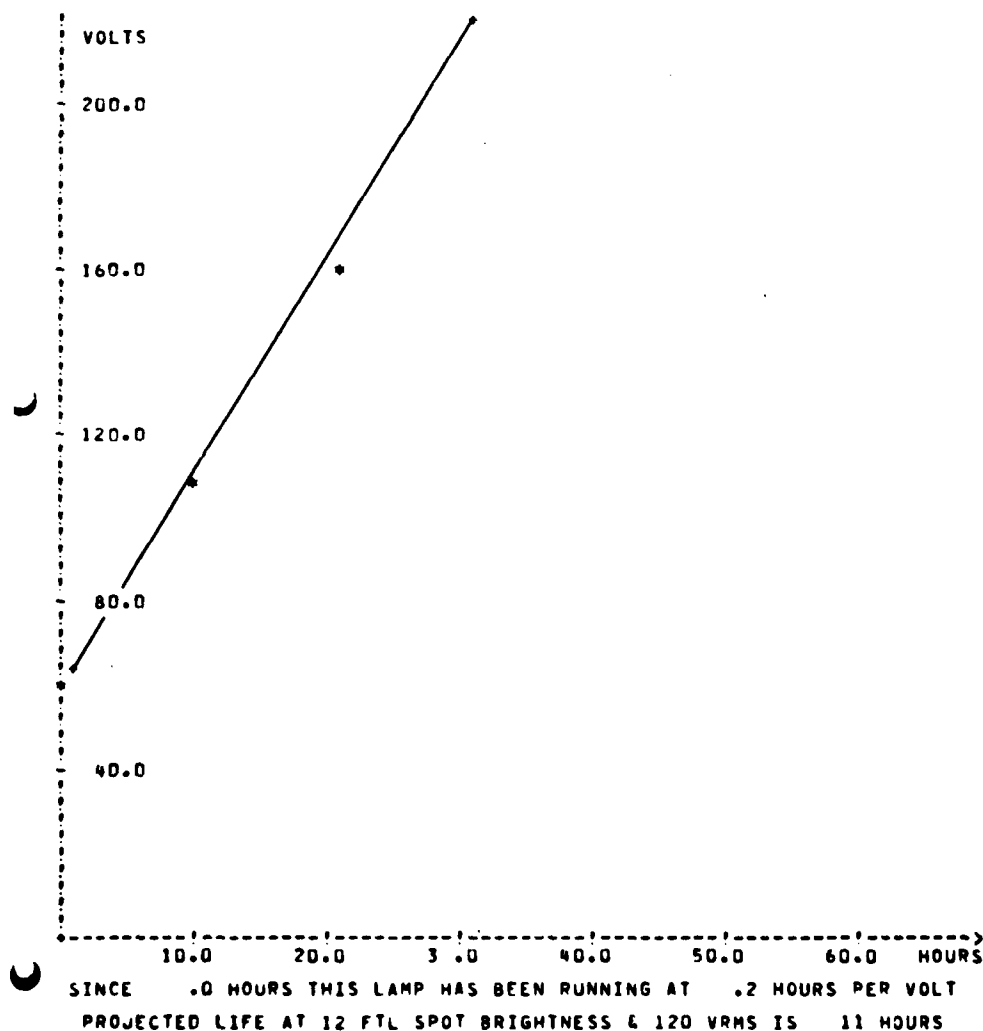


Figure 7.45 Life Testing Analysis of Sample Number 568-6 listed in Table 7.4, constituting the First Encapsulation Experiment. Sample Configuration is Stycast Encapsulant with no Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Vacuum.

UPDATE FEBRUARY 19, 1979

SAMPLE NUMBER	568-3	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-06-78
QVLN NUMBER	2	TEST AMBIENT	VACUUM
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C

ENCAP TEST NO. 1	BASE COAT WT	***
THIS SAMPLE STYCAST	TOP COAT 1	***
AND POLYSULFIDE	TOP COAT 2	***
EDGE SEAL	PHOSPHOR WEIGHT	***
** DID NOT LAST 24 HRS**	SHEET RESISTANCE	***

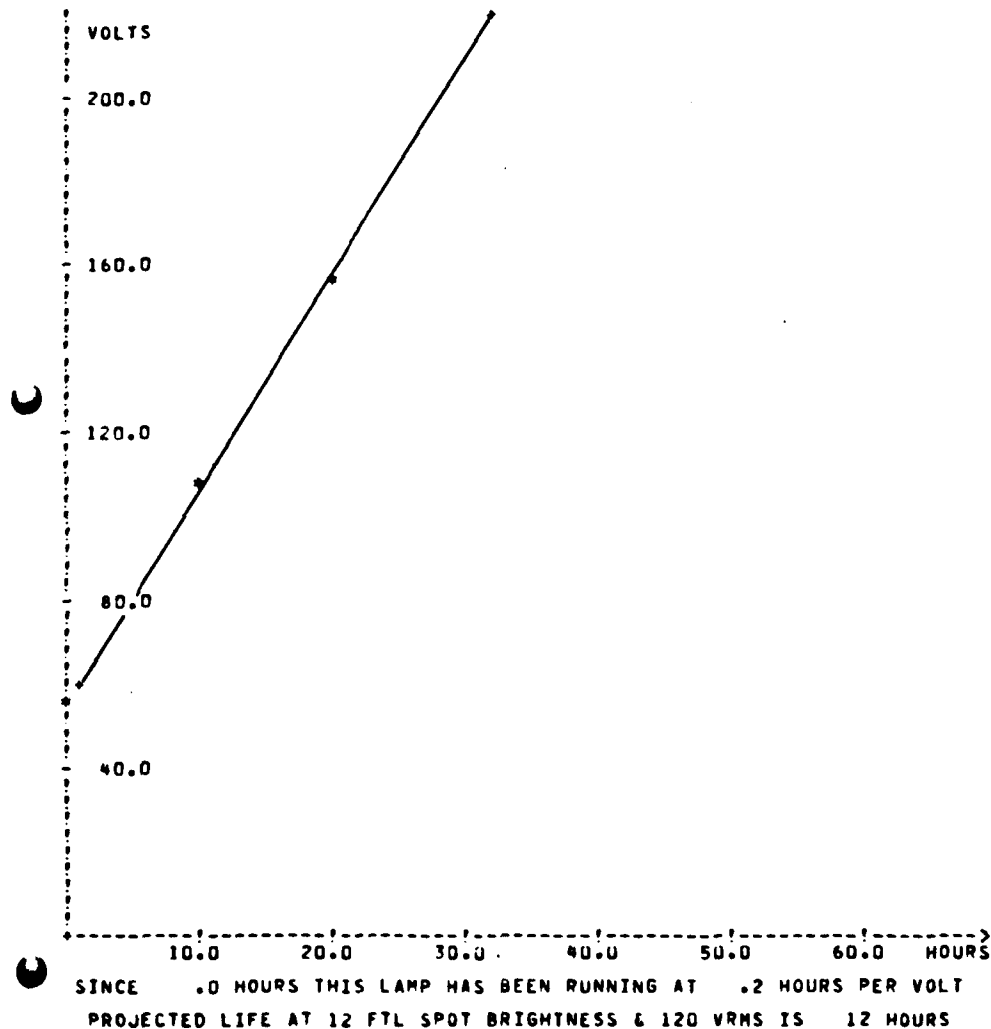


Figure 7.46 Life Testing Analysis of Sample Number 568-3 listed in Table 7.4, constituting the First Encapsulation Experiment. Sample Configuration is Stycast Encapsulant and Polysulfide Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Vacuum.

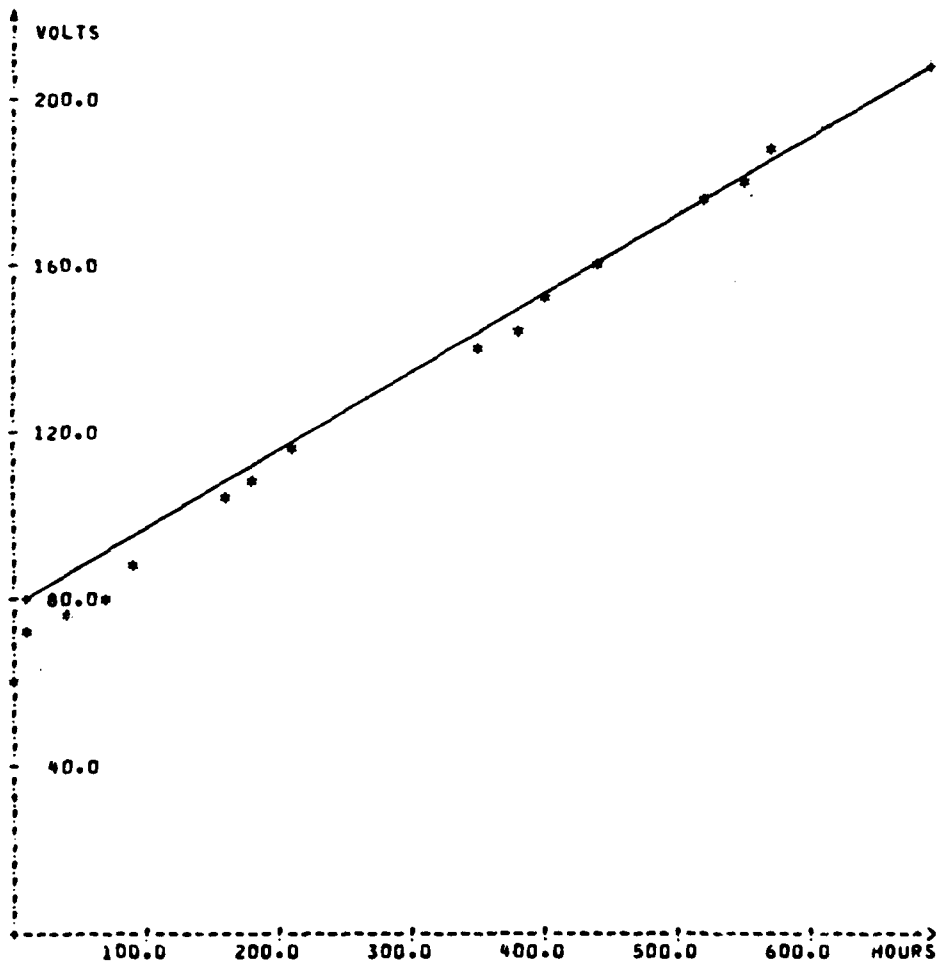
UPDATE FEBRUARY 15, 1979

SAMPLE NUMBER 566-4  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

SAME AS 566-3  
BUT TESTED IN VACUUM

FIGURING BOOK REFERENCE 207951/144  
DATE FABRICATED 11-05-78  
TEST AMBIENT VAC  
TEST TEMPERATURE 72

BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE



SINCE 433.8 HOURS THIS LAMP HAS BEEN RUNNING AT 5.3 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 215 HOURS

Figure 7.47 Life Testing Analysis of Sample Number 566-4 listed in Table 7.4, constituting the First Encapsulation Experiment. Sample Configuration is no Encapsulant and Poly-sulfide Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Vacuum.



UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	568-7	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-07-78
OVEN NUMBER	1	TEST AMBIENT	AIR
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C
ENCAP TEST #1		BASE COAT WT	---
THIS SAMPLE STYCAST		TOP COAT 1	---
AND COVER GLASS - NO		TOP COAT 2	---
EDGE SEAL		PHOSPHOR WEIGHT	---
		SHEET RESISTANCE	---

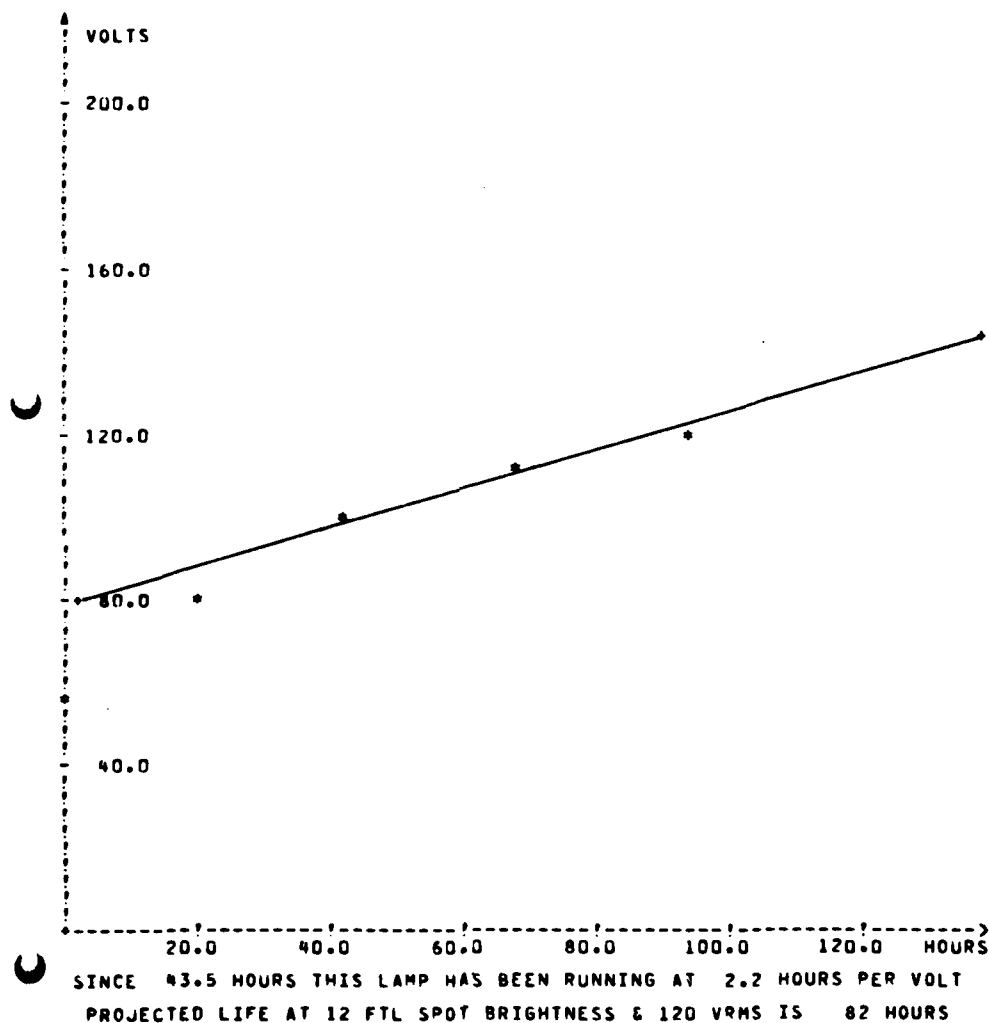


Figure 7.48 Life Testing Analysis of Sample Number 568-7 listed in Table 7.4, Constituting the First Encapsulation Experiment. Sample Configuration is Stycast Encapsulant and no Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Air.

UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	568-8	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	*****
OVEN NUMBER	1	TEST AMBIENT	AIR
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C
SAME AS 568-7		BASE COAT WT	---
BUY		TOP COAT 1	---
ELECTRODE SHORTED		TOP COAT 2	---
AFTER		PHOSPHOR WEIGHT	---
TWO DAYS		SHEET RESISTANCE	---

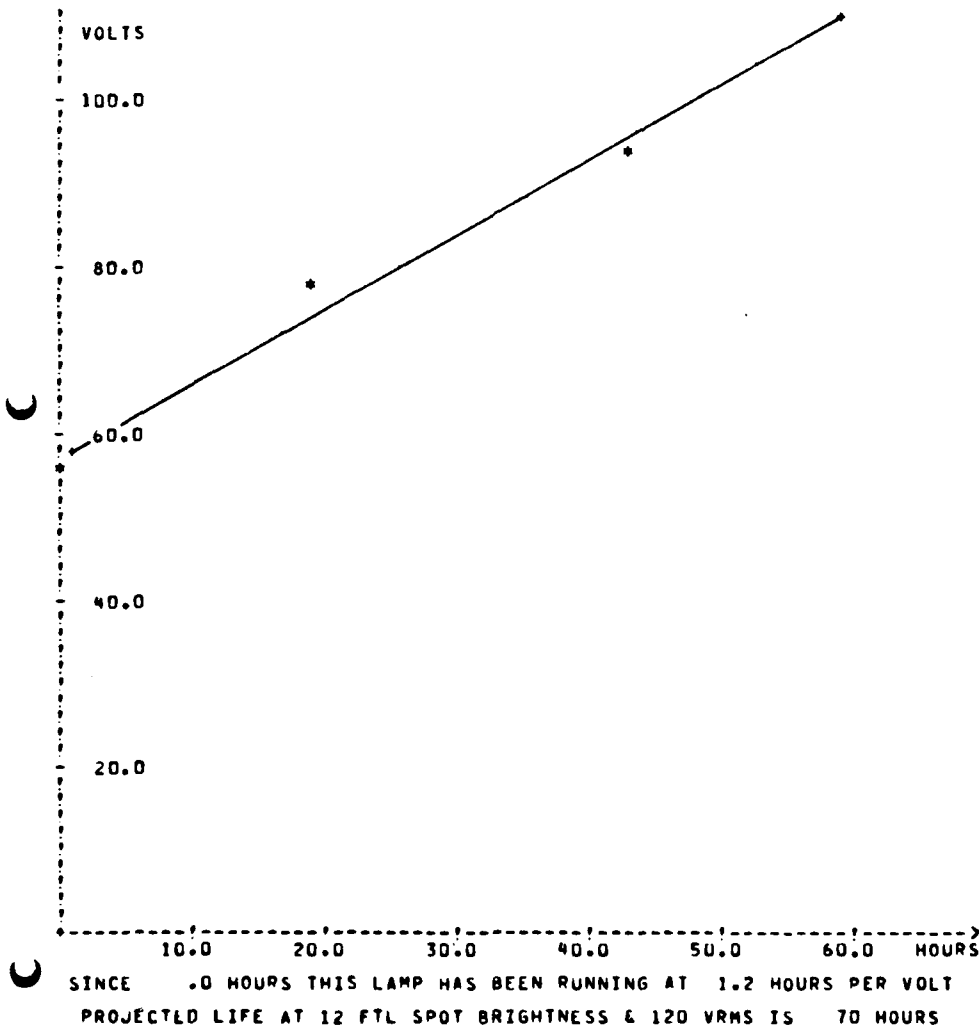


Figure 7.49 Life Testing Analysis of Sample Number 568-8 listed in Table 7.4, Constituting the First Encapsulation Experiment. Sample Configuration is Stycast Encapsulant and no Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Air.

UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	568-4	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-06-78
OVEN NUMBER	1	TEST AMBIENT	AIR
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C
ENCAP TEST #1		BASE COAT WT	---
RISTON, STYCAST		TOP COAT 1	---
E POLYSULFIDE		TOP COAT 2	---
THIRD POINT		PHOSPHOR WEIGHT	---
PAKED LINEAR		SHEET RESISTANCE	---

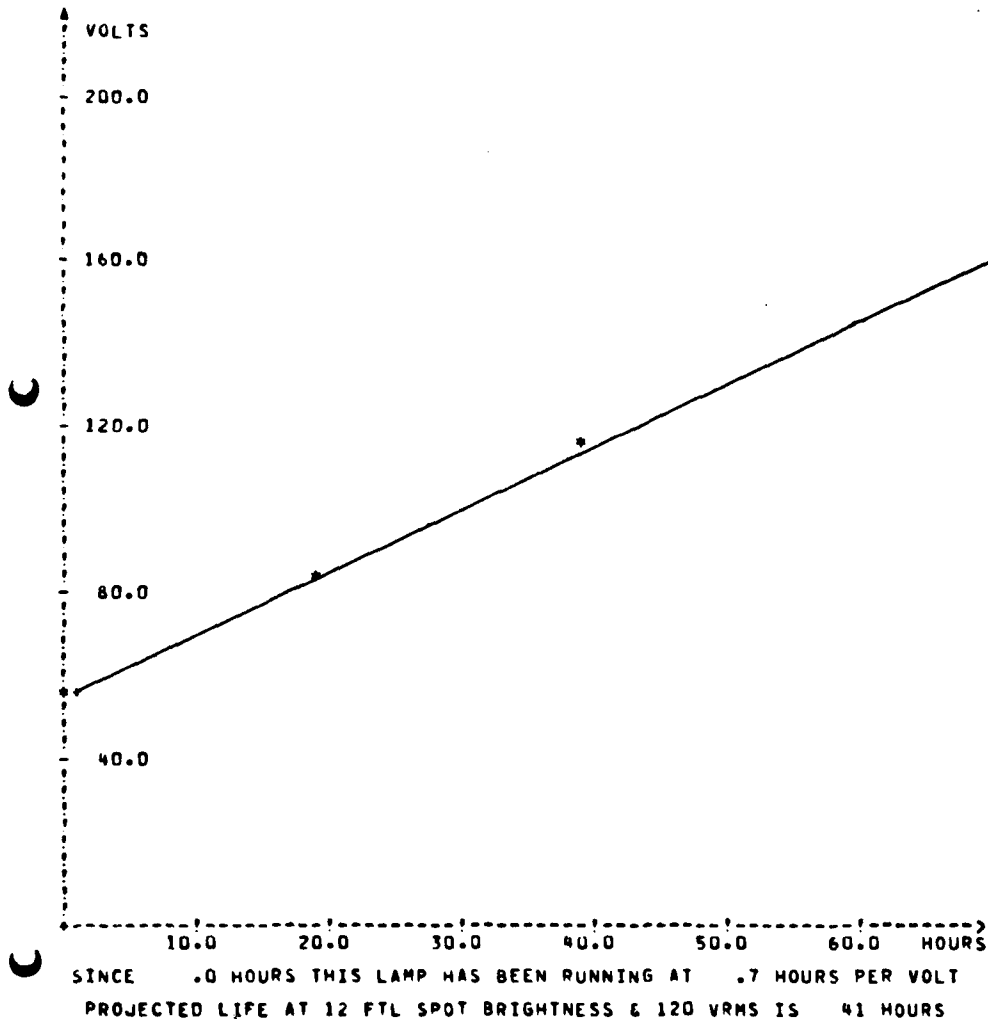


Figure 7.50 Life Testing Analysis of Sample Number 568-4 listed in Table 7.4, Constituting the First Encapsulation Experiment. Sample Configuration is Stycast Encapsulant and Polysulfide Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Air.

UPDATE FEBRUARY 20, 1979

SAMPLE NUMBER	568-5	FIGURING BOOK REFERENCE	951/144
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	11-06-78
OVEN NUMBER	1	TEST AMBIENT	AIR
BRIGHTNESS	3.6	TEST TEMPERATURE	72 DEG C
SAME AS 568-4		BASE COAT WT	:::
		TOP COAT 1	:::
		TOP COAT 2	:::
		PHOSPHOR WEIGHT	:::
		SHEET RESISTANCE	:::

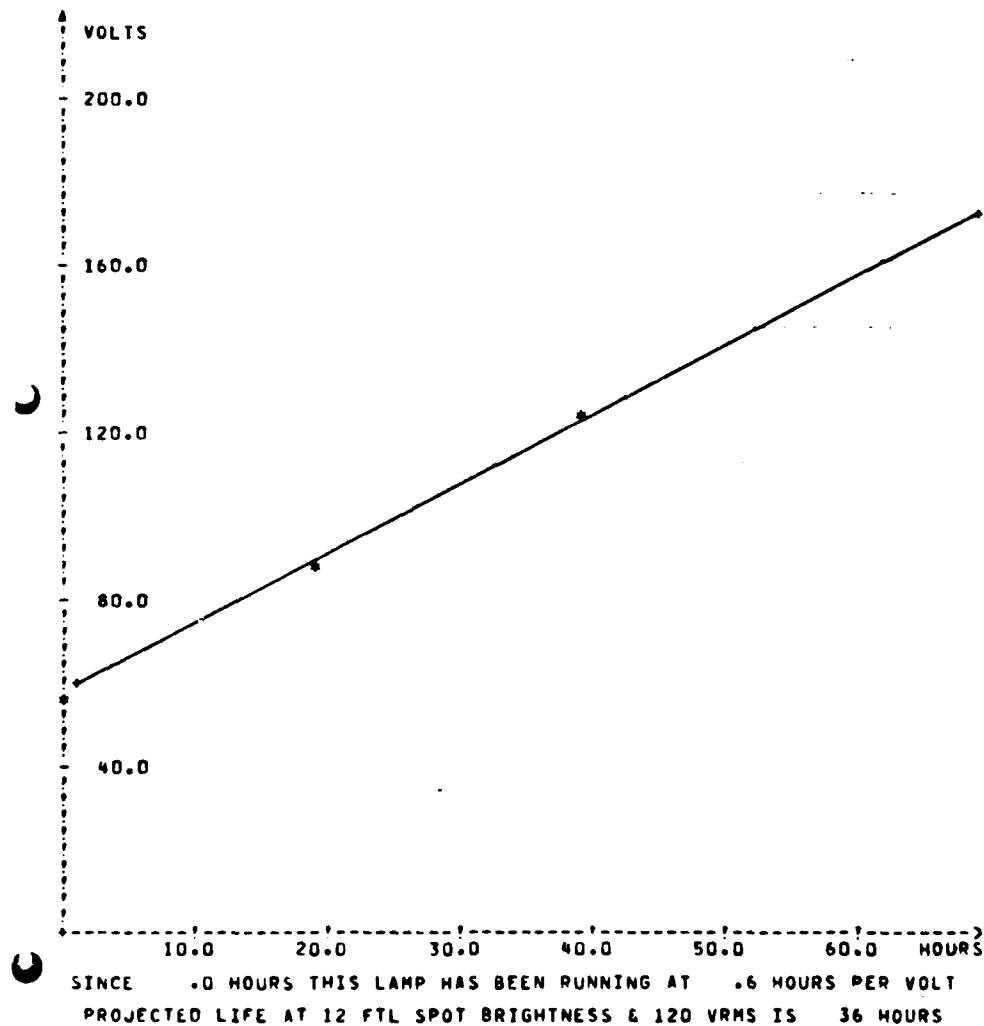


Figure 7.51 Life Testing Analysis of Sample Number 568-5 listed in Table 7.4, Constituting the First Encapsulation Experiment. Sample Configuration is Stycast Encapsulant and Polysulfide Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Air.

UPDATE FEBRUARY 14, 1979

SAMPLE NUMBER 566-3  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6

ENCAP TEST NO. 1  
POLYSULFIDE EDGE  
SEAL AROUND COVER  
GLASS - NO STYCAST

FIGURING BOOK REFERENCE 207951/144  
DATE FABRICATED 11-05-78  
TEST AMBIENT AIR  
TEST TEMPERATURE 72 DEG C

BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE

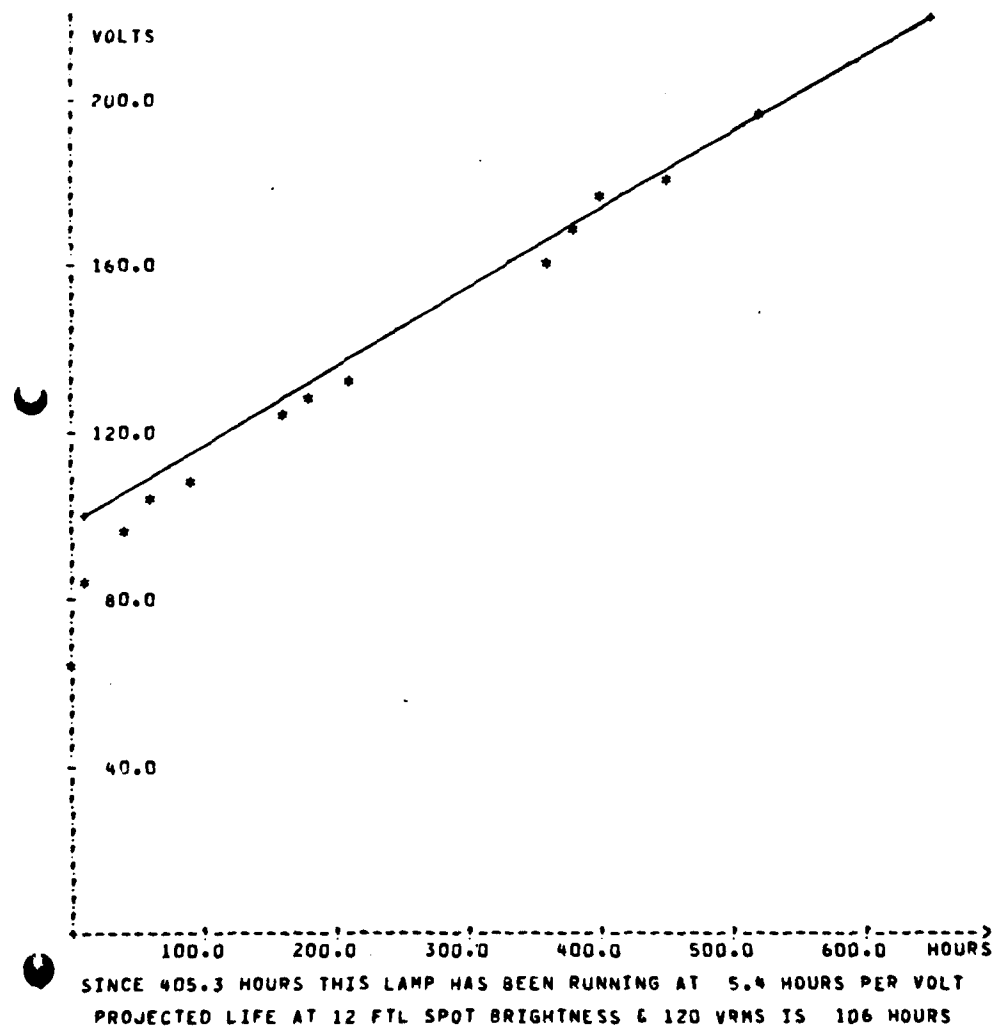


Figure 7.52

Life Testing Analysis of Sample Number 566-3 listed in Table 7.4, Constituting the First Encapsulation Experiment. Sample Configuration is no Encapsulant and Polysulfide Edge Seal. Sample Had Cover Glass and Was Tested in 72°C Air.

- (3) The polysulfide edge seal samples (with no Stycast), 566-4 and 566-3, exhibit significantly above average threshold voltage for which we have no explanation.

On the basis of the results and conclusions derived from this first experiment, we formulated the following two hypotheses.

- H1. The Stycast epoxy, as ordinarily prepared, contained water whose deleterious properties with respect to phosphor maintenance were well established.
- H2. The Stycast chemistry itself was basically hostile towards the stability of the phosphor at 72°C.

These hypotheses were tested in a second encapsulation experiment wherein tactics were employed to separate out what were perceived as distinct effects, namely, inherent hostility of the materials used in encapsulation themselves - chiefly Stycast epoxy - towards the phosphor layer subsystem, and the failure of these materials adequately protect the same subsystem from the air ambient at 72°C. Accordingly, this second experiment dealt exclusively with inherent hostility and featured samples tested at 72°C in vacuum alone. The encapsulants were specially pre-dried Stycast epoxy and an alternate material, silicone RTV. The Stycast was prepared with two different component ratios of hardener which was suspected as being responsible for the degradation of the phosphor layer subsystem. Some postage stamp samples were fitted with a cover glass and others did not have one. All samples had the state-of-the-art lead oxide top electrode base, since the experiment was conducted prior to the hypothesis that this material had a deleterious effect on the phosphor grains was formulated. A new feature was adopted, however, wherein the top electrodes of all samples were sprayed with a mechanically protective thin layer of Krylon before application of the encapsulant. We knew from prior experience that this material had no deleterious effect on the phosphor layer subsystem. The experimental configurations and corresponding results of 72°C life testing are shown in Table 7.5. As before, all samples featured as closely as possible

Table 7.5 Comparison of 72°C Maintenance Performances in Vacuum of Postage Stamp Display Simulators with Alternative Pre-Dried Encapsulants - no Edge Seal: Lead Oxide Top Electrode Base Hall Samples.

Sample Number	Figure Number	Sample Configuration		Performance		Duration of Test (hours)
		No Cover Glass	With Cover Glass	Inverse Degradation Rate Hrs/volt	Maintenance for 120 vrms Voltage $V_T$	
575-1	7.25		Control	4.3	118	350
575-6	7.26	NA	Samples - no encapsulant or edge seal	3.7	95	160
575-7	7.53	NA	Pre-dried Stycast with 28% Hardener	2.5	16	170
575-3	7.54	NA	Pre-dried Stycast with 20% Hardener	2.1	33	190
575-9	7.55	NA	Pre-dried Silicone RTV Encapsulant	3.1	123	380
575-2	7.56	Pre-dried Stycast with 28% Hardener	NA	2.6	45	170
575-8	7.57	Pre-dried Stycast with 20% Hardener	NA	2.9	120	370
575-4	7.58	Pre-dried Silicone RTV Encapsulant	NA	3.6	139	370

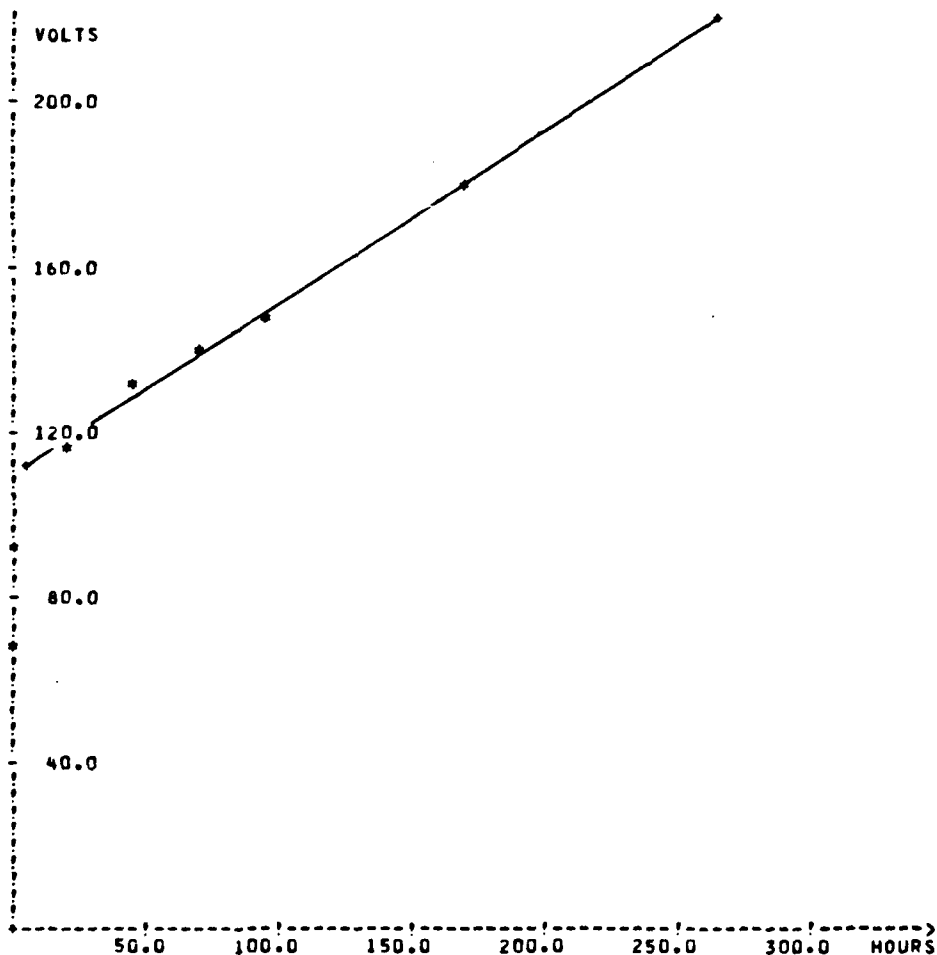
UPDATE

SAMPLE NUMBER 575-7  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

PREDRIED STYCAST & SILICON  
RTV TEST WITH KRYLON  
OTHER LAMPS IN SERIES 1 THRU 8  
28% STYCAST  
WITH COVER

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .45  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT -----  
SHEET RESISTANCE -----



SINCE 47.5 HOURS THIS LAMP HAS BEEN RUNNING AT 2.5 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 V RMS IS 16 HOURS

Figure 7.53 Life Testing Analysis of Sample 575-7 listed in Table 7.5 Describing the Second Encapsulation Experiment. Encapsulant is Predried Stycast with 28% Hardener with Cover Glass. Ambient is 72°C Vacuum.



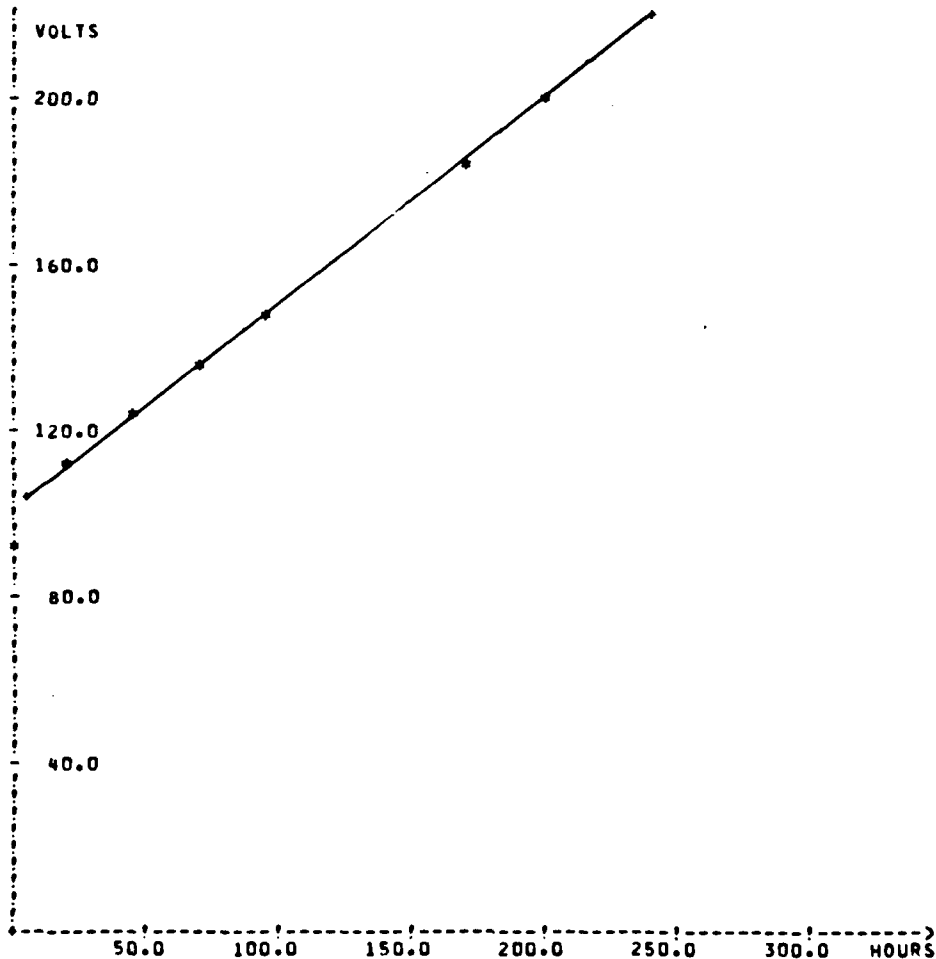
UPDATE

SAMPLE NUMBER 575-3  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

PREDRIED STYCAST & SILICON\*  
RTV TEST WITH KRYLON  
OTHER LAMPS IN SERIES 1 THRU 8\*  
20% STYCAST\*  
NO COVER GLASS\*

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .45  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT -----  
SHEET RESISTANCE -----



SINCE 47.5 HOURS THIS LAMP HAS BEEN RUNNING AT 2.1 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 33 HOURS

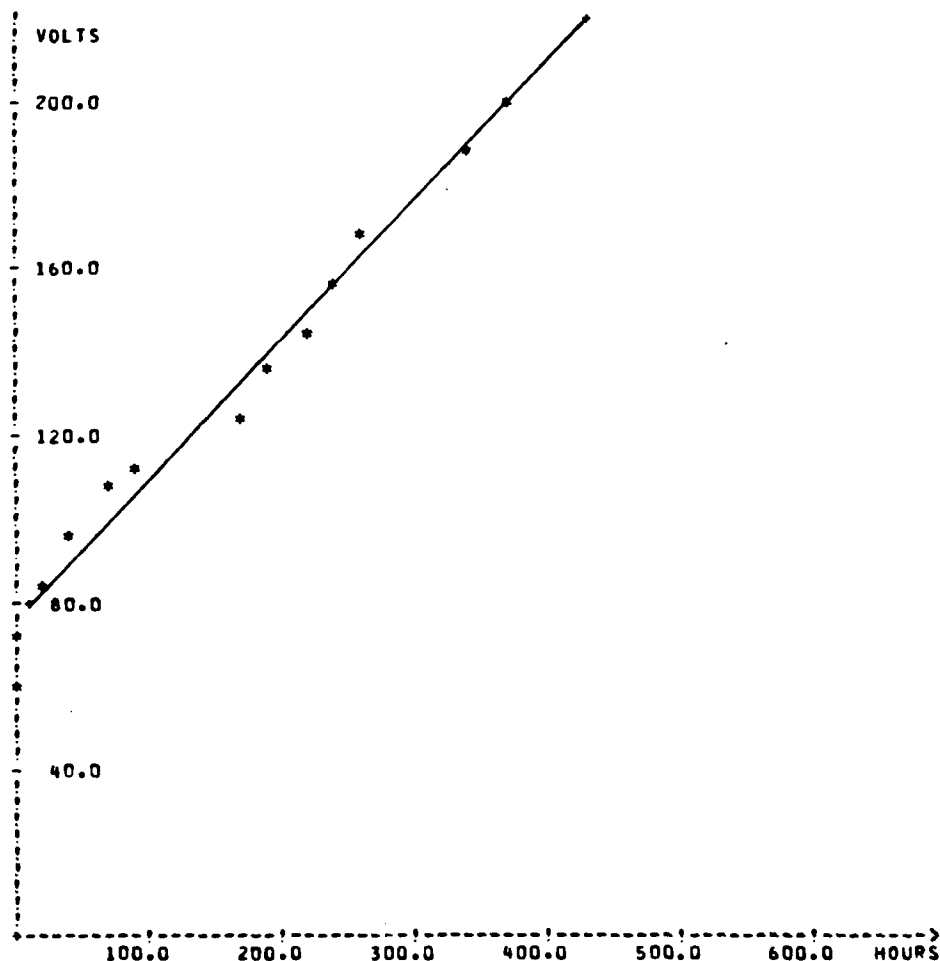
Figure 7.54 Life Testing Analysis of Sample 575-3 Listed in Table 7.5 Describing the Second Encapsulation Experiment. Encapsulant is Predried Stycast with 20% Hardener with Cover Glass. Ambient is 72°C Vacuum.

UPDATE

SAMPLE NUMBER 575-9  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6  
  
PREDRIED STYCAST & SILICONE\*  
RTV TEST WITH KRYLON\* \* \*  
OTHER LAMPS IN SERIES 1 THRU 8\*  
SILICONE RTV\*  
WITH COVER GLASS\*

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .45  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT ----  
SHEET RESISTANCE ----



SINCE 47.5 HOURS THIS LAMP HAS BEEN RUNNING AT 3.1 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 123 HOURS

Figure 7.55

Life Testing Analysis of Sample 575-9 Listed in Table 7.5  
Describing the Second Encapsulation Experiment. Encapsulant  
is Predried Silicone RTV with Cover Glass. Ambient is 72°C  
Vacuum.

UPDATE

SAMPLE NUMBER 575-2  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

PREDRIED STYCAST & SILICONE  
RTV TEST WITH KRYLON  
OTHER LAMPS IN SERIES 1 THRU 8  
8% STYCAST  
NO COVER GLASS

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .45  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT ----  
SHEET RESISTANCE ----

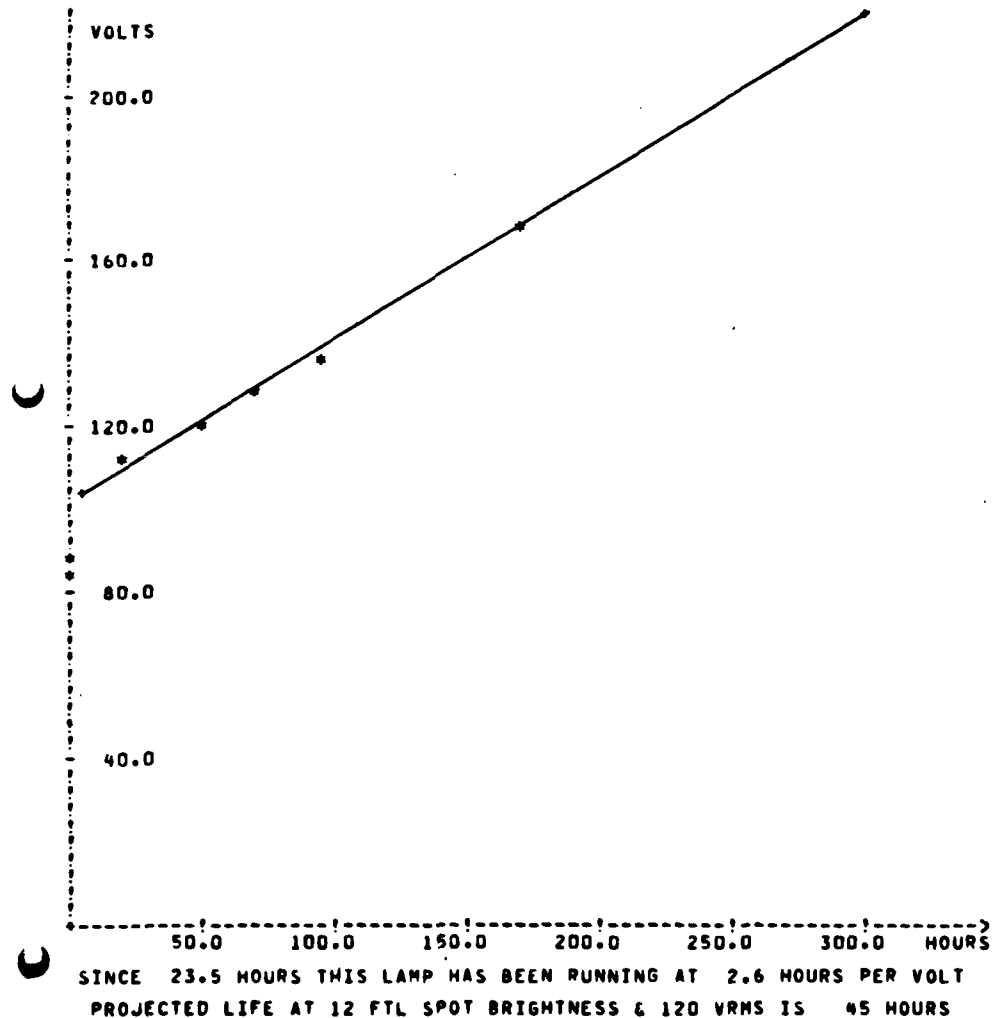


Figure 7.56 Life Testing Analysis of Sample 575-2 Listed in Table 7.5 Describing the Second Encapsulation Experiment. Encapsulant is Predried Stycast with 20% Hardener with no Cover Glass. Ambient is 72°C Vacuum.

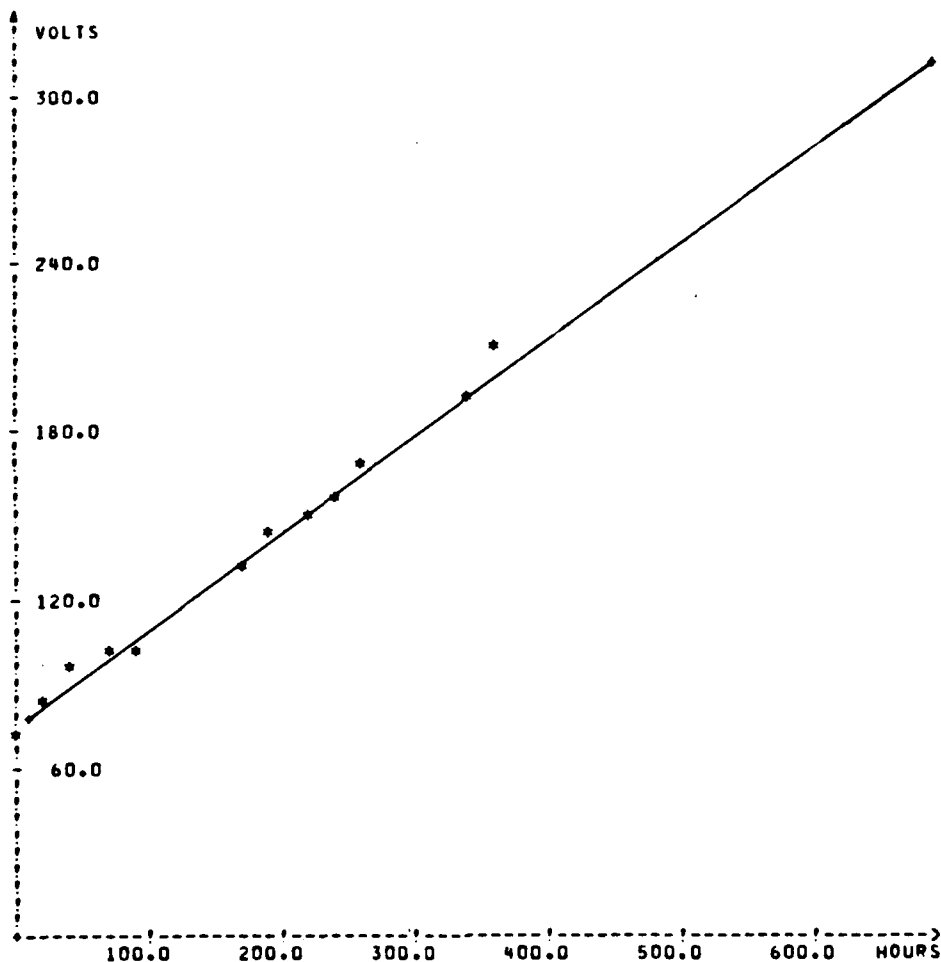
UPDATE

SAMPLE NUMBER 575-8  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

PREDRIED STYCAST & SILICONE  
RTV TEST WITH KRYLON  
OTHER LAMPS IN SERIES 1 THRU 8  
20% STYCAST  
WITH COVER GLASS

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT 180  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT ----  
SHEET RESISTANCE ----



SINCE 23.5 HOURS THIS LAMP HAS BEEN RUNNING AT 2.9 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 120 HOURS

Figure 7.57 Life Testing Analysis of Sample 575-8 Listed in Table 7.5 Describing the Second Encapsulation Experiment. Encapsulant is Predried Stycast with 20% Hardener with no Cover Glass. Ambient is 72°C Vacuum.

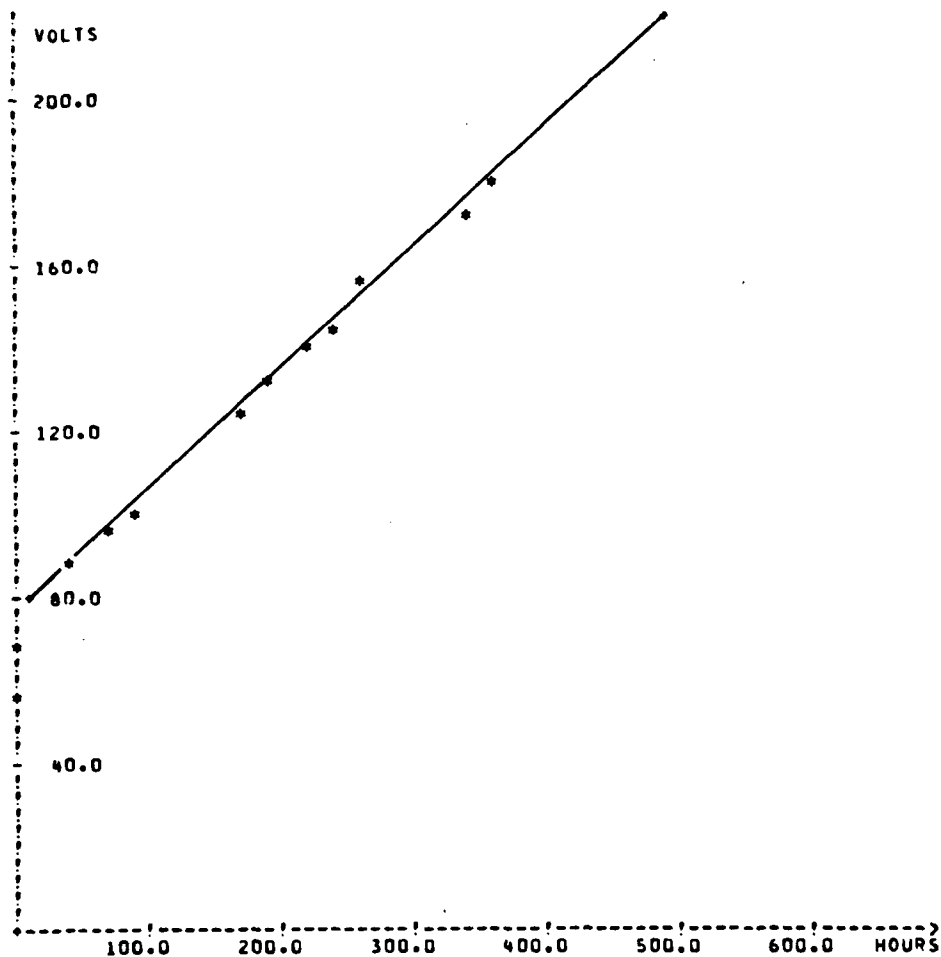
UPDATE

SAMPLE NUMBER 575-4  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 2  
BRIGHTNESS 3.6

PREDRIED STYCAST & SILICONE  
RTV TEST WITH KRYLON  
OTHER LAMPS IN SERIES 1 THRU 8  
SILICONE RTV  
NO COVER GLASS

FIGURING BOOK REFERENCE 207951-145  
DATE FABRICATED 12-01-78  
TEST AMBIENT VACUUM  
TEST TEMPERATURE 72 DEG C

BASE COAT WT .45  
TOP COAT 1 .22  
TOP COAT 2 .46  
PHOSPHOR WEIGHT -----  
SHEET RESISTANCE -----



SINCE 269.0 HOURS THIS LAMP HAS BEEN RUNNING AT 3.6 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 139 HOURS

Figure 7.58 Life Testing Analysis of Sample 575-4 Listed in Table 7.5 Describing the Second Encapsulation Experiment. Encapsulant is Predried Silicone RTV with no Cover Glass. Ambient is 72°C Vacuum.

identical structure as regards phosphor weight, CE:PVA binder thickness, and top electrode sheet resistivity. Maintenance was again defined for 12 fL spot brightness and maximum 5 kHz excitation was again 120 VRMS. The computer graphics pertaining to samples 575-7 through 575-4 in the order listed in Table 7.5 are shown in Figures 7.53 through 7.58 respectively.

With reference to Table 7.5, we note an affirmative response to both hypotheses H1 and H2 advanced previously. The pre-drying of the standard 28% Stycast mix, all other conditions remaining the same, results in the favorable comparison as shown in Table 7.6.

Table 7.6. Impact of Pre-drying the Standard 28% Stycast Mix on Sample 72°C Performance in Vacuum

	Sample 568-6	Sample 575-7
Inverse Degradation Rate Hrs/volt	0.2	2.5
Maintenance Hrs.	11	16
Threshold Voltage	60	110

With respect to suspicions centered on the chemistry of the Stycast mix, and in particular on the hardener, we observed in Table 7.7 significantly better maintenances provided by the lower 20% ratio. In fact, in the case of sample 575-8, we observe even better performance in this respect than the unencapsulated control samples 575-1 and 575-6. However, here we may be observing the effects of the lead oxide electrode base becoming dominant. In any event, with reference again

Table 7.7      Impact of Different Pre-dried Stycast Mix Hardener Ratios  
on 72°C Encapsulated Postage Stamp Life Testing

Sample	Hardener Ratio	Main- tenance Hrs.	Inverse Degradation Rate	Threshold Voltage	
575-7	28%	16	2.5	110	Without
575-3	20%	33	2.1	105	Cover
					Glass
575 2	28%	45	2.6	105	With
575-8	20%	120	2.9	80	Cover
					Glass

to Table 7.5 we observe conclusively superior performance of the silicone RTV encapsulant which is consistent with the data shown in Tables 7.6 and 7.7 identifying both the Stycast hardener chemistry and any residual water contamination being deleterious to phosphor performance.

It was at this point in the developmental activity that we focussed attention on the somewhat mediocre performance of control samples 575-1 and 575-6 of the second encapsulation experiment and conducted phosphor layer Experiment No. 3 previously discussed in connection with the data in Table 7.3. There we clearly identified the relatively deleterious effect of lead oxide as a top electrode base and successfully substituted cadmium fluoride. From this point on, cadmium fluoride was adopted as a standard material in the same way we had earlier switched from cyanoethylated sucrose-starch to cyanoethylated polyvinyl alcohol for the binder.

Accordingly, a third encapsulation experiment was devised to compare performances of unencapsulated control postage stamps with similar devices encapsulated with a silicone RTV and a cover glass. Two samples

of each type were all fabricated with cadmium fluoride but 72°C testing was confined to a vacuum ambient. The reason was that we were looking for a comparison of the effect of the silicone RTV encapsulant on devices fabricated on the one hand with lead oxide and, on the other, with cadmium fluoride top electrode bases. In addition, we needed to compare in absolute terms the performance of the cadmium fluoride-silicone RTV configuration with the best unencapsulated devices we could then make, in a search for any deleterious effects between the silicone RTV and the cadmium fluoride. Sample configurations and results are shown in Table 7.8. Graphical analyses for control samples 577-1 and 577-2 have previously been shown in Figures 7.35 and 7.36 respectively. Corresponding computer printouts for the other two samples in the test are shown in Figures 7.59 and 7.60 respectively.



Table 7.8 Evaluation of the Silicon RTV encapsulant in Conjunction with Cadmium Fluoride  
Top Electrode Bases in 72° Life Testing in Vacuum.

Postage Stamp Sample Number	Figure Number	Description	Structural Details					Performance				
			Clear Coat Weights mg/cm <sup>2</sup>			Phosphor weight mg/cm <sup>2</sup>	Top Electrode Sheet Resistivity Ω/sq.	Inverse Degradation Rate	Maintenance to 120 vrms hrs.	Threshold Voltage V <sub>T</sub>	Duration of Test (Hours)	
			Bottom Coat	First Top Coat	Second Topcoat							
												Total
577-1	7.35	Control Samples not encapsulated	0.44	0.22	0.34	1.00	4.23	36	5.2	283	60	650
577-2	7.36		0.46	0.18	0.33	1.00	4.40	45	5.5	303	60	700
577-3	7.59	Encapsulated with Silicone RTV	0.44	0.23	0.33	1.00	4.31	100	6.2	315	65	670
577-4	7.60	and Cover Glass	0.47	0.16	0.30	0.93	4.62	47	5.0	273	65	670

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MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY--ETC(U)  
FEB 80 M W CRESSWELL, P R MALMBERG, J MURPHY DAAB07-76-C-0027

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First, two general observations can be made from the results listed in Table 7.4.8. These are that

- 1) Process refinement, by way of substituting alternative materials, had continued to deliver impressively better results to this point.

- 2) The cadmium-fluoride/silicone RTV combination offered no inherent hostility to 72°C phosphor maintenance. There is no significant difference in performance of the sample groupings shown in Table 7.8.

More specifically, the switch from lead oxide to cadmium fluoride within the context of silicone RTV encapsulated devices shows distinct advantages which have been listed in Table 7.9.

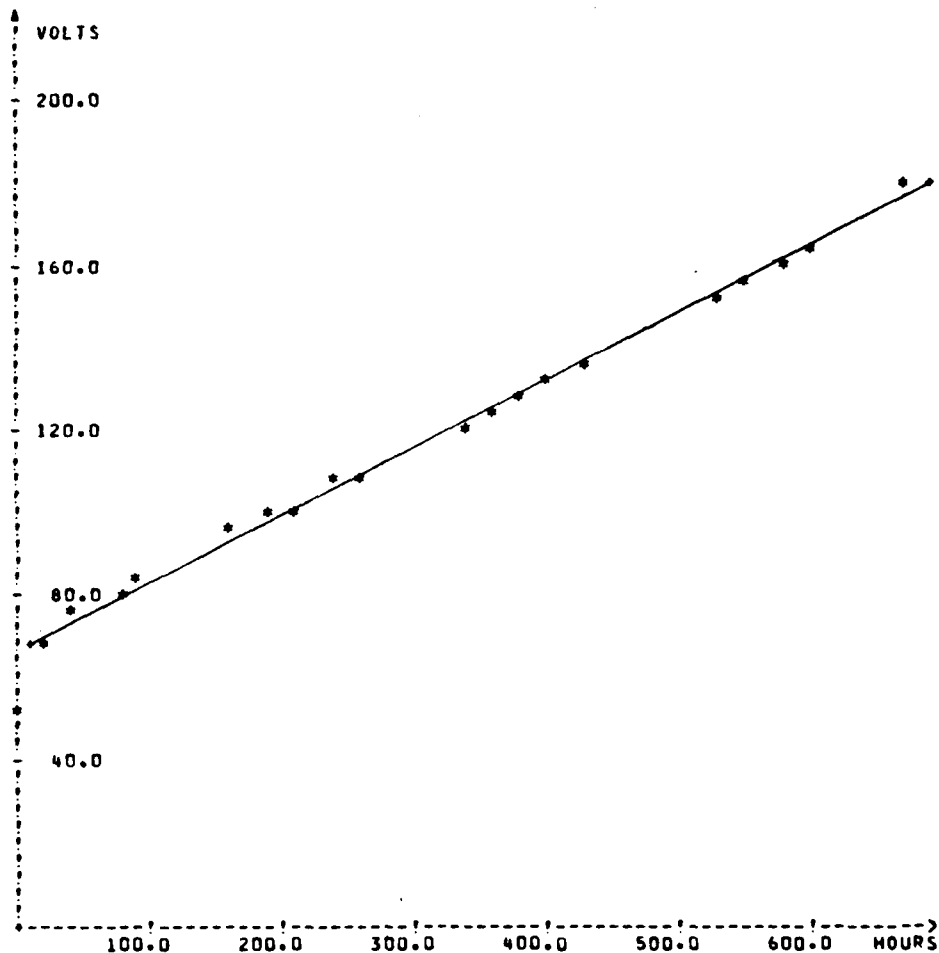
UPDATE 3-1-79

SAMPLE NUMBER 577-3  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER 1  
BRIGHTNESS 3.6 FL

NEW SOURCE  
CAD FLUORIDE  
SILICONE WITH  
GLASS COVER  
SAME AS 577-4

FIGURING BOOK REFERENCE NA  
DATE FABRICATED 1-10,11-79  
TEST AMBIENT VAC  
TEST TEMPERATURE 72C

BASE COAT WT .44  
TOP COAT 1 .23  
TOP COAT 2 .33  
PHOSPHOR WEIGHT 4.31  
SHEET RESISTANCE 100



SINCE 72.0 HOURS THIS LAMP HAS BEEN RUNNING AT 6.2 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 315 HOURS

Figure 7.59 Computer analysis of performance of Silicone RTV encapsulated Sample No. 577-3 featuring cadmium fluoride top electroding. Sample participated in third encapsulation experiment described in Table 7.8.

UPDATE 3-1-79

SAMPLE NUMBER 577-4  
SAMPLE TYPE POSTAGE STAMP  
OVEN NUMBER  
BRIGHTNESS 3.6 FL

NEW SOURCE:  
CAD FLUORIDE  
SILICONE WITH  
OVER GLASS  
SAME AS 577-3

FIGURING BOOK REFERENCE NA  
DATE FABRICATED 1-10,11-79  
TEST AMBIENT VAC  
TEST TEMPERATURE 72C

BASE COAT WT .47  
TOP COAT 1 .16  
TOP COAT 2 .30  
PHOSPHOR WEIGHT 4.62  
SHEET RESISTANCE 47

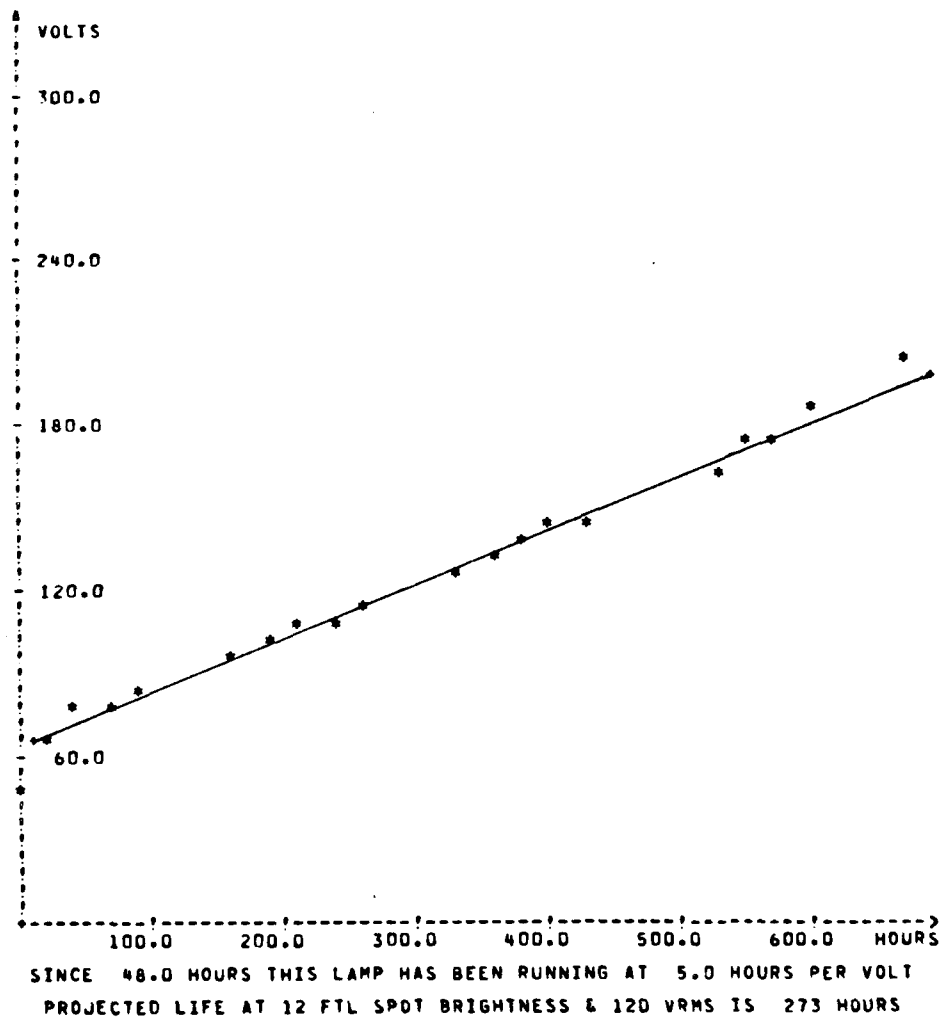


Figure 7.60 Computer analysis of performance of Silicon RTV encapsulated Sample No. 577-4 featuring cadmium fluoride top electroding. Sample participated in third encapsulation experiment described in Table 7.8.

UPDATE 4-18-79

SAMPLE NUMBER	583-1	FIGURING BOOK REFERENCE	NA
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	3-13-79
OVEN NUMBER	2	TEST AMBIENT	VAC
BRIGHTNESS	3.6	TEST TEMPERATURE	72C
FIRST OF THREE TO COMPARE SILICONE IN AIR VS VACUUM SAME AS 583-2 & 583-3		BASE COAT WT	.64
		TOP COAT 1	.26
		TOP COAT 2	.34
		PHOSPHOR WEIGHT	4.36
		SHEET RESISTANCE	130

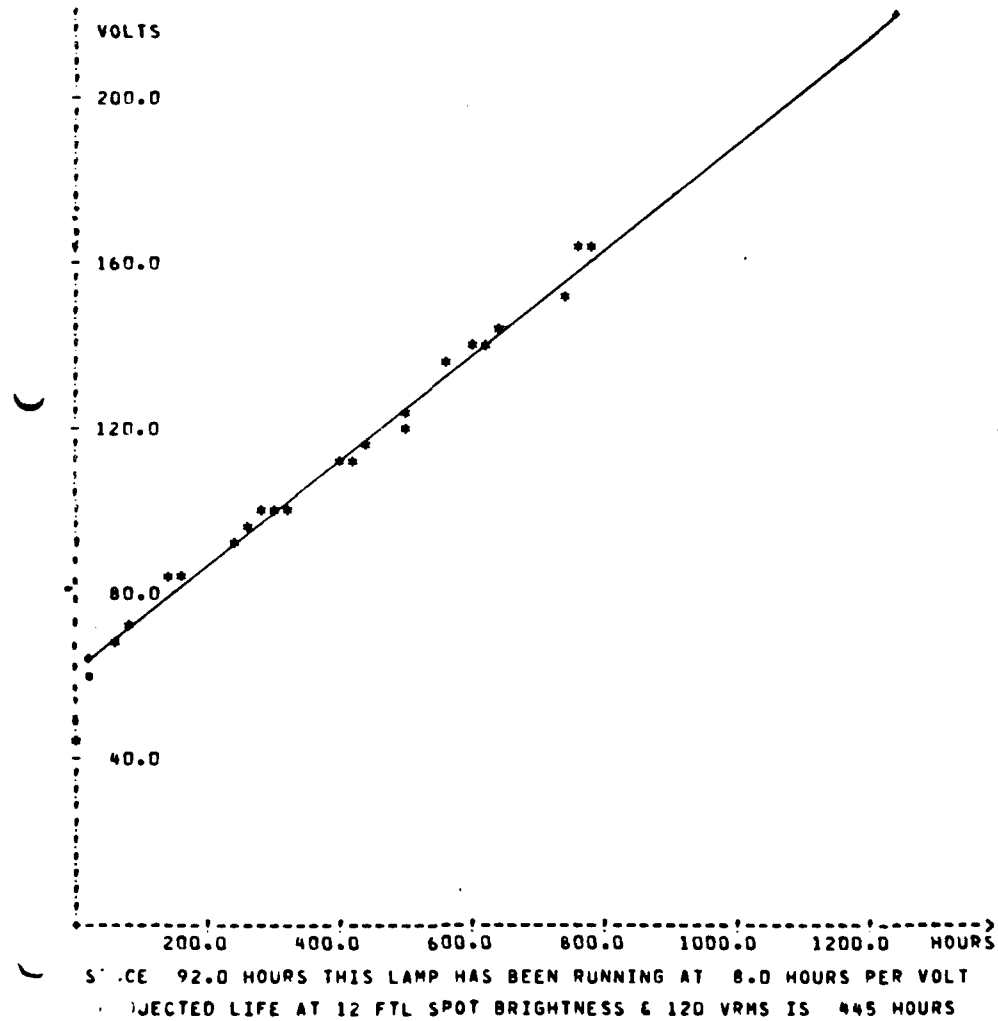


Figure 7.61 Computer analysis of performance of Postage Stamp Test Device 583-1, the first of three Silicone RTV and cover glass encapsulated units life tested in vacuum at 72°C in the fourth and final encapsulation test, illustrated in Table 7.10.

UPDATE 4-18-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS  
SEE 583-1

583-2 FIGURING BOOK REFERENCE  
POSTAGE STAMP DATE FABRICATED  
2 TEST AMBIENT  
3.6 TEST TEMPERATURE  
BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE

NA  
3-13-79  
VAC  
72C  
.64  
.27  
.39  
4.23  
140

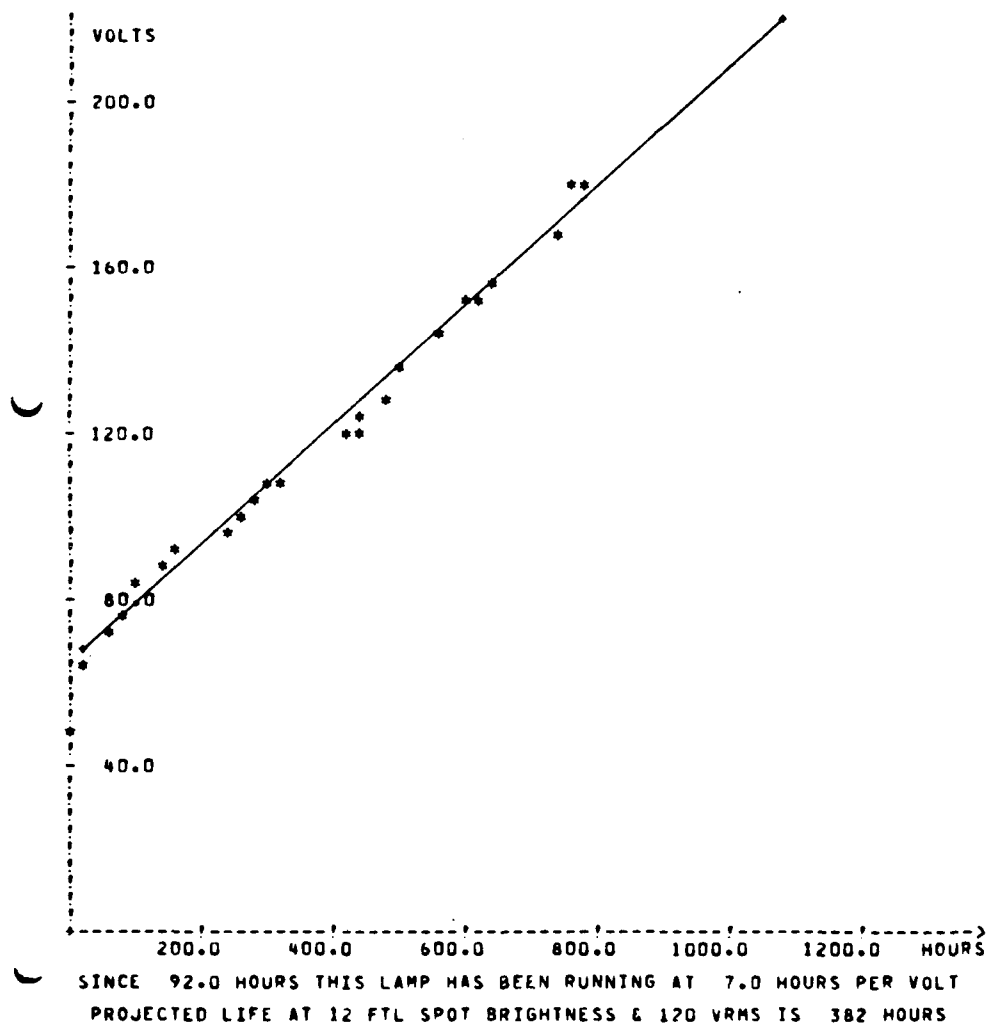
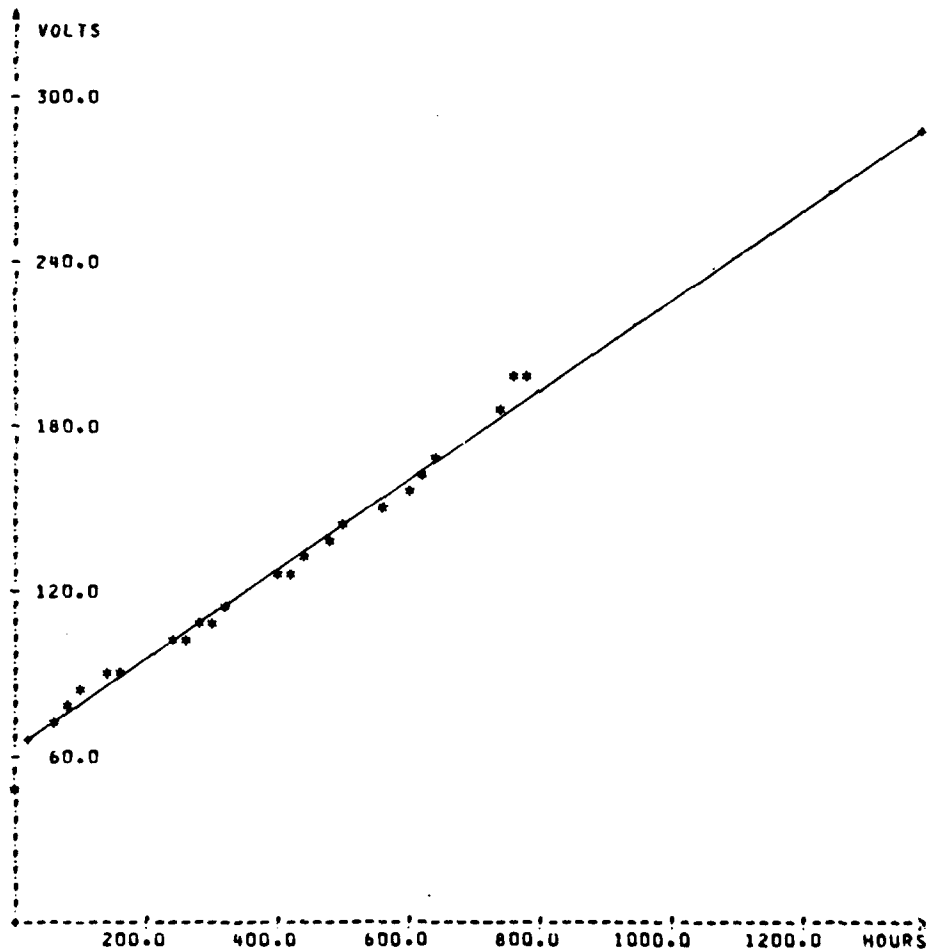


Figure 7.62 Computer analysis of performance of Postage Stamp Test Device 583-2, the second of three Silicone RTV and cover glass encapsulated units life tested in vacuum at 72°C in the fourth and final encapsulation test, illustrated in Table 7.10.

UPDATE 4-18-79

SAMPLE NUMBER	583-3	FIGURING BOOK REFERENCE	NA
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	3-13-79
OVEN NUMBER	2	TEST AMBIENT	VAC
BRIGHTNESS	3.6	TEST TEMPERATURE	72C
SEE 583-1		BASE COAT WT	.62
FREQ. FOR		TOP COAT 1	.28
583-1 THRU -6		TOP COAT 2	.39
ALL 5KHZ		PHOSPHOR WEIGHT	4.05
		SHEET RESISTANCE	120



SINCE 68.0 HOURS THIS LAMP HAS BEEN RUNNING AT 6.1 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 340 HOURS

Figure 7.63 Computer analysis of performance of Postage Stamp Test Device 583-3, the third of three Silicone RTV and cover glass encapsulated units life tested in vacuum at 72°C in the fourth and final encapsulation test, illustrated in Table 7.10.



UPDATE 4-9-79

SAMPLE NUMBER	583-4	FIGURING BOOK REFERENCE	NA
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	3-13-79
OVN NUMBER	3	TEST AMBIENT	AIR
BRIGHTNESS	3.6	TEST TEMPERATURE	72C
583-4 THRU -6		BASE COAT WT	.65
SAME AS 583-1 THRU		TOP COAT 1	.28
3 EXCEPT LIT &		TOP COAT 2	.41
TESTED IN AIR BUT		PHOSPHOR WEIGHT	4.10
RESTED IN VACUUM		SHEET RESISTANCE	230

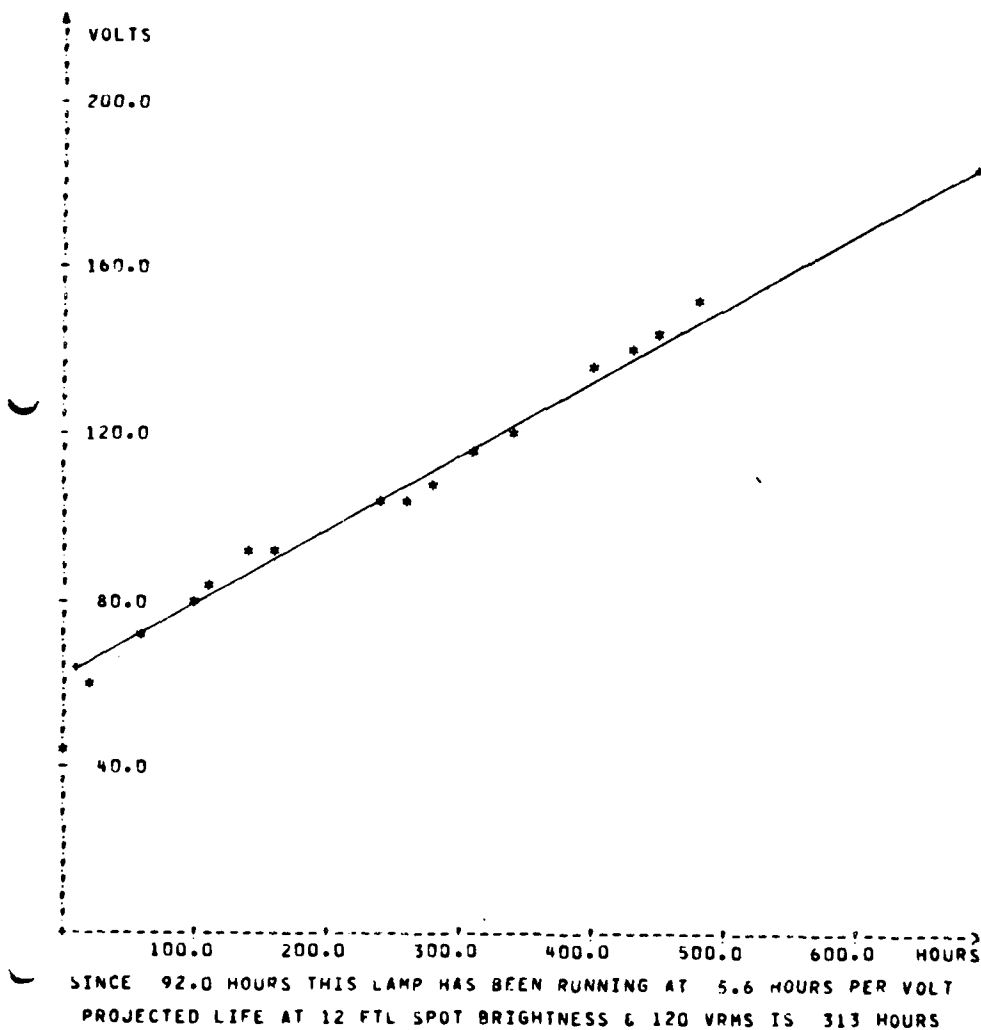


Figure 7.64 Computer analysis of performance of Postage Stamp Test Device 583-4, the first of three Silicone RTV and cover glass encapsulated units life tested in air at 72°C in the fourth and final encapsulation test, illustrated in Table 7.10.

UPDATE 4-9-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

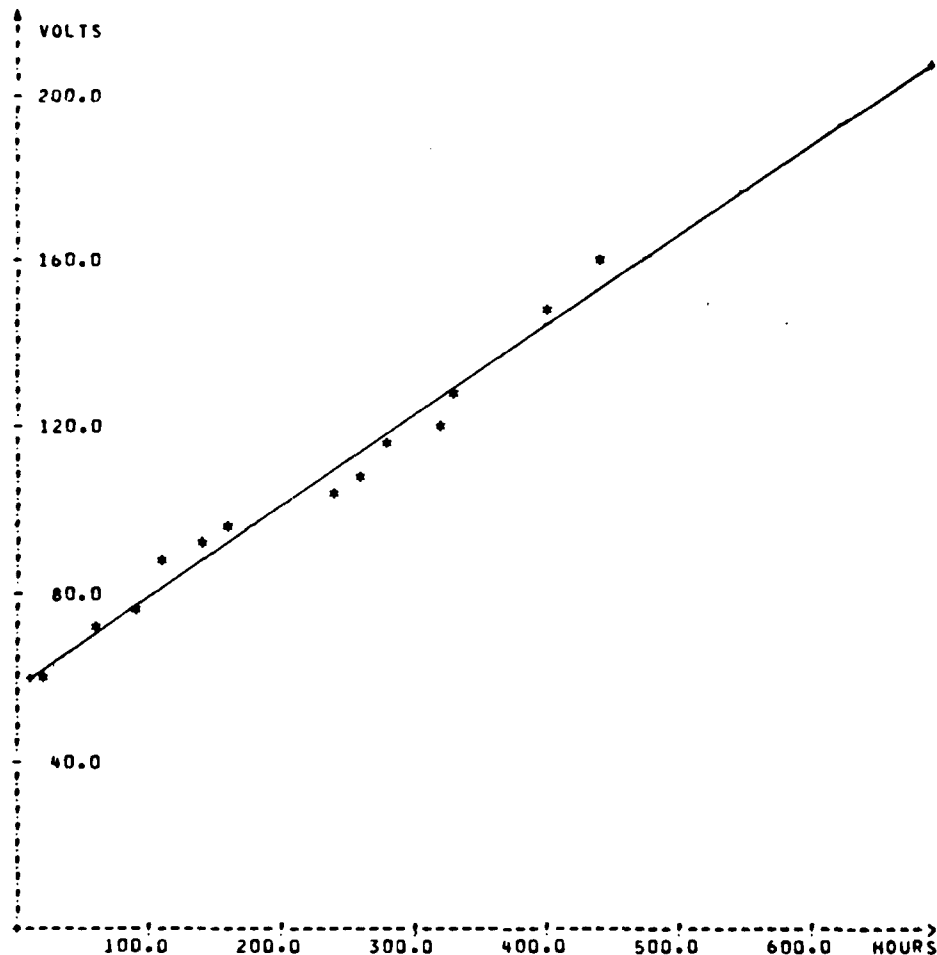
POSTAGE 583-5  
STAMP 3  
3.6

FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
3-13-79  
AIR  
72C

SEE 583-4  
ALL 583-1 THRU -6  
HAVE SILICONE AND  
COVER GLASS

BASE COAT WT .55  
TOP COAT 1 .18  
TOP COAT 2 .32  
PHOSPHOR WEIGHT 4.08  
SHEET RESISTANCE 400



SINCE 116.0 HOURS THIS LAMP HAS BEEN RUNNING AT 4.6 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 280 HOURS

Figure 7.65 Computer analysis of performance of Postage Stamp Test Device 583-5, the second of three Silicone RTV and cover glass encapsulated units life tested in air at 72°C in the fourth and final encapsulation test, illustrated in Table 7.10.

UPDATE 4-10-79

SAMPLE NUMBER	583-6	FIGURING BOOK REFERENCE	NA
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	3-13-79
OVEN NUMBER	3	TEST AMBIENT	AIR
BRIGHTNESS	3.6	TEST TEMPERATURE	72C
SAME AS 583-3 & 4		BASE COAT WT	.54
THE 583 BATCH ARE		TOP COAT 1	.22
FIRST STAMPS MADE		TOP COAT 2	.36
SINCE 2C32 VACUUM		PHOSPHOR WEIGHT	4.05
SYSTEM WAS OVERHAULED		SHEET RESISTANCE	175

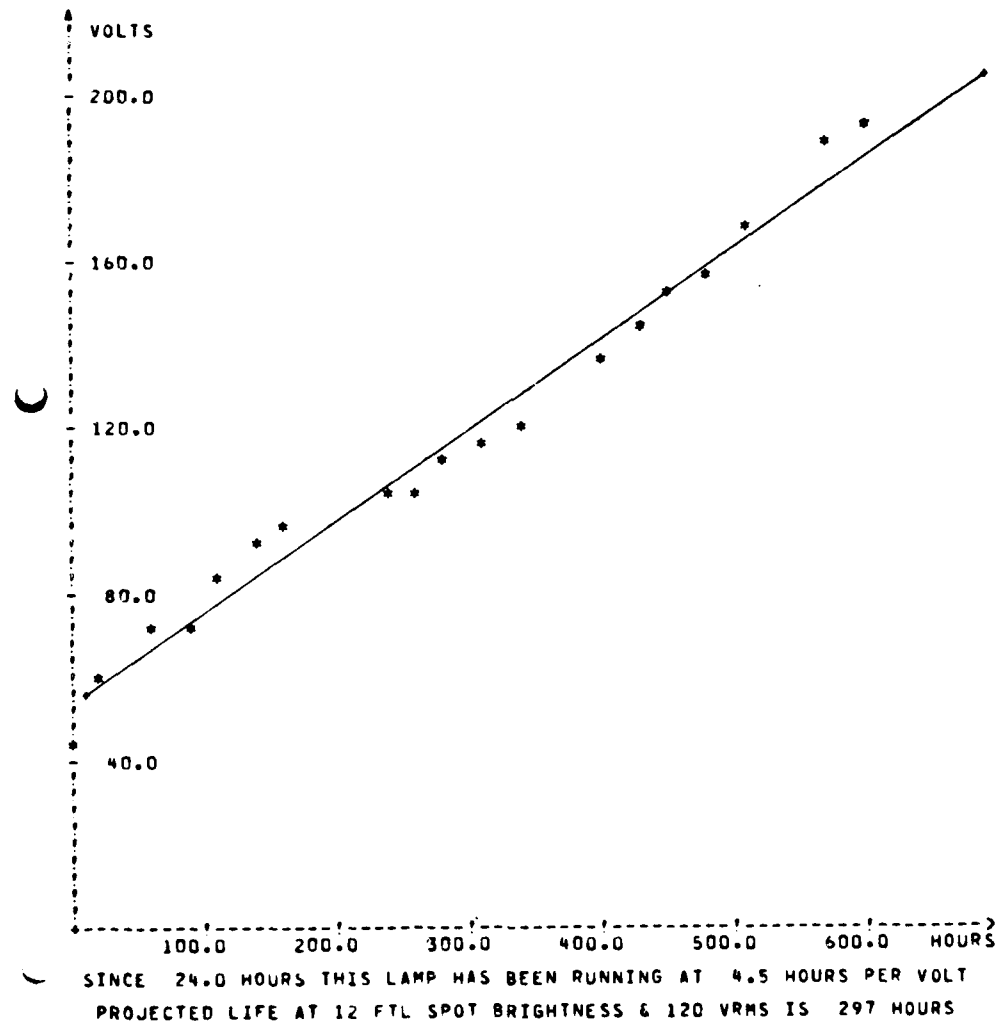


Figure 7.66 Computer analysis of performance of Postage Stamp Test Device 583-6, the third of three Silicone RTV and cover glass encapsulated units life tested in air at 72°C in the fourth and final encapsulation test, illustrated in Table 7.10.

Curve 720727-8

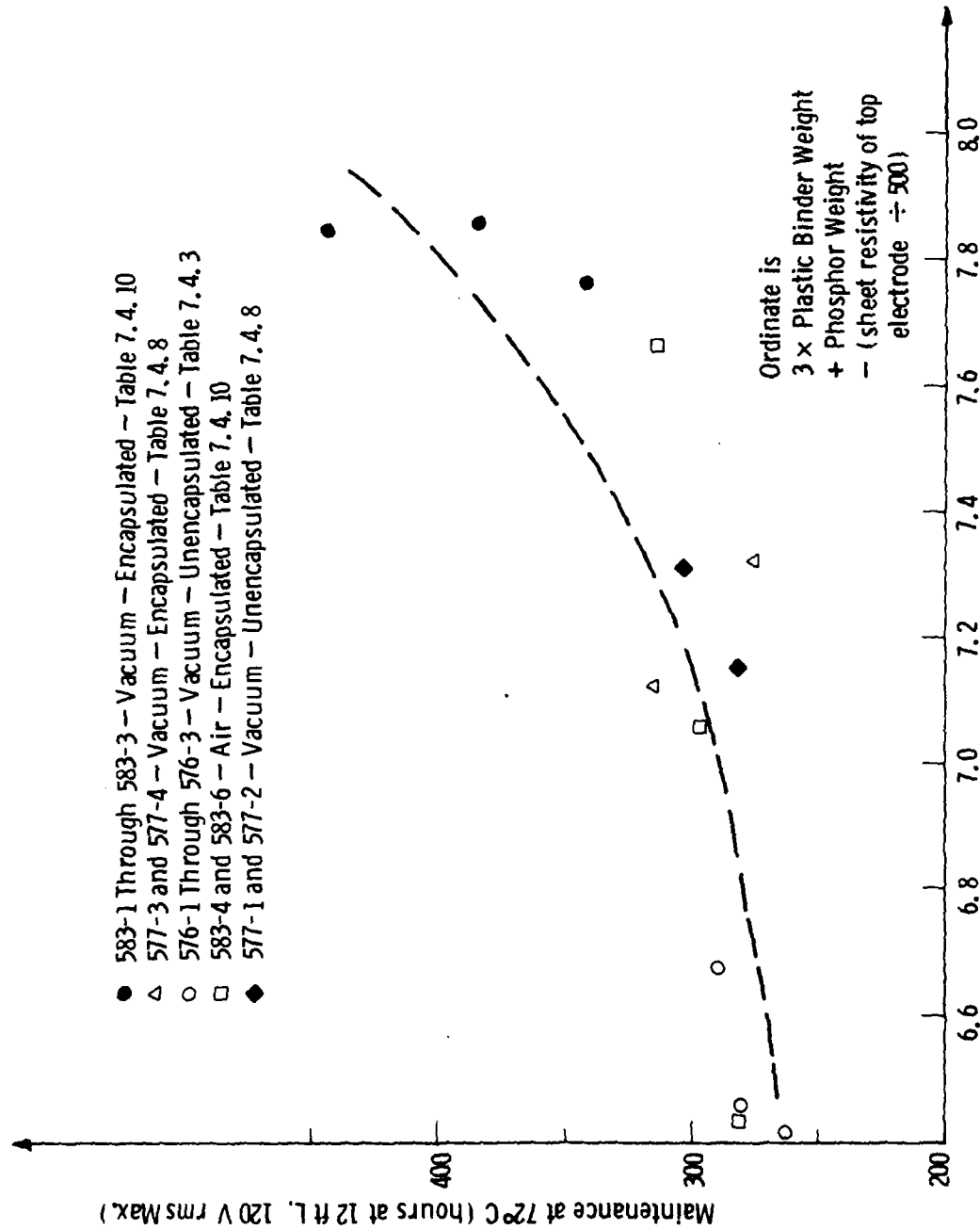


Figure 7.67 Impact of Postage Stamp fabrication parameter on 72°C maintenance for cadmium fluoride electrode bases.

Curve 720728-B

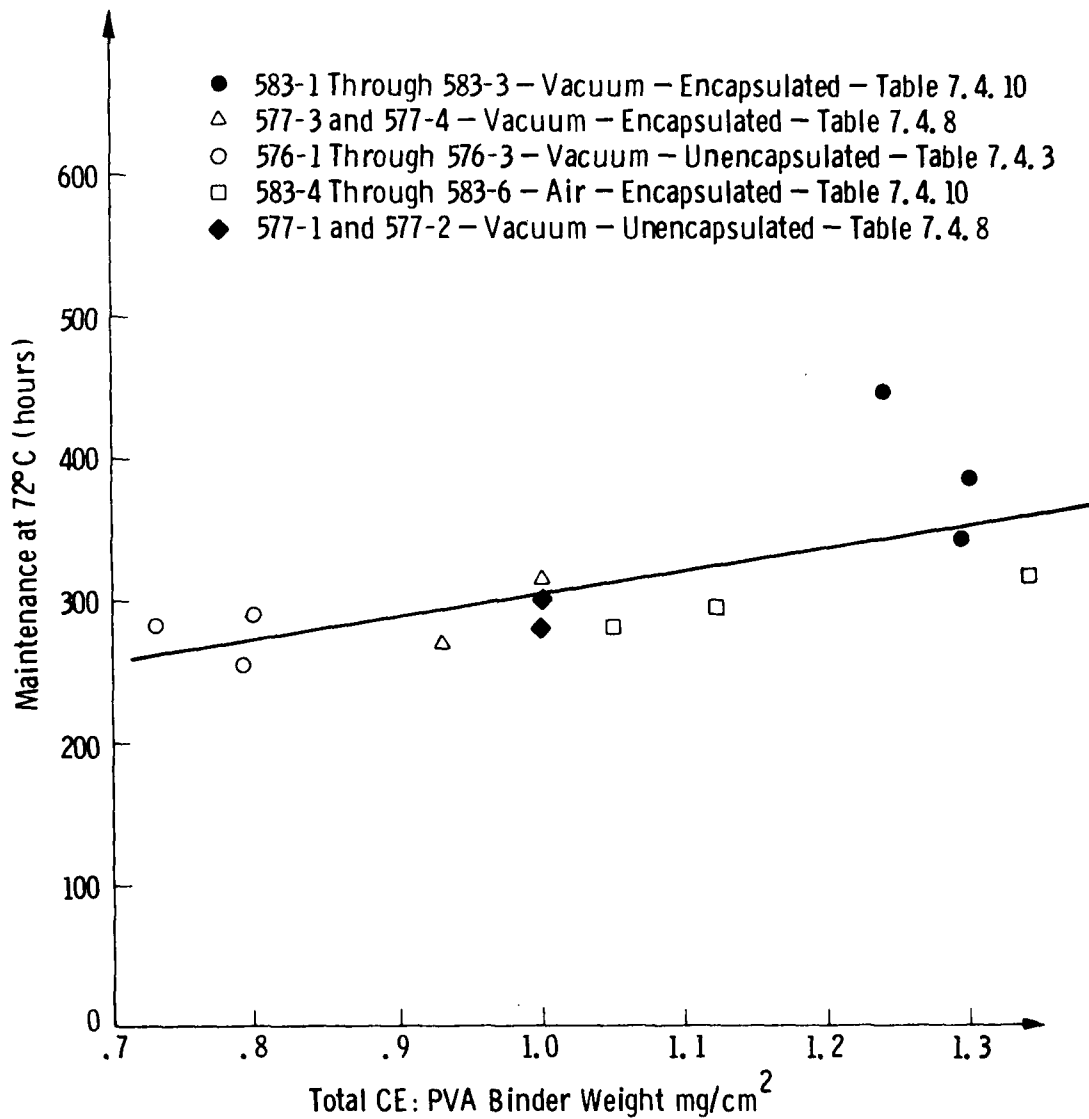


Figure 7.68 Variation of maintenance with total plastic binder weight for Postage Stamps indicated under 72°C life testing in third and fourth encapsulation tests. All devices feature CdF top electrode base, phosphor application by brushing, and CE:PVA binder.

TABLE 7. 9. COMPARISON OF THE PERFORMANCES, UNDER 72°C LIFE TESTING,  
OF SILICONE RTV ENCAPSULATED DEVICES (WITH COVER GLASSES)  
WITH CADMIUM FLUORIDE AND LEAD OXIDE TOP ELECTRODE BASES

Sample No.	Figure No.	Top Electrode Base Material	Inverse Degradation Rate W/Volt	Mainte- nance (Hours)	Thresh- old Voltage $V_T$
575-9		PbO	3.1	123	80
577-3		CdF	6.2	315	65
577-4		CdF	5.0	273	65

Finally, with respect to Table 7.8 , devices 577-3 and 577-4 show a possibly significant decrease in maintenance with plastic thickness, consistent with the broken line shown previously in Figure 7.40. This decrease in maintenance with respect to sheet resistivity of the top electrode layer, in addition, conforms to the pattern depicted in Figure 7.42.

At this point, therefore, the important consideration which could be drawn relative to 72°C performance was that, as far as vacuum testing was concerned, we had a new encapsulation system which provided performance commensurate with unencapsulated devices. It featured pre-dried silicon RTV as a substitute for Stycart epoxy. What obviously had to be done next was to test groups of samples encapsulated this way in both vacuum and air. This activity constituted the fourth and final encapsulation test, for which the sample configurations and results are shown in Table 7.10. Corresponding computer generated life testing analyses are shown in Figures 7.61 through 7.66.

With reference to Table 7.10 , we observe a small but significant inferiority in the performance of the air-tested samples in comparison to the vacuum-tested ones. However, at the same time, the top electrode sheet resistivities of the former are significantly higher than those of the latter. In light of the suspected adverse impact of this feature, originally disclosed in the discussion pertaining to the results shown in Figure 7.42, it is hard to discuss a firm conclusion concerning the effectiveness or otherwise of the silicone RTV with cover glass encapsulation system.

In particular, if we hypothesize that indeed the encapsulation is effective and consequently plot a linear function of the construction parameters total Ginder weight, phosphor weight, and sheet

TABLE 7. 10 THE FOURTH AND FINAL FORMAL ENCAPSULATION LIFE TEST AT 72°C FEATURING  
TWO GROUPS OF POSTAGE STAMP DEVICES WITH SILICONE RTV AND COVER GLASS ENCAPSULATION  
UNDER AIR AND VACUUM AMBIENTS

Sample No.	Figure No.	Ambient in Test (72°C)	Fabrication Details			Performance			Dura- tion of Test Hours
			Total Plastic mg/cm <sup>2</sup>	Phos- phor mg/cm <sup>2</sup>	Sheet Resis- tivity Ω/sq.	Inverse Degrada- tion Rate Hours/ Volt	Mainte- nance at 120 VRMS Volts	Thresh- old Voltage V <sub>T</sub>	
583-1	7.61	Vacuum	1.24	4.36	130	8.0	445	65	760
583-2	7.62	Vacuum	1.30	4.23	140	7.0	382	65	760
583-3	7.63	Vacuum	1.29	4.05	120	6.1	340	60	760
583-4	7.64	Air	1.34	4.10	230	5.6	313	60	470
583-5	7.65	Air	1.05	4.08	400	4.6	280	60	420
583-6	7.66	Air	1.12	4.05	175	4.5	297	55	580



resistivity, as in Figure 7.67, we observe a remarkable correlation of maintenance with the arbitrary function.

$3 \times \text{Ginder weight} + \text{phosphor weight} - \text{sheet resistivity}/500$  regardless of whether the samples were life tested in vacuum or in air. This analysis seems to respond positively to such a hypothesis in addition to firming up earlier indications that maintenance increases with Ginder weight and decreases with sheet resistivity, as suggested previously by data in Figures 7.31 and 7.33. We also show, in Figure 7.59, maintenance versus total Ginder weight for the same group of samples, all of which were fabricated with the new cadmium fluoride top electrode base. In both Figures 7.67 and 7.68, results for sample 576.4 have been deliberately omitted since this lamp failed prematurely under test and the extrapolated maintenance is highly suspect. This same group of samples did not show any gross correlation of maintenance with the sheet resistivity and phosphor weight individually. On the basis of results from these four encapsulation experiments, a new display packaging process was formulated during Program Phase III and it is presented in Section 8.2.

This present section concludes with a discussion of some other related results and a brief summary.

### 7.5.3 Other Related Phosphor Testing Results

So far we have presented a discussion of the reformulation of the phosphor and encapsulation process exclusively within the context of life testing at 72°C. Since no information on voltage ratcheting was available for room or any other temperature performance, we undertook to quickly examine how the new processes and fabrication procedures behaved at 25°C and an intermediate temperature of 250°C.

A selection of postage stamps was assembled from which three were tested at 25°C and four at 50°C. The various configuration parameters and results are shown in Table 7.11 and the corresponding computer graphics in Figures 7.69 through 7.75. The relationship of maintenance to temperature is shown in Figure 7.68. The 72°C samples are 583-4 through 583-6 previously listed in Table 7.10. The results clearly indicate temperature as the dominantly limiting factor in performance with respect to maintenance. Whereas it is unfortunate that the samples in Table 7.11 tested at 25°C were not encapsulated and tested in air, the effects of variation of maintenance with temperature are still well represented. The analysis of the previous section concluded tentatively that fabrication, not ambient, determined performance.

So far we have fairly convincingly demonstrated a processing technique which, in conjunction with voltage ratcheting, provides about 300 hours of 12 ft-L illumination at 72°C. Although this falls short of the program required 500 hours on the face of it, two other factors must be considered. Firstly, all the results were derived before the extraordinary benefits of the second rinse-out procedure, described in Section 7.5.2, was adopted. Secondly, this performance was consistent with a definition of maintenance with an implicit 120 V<sub>rms</sub>, corresponding to ~300 volt peak-to-peak stress on the circuit transistors. We have demonstrated in Section 5.4 that this now looks like a fairly conservative rating. This analysis holds to the extent that we used continuous sinusoidal 5 kHz AC for phosphor excitation in the related testing. However, as explained in Section 9.5 of this report, we now

know many circuit fabrication and operating advantages will accrue from modifying the display drive waveforms to accommodate certain deficiencies of the thin film transistors, real or otherwise. Thus, we should relate our existing experience with the powder phosphor under 5 kHz (continuous AC) excitation to what we now recommend, namely, significantly non-sinusoidal excitation of the type shown in Figure 7.67.

During the last month of the program we initiated a study of phosphor performance under non-sinusoidal excitation by measuring brightness of typical phosphor layers as a function of frequency. As a first step, the brightness of the phosphor as a function of continuous AC frequency was measured using two samples at 25°C. Aside from questions of life testing and maintenance, it was important to determine the scope of the flexibility at our disposal vis-à-vis bursting with different frequencies and duty cycle. Results from two similarly prepared test samples are illustrated in Figures 7.67 and 7.68.

From these curves we can conclude that brightness itself, at any given voltage, continues to increase up to at least 15 kHz, about the maximum the new exerciser design contemplated using.

With this information, the next question was--how does the phosphor layer behave in life testing at different frequencies? A further eight samples were prepared without encapsulation and mounted in three different but similar vacuum ovens. The samples in each oven were driven at a different frequency. Other than this, the tests were conducted at constant brightness with voltage ratcheting as before. The results in terms of maintenance are listed in Table 7.12 and illustrated in Figure 7.79.

Unfortunately, the spread of points at the 5 kHz mark prevents concluding anything firmer than there appears to be a sharply optimum frequency (from the maintenance viewpoint) somewhere in the range 4 to 8 kHz. An earlier observation also relates to the data shown in Figure 7.70. We have traditionally used 5 kHz for phosphor

excitation. This frequency was selected on the basis of efficiency measurements made with the former spray-starch application earlier in this program. The picture that has continuously emerged is, basically, the phosphor maintenance is largely a temperature limited characteristic. One may conjecture that the more inefficient the phosphor is (as frequency is varied), the hotter it becomes when it is driven to maintain the particular brightness we use in life testing. This ties in with our earlier observations of substantially inferior maintenance at 72°C when compared to that experienced under normal operating conditions.

While the frequency vs. maintenance tests were beginning, equipment was assembled to generate the waveform shown in Figure 7.67. The object was to examine the luminence vs. peak voltage characteristic of the phosphor layer, in parallel with the new exerciser design activity.

The 400  $\mu$ sec "on time" of the excitation AC corresponds to 10 kHz continuous excitation. The line write cycle time corresponds to a display frame refresh rate of about 10 Hz. An essential feature of this waveform is the negative DC offset equal to about one-half the peak-to-peak excitation. This feature provides a very desirable zero voltage across the sources and drains of the power transistors while their gates are being impressed with their respective video levels.

Brightness versus peak-to-peak voltage for two samples driven by this waveform are shown in Figure 7.80. These measurements were made at 25°C. The curves happen to match almost identically what we observe from similar samples at a continuous 2.5 kHz sinusoidal waveform. This just happens to be (duty cycle x 10 kHz) for the waveform shown in Figure 7.76, but increased the burst frequency to 15 kHz. The fact that brightness was lower at all voltages combined with the other observation that an 'optimum' continuous frequency exists somewhere in the 4-8 kHz range for maintenance purposes, suggests we should have life tested with two or three excitation pulses in the 400  $\mu$ sec on-time. Unfortunately, program activity had to be terminated before these issues could be resolved.

UPDATE 6-5-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

POSTAGE STAMP 589-7  
2  
3.6

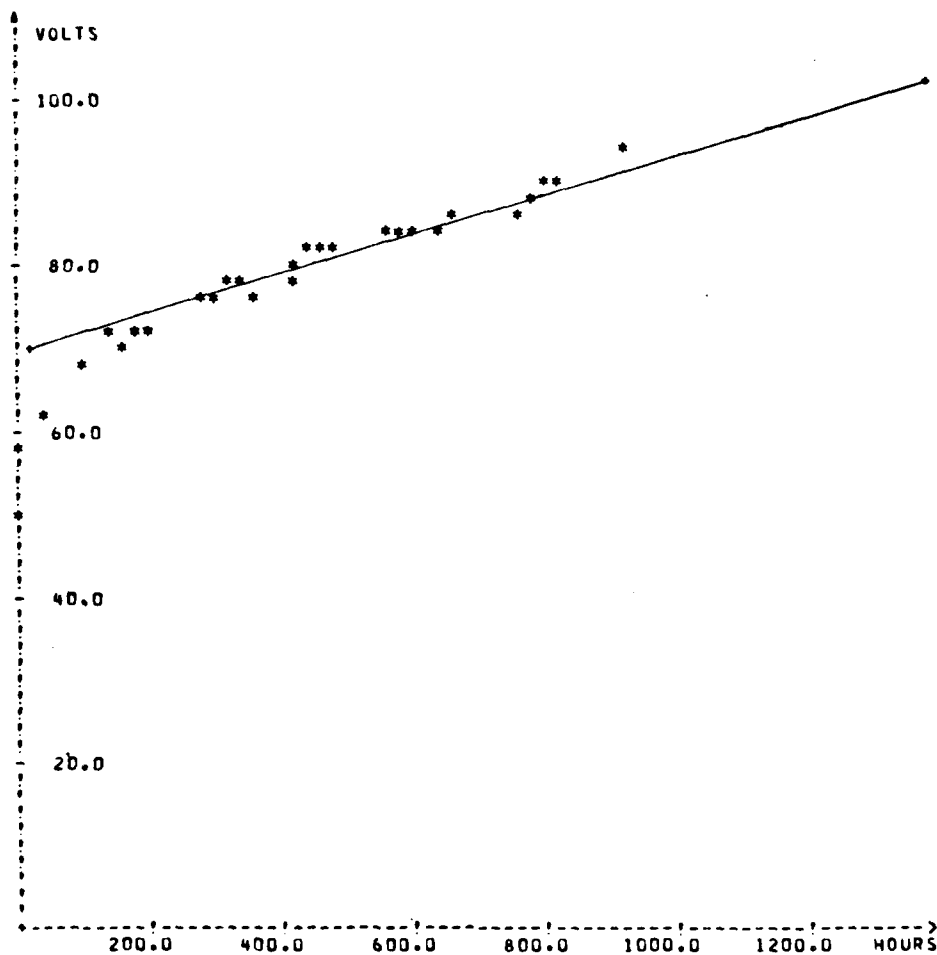
FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-25-79  
VAC  
25C

RISTON RINSE  
5KHZ-SINE  
NO REST PERIOD  
TEST @ ROOM TEMP.

BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE

.59  
.19  
.18  
4.17  
200



SINCE 450.0 HOURS THIS LAMP HAS BEEN RUNNING AT 42.5 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 2066 HOURS

Figure 7.69

Computer analysis of life testing of postage stamp  
Device No. 589-7 in an experiment to determine  
effect of ambient temperature on maintenance.

UPDATE 6-5-79

SAMPLE NUMBER	589-8	FIGURING BOOK REFERENCE	NA
SAMPLE TYPE	POSTAGE STAMP	DATE FABRICATED	4-25-79
OVEN NUMBER	2	TEST AMBIENT	VAC
BRIGHTNESS	3.6	TEST TEMPERATURE	25C
SAME AS 589-7		BASE COAT WT	.59
		TOP COAT 1	.19
		TOP COAT 2	.18
		PHOSPHOR WEIGHT	4.17
		SHEET RESISTANCE	160

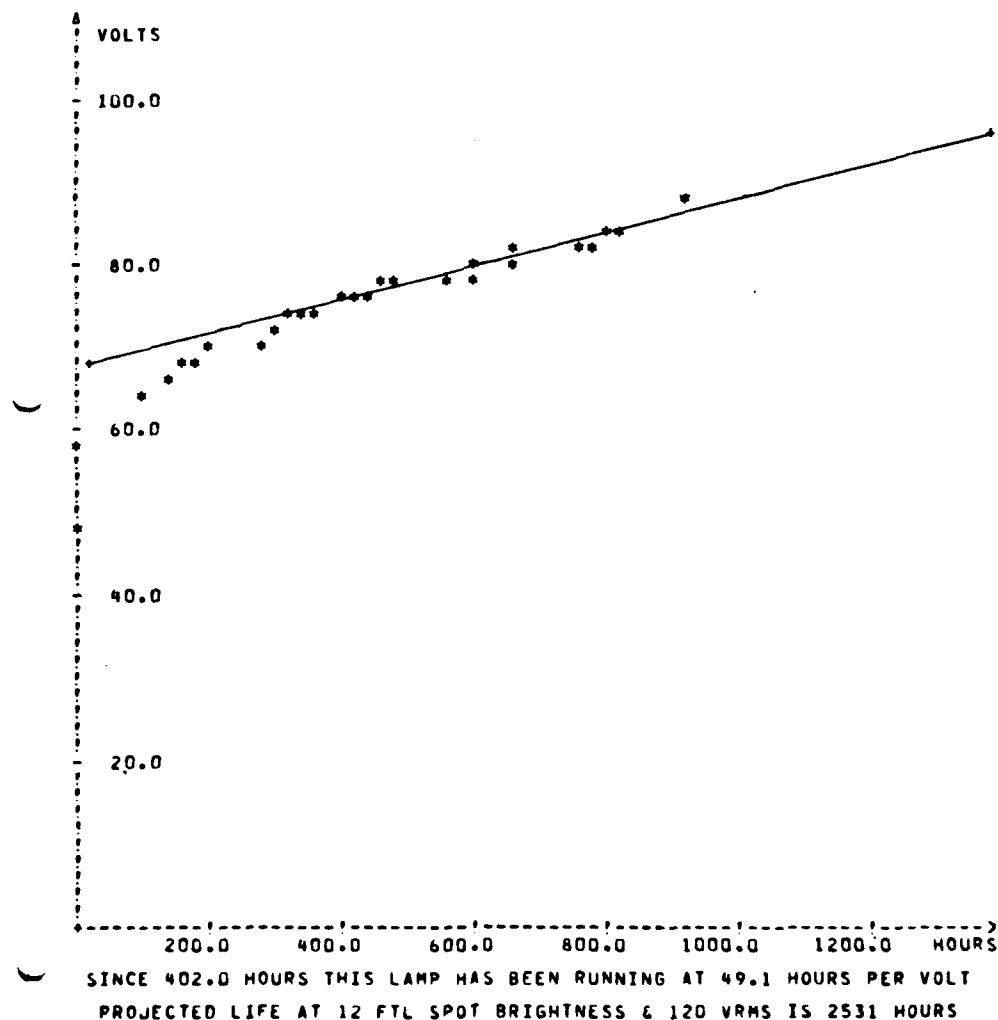


Figure 7.70 Computer analysis of life testing of postage stamp Device No. 589-8 in an experiment to determine effect of ambient temperature on maintenance.

UPDATE 6-5-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

589-9  
POSTAGE STAMP  
2  
3.6

FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-25-79  
VAC  
25C

SAME AS 589-7

BASE COAT WT .59  
TOP COAT 1 .19  
TOP COAT 2 .18  
PHOSPHOR WEIGHT 4.17  
SHEET RESISTANCE 118

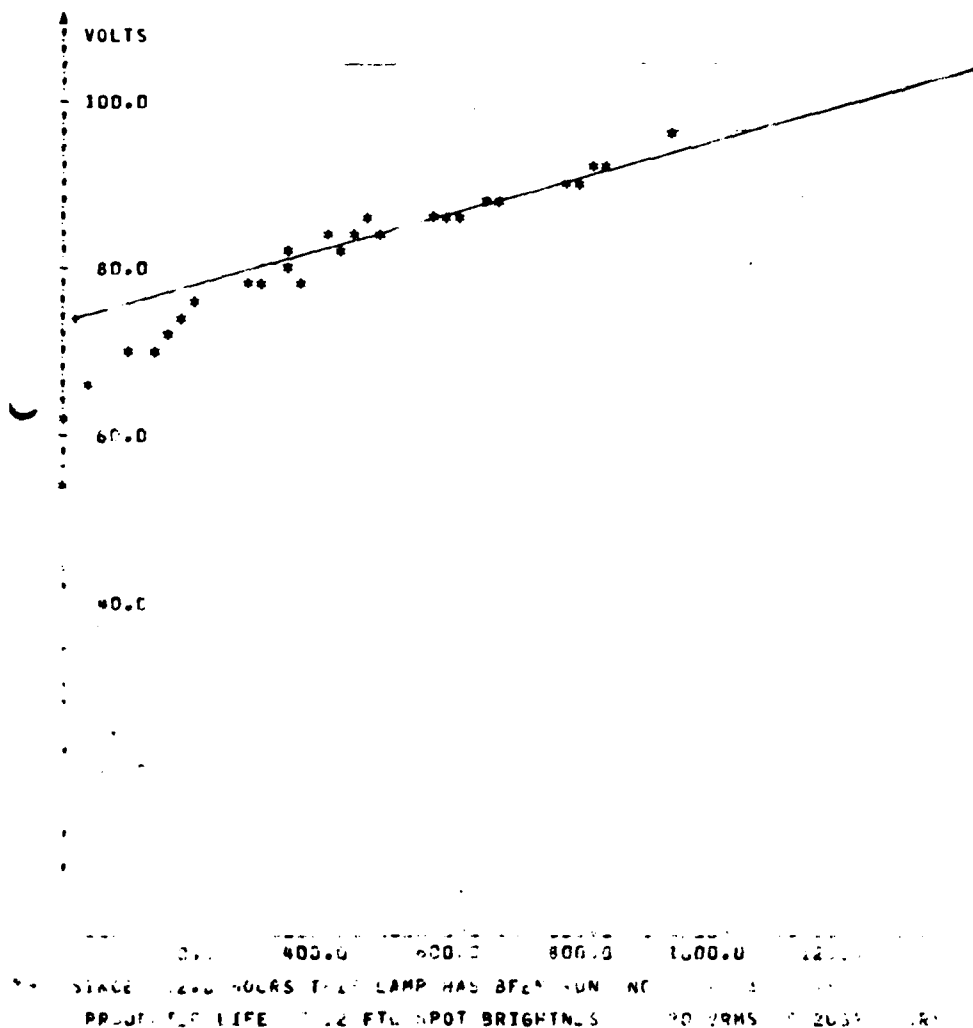


Figure 7.71

Computer analysis of life testing of postage stamp  
Device No. 589-9 in an experiment to determine  
effect of ambient temperature on maintenance.

UPDATE 5-30-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

589-3  
POSTAGE STAMP  
3.6

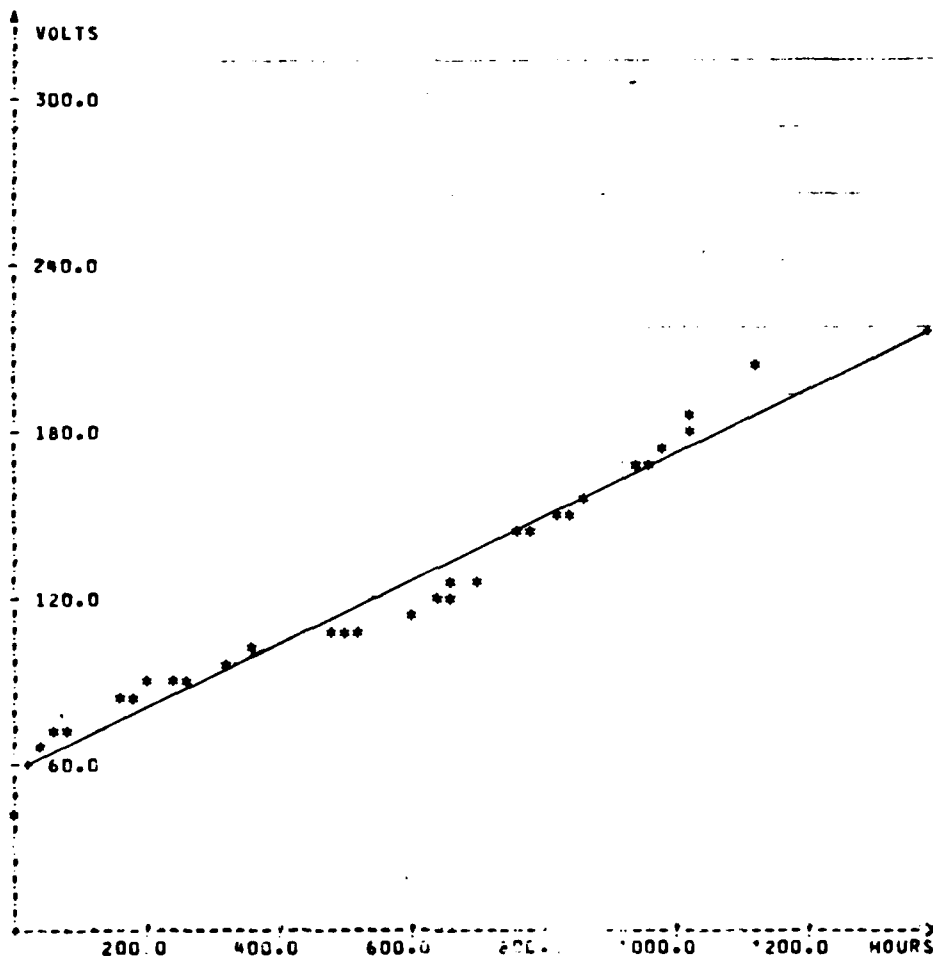
FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-16-79  
AIR  
50C

589-3,4 ON HEAT SINK  
WITH PASTE. ALL 4  
STAMPS (589-5,6) ENCAPPED.  
WITH SILICONE ONLY - NO  
POLYSULFIDE. 5KHZ SINE.

BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE

.64  
.21  
.23  
4.02  
94



SINCE 98.0 HOURS THIS LAMP HAS BEEN RUNNING AT 8.8 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 525 HOURS

Figure 7.72

Computer analysis of life testing of postage stamp  
Device No. 589-3 in an experiment to determine  
effect of ambient temperature on maintenance.



UPDATE 5-30-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

589-4  
POSTAGE STAMP  
3.6

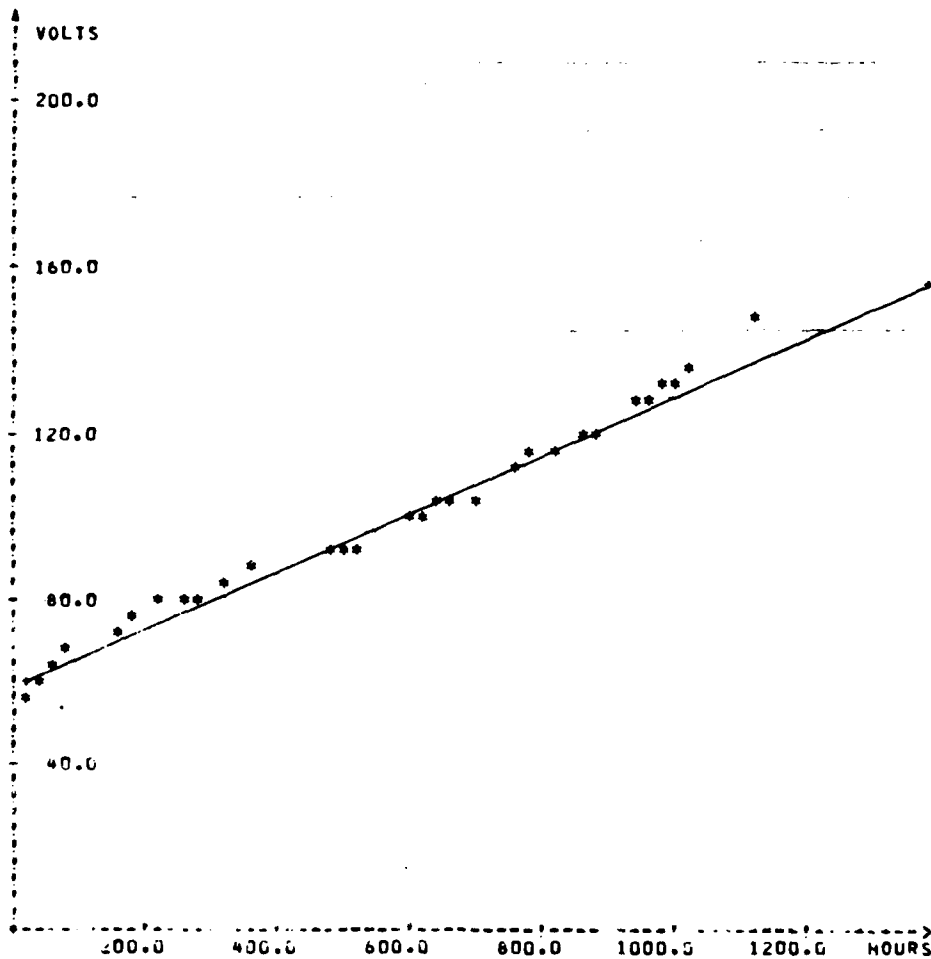
FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-16-79  
AIR  
50C

SAME AS 589-4

BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE

.64  
.21  
.23  
4.02  
90



SINCE 12.0 HOURS THIS LAMP HAS BEEN RUNNING AT 14.2 HOURS PER VOLT  
PROJECTED LIFE AT 12 FTI SPOT BRIGHTNESS & 120 VRMS IS 820 HOURS

Figure 7.73

Computer analysis of life testing of postage stamp  
Device No. 589-4 in an experiment to determine  
effect of ambient temperature on maintenance.

UPDATE 6-5-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

589-5  
POSTAGE STAMP  
3.6

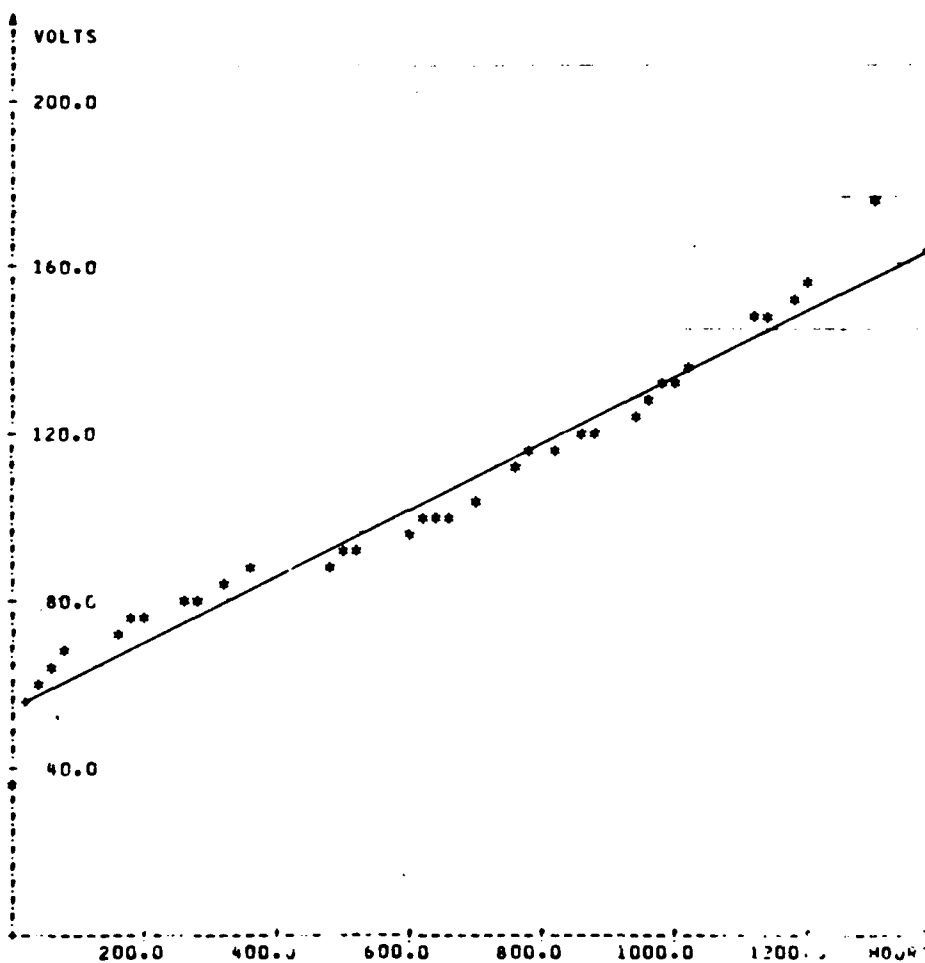
FIGURING BOOK REFERENCE  
DATE FABRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-16-79  
AIR  
50C

589-5,6 SAME AS  
589-2,3 EXCEPT  
NO HEAT SINKING  
NOTE LOWER  
TEMPERATURE

BASE COAT WT  
TOP COAT 1  
TOP COAT 2  
PHOSPHOR WEIGHT  
SHEET RESISTANCE

.64  
.21  
.23  
4.02  
100



SINCE 48.0 HOURS HIS LAMP HAS BEEN RUNNING AT 12.0 HOURS PER VOL  
PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 120 VRMS IS 797 HOURS

Figure 7.74

Computer analysis of life testing of postage stamp  
Device No. 589-5 in an experiment to determine  
effect of ambient temperature on maintenance.

UPDATE 6-5-79

SAMPLE NUMBER  
SAMPLE TYPE  
OVEN NUMBER  
BRIGHTNESS

POSTAGE 589-8  
STAMP 2  
3.6

FIGURING BOOK REFERENCE  
DATE FARRICATED  
TEST AMBIENT  
TEST TEMPERATURE

NA  
4-25-79  
VAC  
25C

SAME AS 589-7

BASE COAT WT .59  
TOP COAT 1 .19  
TOP COAT 2 .18  
PHOSPHOR WEIGHT 4.17  
SHEET RESISTANCE 160

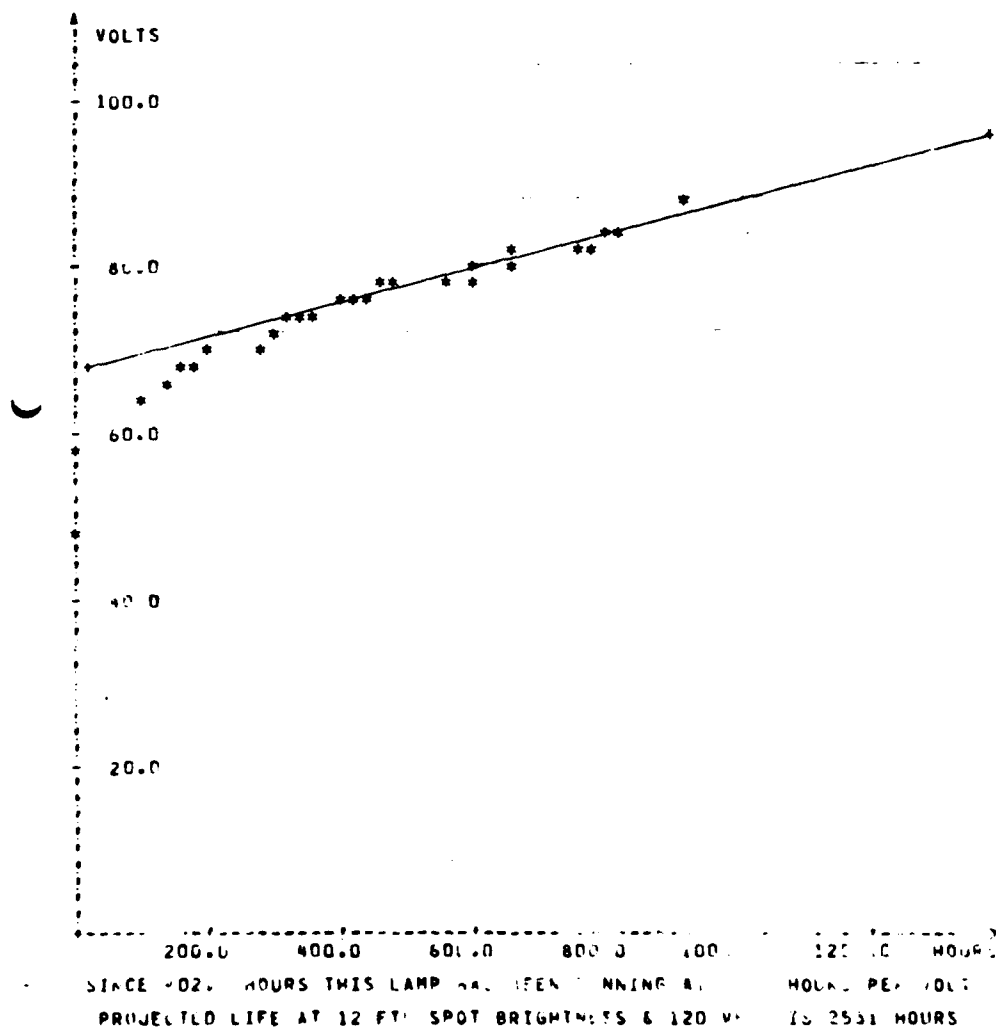


Figure 7.75

Computer analysis of life testing of postage stamp Device No. 589-6 in an experiment to determine effect of ambient temperature on maintenance.

Curve 715879-A

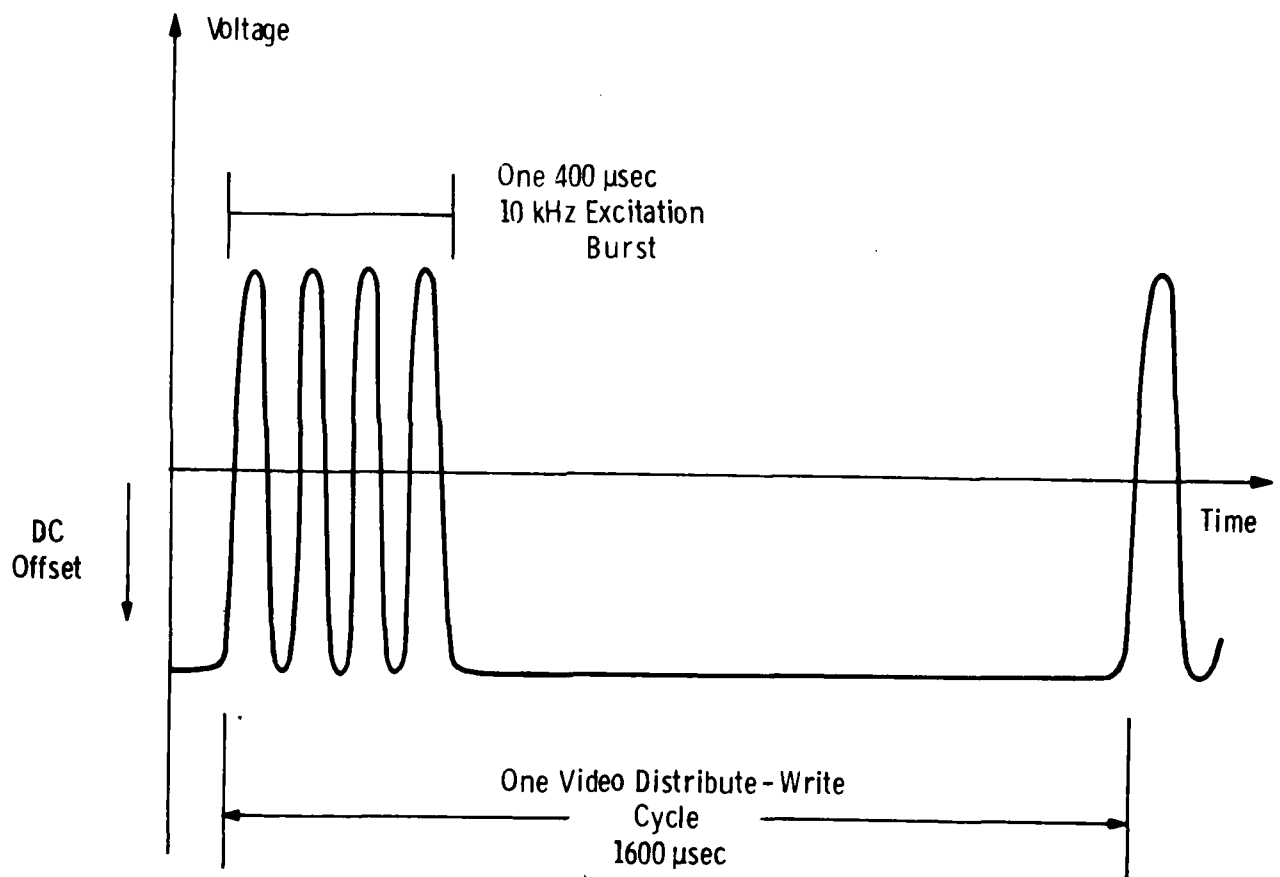


Figure 7.76 Waveform used to test luminance vs brightness of the new powder phosphor layers in a mode planned for the new exercisers

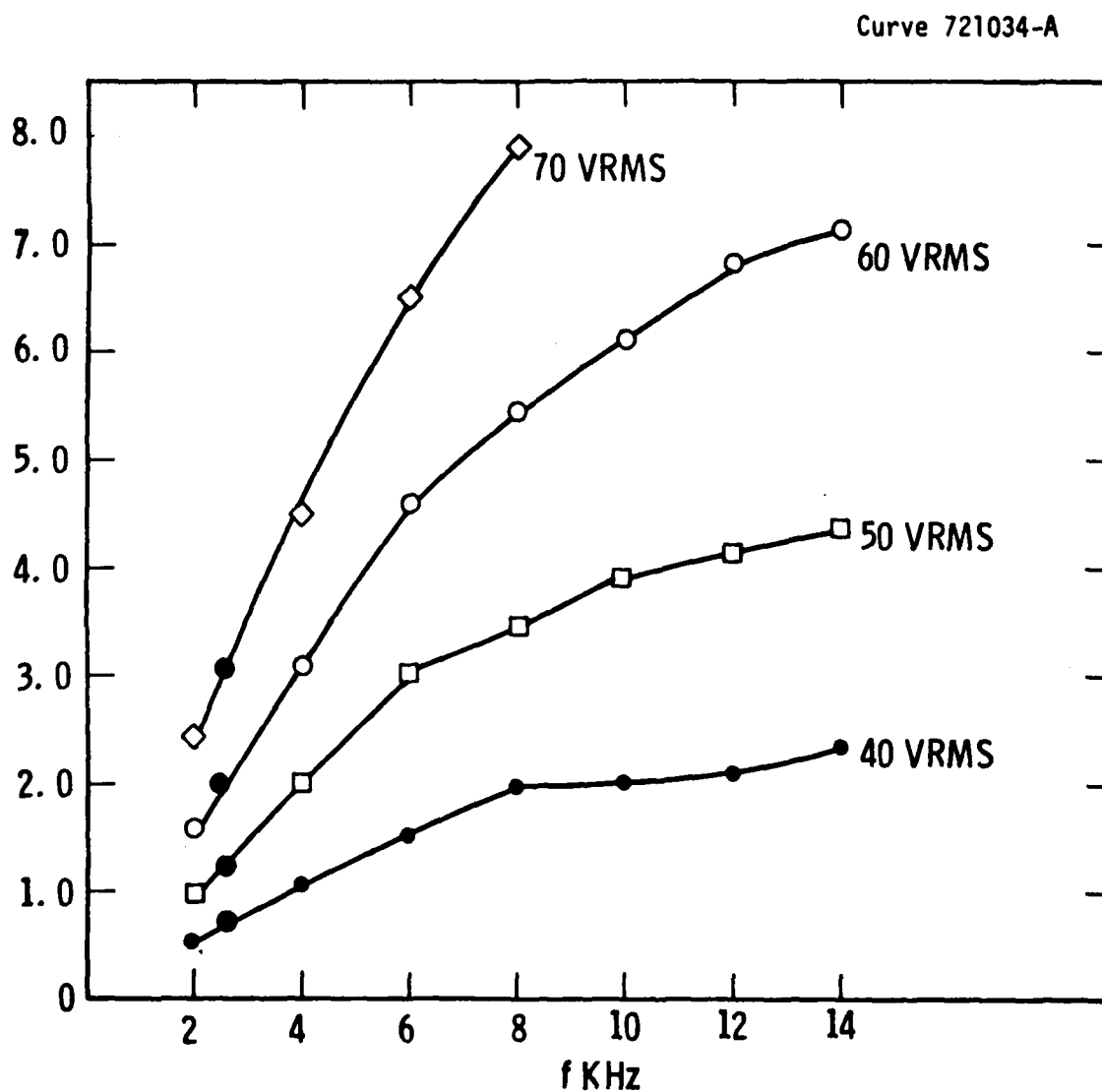


Figure 7.77 Powder phosphor performance as a function of sinusoidal frequency and voltage (first of two samples).

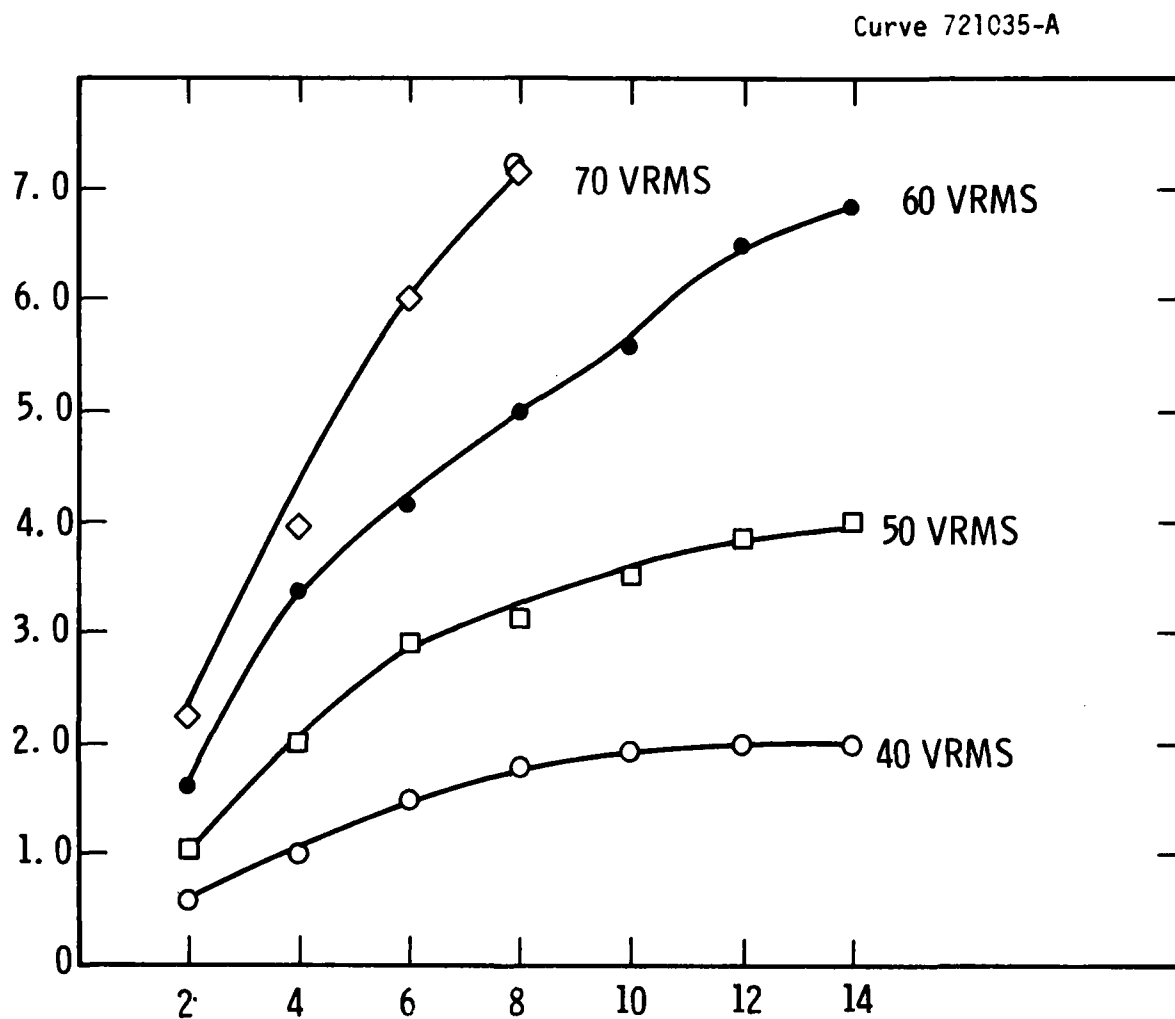


Figure 7.7 Powder phosphor performance as a function of sinusoidal frequency and voltage (second of two samples).

Curve 720668-A

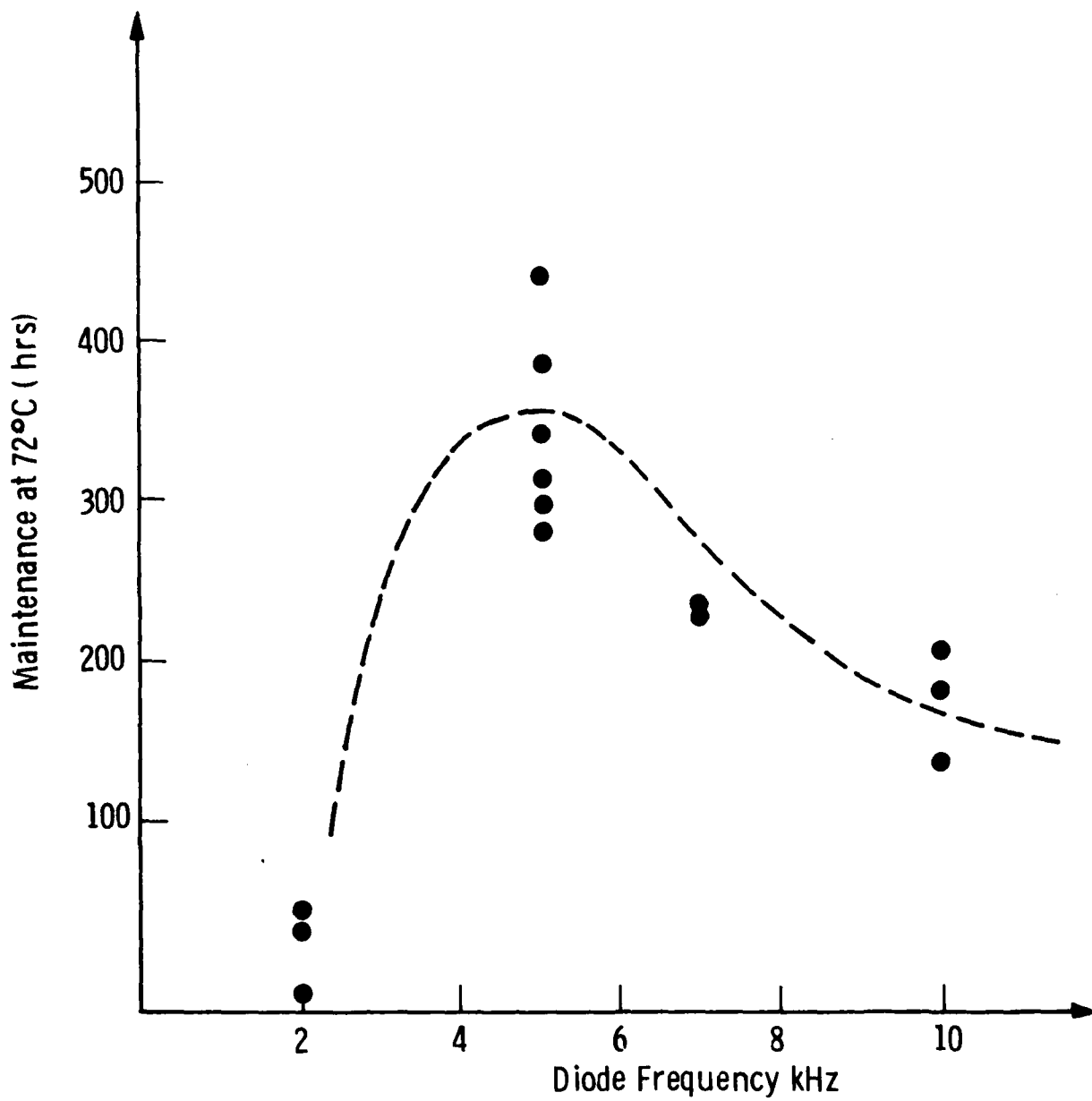


Figure 7.70 Behavior of maintenance with excitation voltage frequency at 72°C.

Curve 715879-A

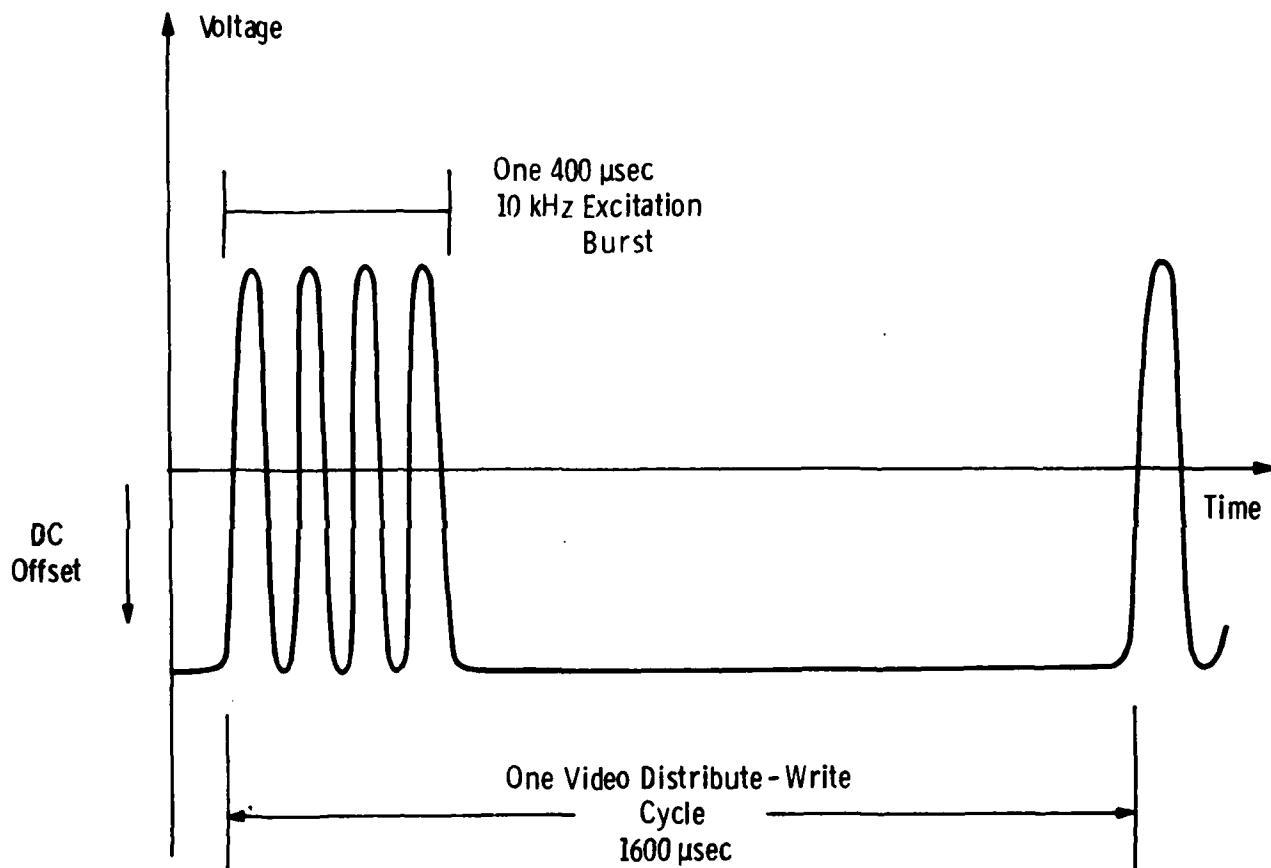


Figure 7.80 Waveform used to test brightness versus peak-to-peak voltage for two samples in the burst waveform mode.



#### 7.5.4 Summary of Phosphor Layer and Related Encapsulation Technology Development

In Table 7.12 we summarize procedural changes and attendant results resulting from activity executed during program Phases II and III. This was directed almost exclusively at catastrophic failures experienced with prior art during 72°C life testing.

Other relatively minor but beneficial procedural details and changes not discussed here are incorporated into the final formulation of the processes discussed in the next section, for phosphor layers, and in Section 8.2 for encapsulation.

TABLE 7.11 Comparison of the life testing performances of similarly constructed postage stamp devices at three different temperatures. (Maintenance is defined as usual in terms of a 120 V<sub>rms</sub> maximum excitation voltage).

Sample No.	Figure No.	Test		Configuration	Fabrication Parameters			Performance			
		Temp.	Ambient		Total Plastic Weight mg/cm <sup>2</sup>	Phosphor Weight mg/cm <sup>2</sup>	Top Electrode Resistivity $\Omega$ /sq	Inverse Degradation Rate (hr/v)	Main-tenance (hr)	Threshold Voltage V <sub>T</sub>	Duration of Test (hr)
589-7	7.60	25°C	Vacuum	No encapsulation	.96	4.17	200	42.5	2066	70	890
589-8	7.70				.96	4.17	160	49.1	2531	70	900
589-9	7.71				.96	4.17	118	45.3	2052	75	950
589-3	7.72	50°C	Air	Encapsulated	1.08	4.02	94	8.8	525	60	1100
589-4	7.73			with Silicone RTV & covered and fitted with heat sink	1.08	4.02	90	14.2	820	60	1100
589-5	7.74	50°C	Air	Same as 589-3,4	1.08	4.02	100	12.8	797	60	1250
589-6	7.75			but no heat sink	1.08	4.02	90	18.0	1106	60	1250
583-4	7.76	72°C	Air	Same as 589-3,4	1.34	4.10	230	5.6	313	60	470
583-5	7.77				1.05	4.08	400	4.6	280	60	420
583-6	7.78				1.12	4.05	175	4.5	297	55	580

TABLE 7.12      Summary of Procedural Changes and  
Resultant Benefits Derived from  
Phosphor Layer and Encapsulation  
Development Activity

	Prior Art	Program Devel. Art
Phosphor Layer Fabrication		
Binder	CE:S&S	CE:PVA
Phosphor	Same Westinghouse Phosphor	
Top Electrode	Au	Au
Top Electrode Base	PbO	CdF
Phosphor Application	Spray	Hybrid Brush-Spray
Encapsulation		
Epoxy	Stycast 1266	Silicone RTV
Edge Seal	Polysulfide	None
Performance at 12 ft-L		
72°C	< 4 hrs	350 hrs
50°C	not known	900 hrs
25°C	not known	2500 hrs

TABLE 7.13 Observed Variation of Maintenance with Frequency

Sample No.	Drive Frequency	Maintenance to 120 V <sub>rms</sub> Maximum in hours
584-1	2 kHz	39
584-2	↓	5
584-3		48
583-1	5 kHz	445
583-2	↓	382
583-3		340
583-4		313
583-5		280
583-6	↓	297
584-7	7 kHz	226
584-8	7 kHz	227
584-4	10 kHz	137
584-5	↓	180
584-6		203

## 7.6 Final Procedure for Phosphor Application

### 7.6.1 Phosphor Brushing

For Phosphor Brushing, the equipment and materials needed are as follows:

- Hot plate
- Copper heat sink 6" x 6" x 1"
- Thermocouple bridge
- Vacuum oven
- Spray booth DeVilbiss Type DXF
- Spray gun DeVilbiss Type MBC-510
- Spray shuttle
- Balance Volland and Sonc, Inc. Model 640-D
- PVA Made in Dept.
- Phosphor 11212B Made in Dept.
- Brush 3/4" Delta 1517
- Q-Tips
- Acetone
- Spray plate Alum. 12" x 12" x 1/8"
- MEK
- Dry box (2)
- Double back tape
- #27 alligator clips (2)
- Single edge razor blades

## Process

To begin the sequence of phosphor brushing, the nitrogen supply to the spray gun should be turned "on", followed by the turning "on" of the shuttle control. Then the air ventilation for the spray booth is opened and the spar jar containing PVA is attached to the gun. The next step is to set the spray gun fan, and then the spray gun needle. After that, the spray gun is actuated to observe flow and pattern of PVA sprayed from gun.

The spraying fixture and the spray gun are important elements of the process and hence warrant a brief description. The spraying fixture is a plate attached by cable to a reversible DC motor. Two limit switches at the end of travel in each direction reverse the motor for the next sequence. When the start button is depressed the plate moves from right to left and stops. When the start button is depressed again the plate moves from left to right. This allows the panel to move at a given speed across the path of the spray gun.

The spray gun is attached to a vertical post 8-1/2 inches from the spraying plate. The vertical post has holes located at 3/4" intervals and allows the gun to be moved up and down within these intervals. The top knurled knob on the gun is the fan knob. The lower knurled knob on the gun is the needle valve and is varied according to the layer being sprayed. The position of this knob is recorded in "O'clock" positions. Figure 1 shows fixture and gun arrangement.

Once the spraying routine is over, each half DMD panel is weighed and the weight is recorded as mass  $O(M_o)$  in the spraying tag. Then a strip of half-inch double-backed tape is placed approximately two inches above center, horizontally across the spraying plate. Next, each half DMD is placed on the double-backed tape with the batting edge down. In order to remove the DMD, however, only the width of the top edge fingers should be placed on the tape. The half DMD(s) to be sprayed is/are then blown with ionized nitrogen in order to remove particulate matter. The next step is the clipping--with two #27 alligator

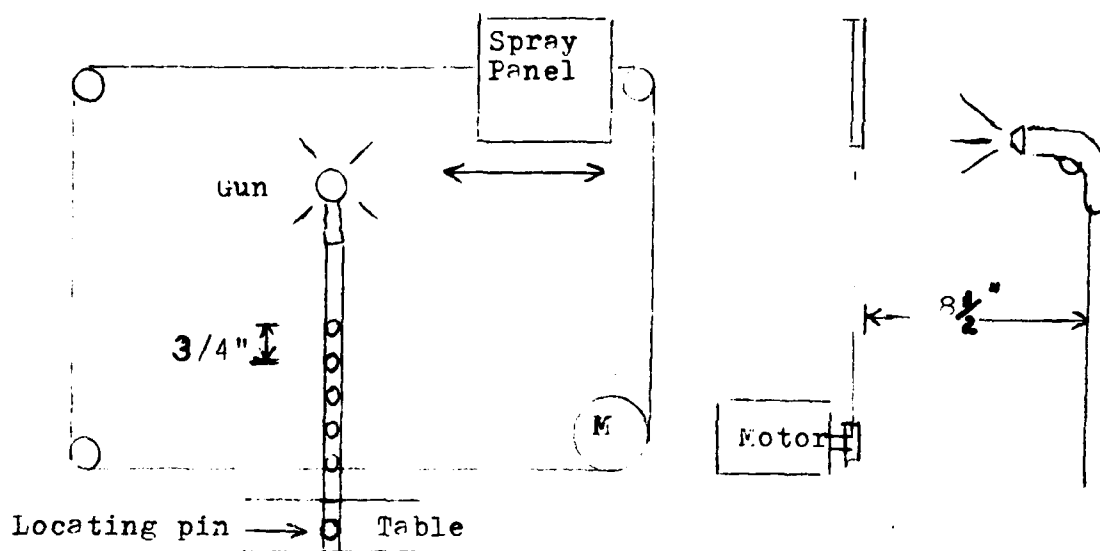


Figure 7.81

clips--of the spraying plate (with the half DMD s taped to it) to the spray shuttle. To spray on the top of the half DMDs, a spray gun is placed vertically about 1-1/2" above the DMDs, and the spray shuttle is actuated by pressing the "red" start button; the spray shuttle will then move across the field of spray.

As the shuttle enters the field of the spray, the spray gun commences disseminating a strip across the attached half DMD(s). After each pass; the spray gun is lowered, and a succeeding pass is begun. When the entire surface of the half DMD(s) is sprayed, the shuttle is stopped and the spray panel is unclipped.

The next step is the placement of the sprayed panel (with the half DMDs in a vacuum oven and its baking in ambient nitrogen. After each spraying, the spray jar with PVA is removed, capped, and stored in a nitrogen atmosphere "dry box" to ensure dryness of the material. The spray gun is then cleaned by passing MEK through the gun, ejecting some, and then allowing the gun to dry.\* When the specified nitrogen

\* The procedure outlined in the preceeding two paragraphs up to this point is repeated again in the process of phosphor application.

bake is over, the vacuum oven is put into vacuum condition (see process specification for vacuum bake time and temperature). The spray panels of the half DMDs are removed from vacuum and allowed to cool. Once cool, the half DMD(s) is/are removed from the spray panel and weighed again. This new weight is recorded as Mass 1 ( $M_1$ ) in the spray log. Mass 0 is subtracted from Mass 1 and the weight of the base coat is derived.

Following the preparation of the DMD panels is the process of the actual phosphor brushing. This procedure is listed below.

#### Procedure for Phosphor Brushing

- A hot plate is heated until specified temperature is reached as measured by a thermocouple and the thermocouple bridge. (See process description for specified temperature.)
- Each half DMD is put on a piece of paper 5-1/2" x 8-1/2".
- The phosphor is placed in the center of the half DMD and evenly distributed over the surface with a 3/4" brush. (See process specification for phosphor type.)
- The paper, with the half DMD on it, is then placed on the hot plate.
- After a span of 15 seconds the 3/4" brush is applied for distributing the phosphor over the surface of the half DMD.
- The excess phosphor is removed by:
  - a. Brushing horizontally across half DMD with 3/4" brush at 3/4" intervals.
  - b. Brushing vertically in the same way as in (a).
  - c. Brushing diagonally in the same way as in (a) from right to left.
  - d. Brushing diagonally in the same way as in (a) from left to right.
  - e. A final brushing as in (a) above.
- The paper and the half DMD is removed from the hot plate and placed on a copper heat sink.



- When the half DMD is cool, the excess phosphor is brushed off with a 3/4" brush and the panel is blown with ionized nitrogen to remove final particles of phosphor.
- The half DMD(s) is/are then placed in the vacuum oven and baked in nitrogen atmosphere. (See process specifications for nitrogen bake time and temperature.) After a specified nitrogen bake time, the oven is put in vacuum condition. (See process specifications for vacuum bake time and temperature.)
- When the specified vacuum bake is over, the half DMD(s) is/are placed in a nitrogen atmosphere dry box and allowed to cool. On completion of the cooling, the half DMD(s) is/are weighed and recorded in the spray log as mass-phosphor ( $M_{\text{phos}}$ ).  $M_1$  is subtracted from  $M_{\text{phos}}$  to derive phosphor coat weight.
- Top Coat 1 is now applied to the half DMD(s). The process following the spraying routine (see footnote p481)--until the cleaning of the spray gun is repeated. (See process specification for settings and time.)
- After the specified nitrogen bake the half DMD(s) is/are removed from spray plate and cooled in dry box and weighed. The weight is recorded as Mass 2 ( $M_2$ ).  $M_{\text{phos}}$  is subtracted from  $M_2$  to derive Top Coat 1 weight.
- Top Coat 2 is then applied to the half DMD(s). Steps following the spraying routine are as explained in pp 480-81(see footnote p481) are repeated. (See process specification for settings and time.)
- After specified vacuum bake the half DMD(s) is/are removed from spray plate and cooled in nitrogen atmosphere dry box. The half DMD(s) is then weighed and the weight recorded in the spray log as Mass 3 ( $M_3$ ).  $M_3 - M_2$  = Top Coat 2 weight.
- The edge contacts are cleaned and the PVA and phosphor are removed. A Q-tip is dipped in Acetone and the excess is wiped off. The Q-tip is then used to remove carefully the PVA-Phosphor back to the Riston

borders. As each Q-tip collects the PVA-Phosphor, a new one is used to prevent build-up. When all three edge contact sides are clean a dry Q-tip is used to remove Acetone residuals.

- The edges of the half-DMD(s) is/are cleaned with a Q-tip and acetone.
- The back of the half DMD(s) is scrapped clean with a single edge razor blade.
- All surfaces of the half DMD(s) is/are blown with ionized nitrogen to remove particulate matter.
- The half DMD(s) is/are now ready for conductive epoxy application.
- Weights recorded in the spray log are now converted to  $\text{mg}/\text{cm}^2$ . A typical example of the conversion to  $\text{mg}/\text{cm}^2$  is discussed as follows:

A. Weight in grams as recorded from balance

$$\begin{array}{ccccc} \frac{M_o}{24.6615} & \frac{M_1}{24.7072} & \frac{M_{\text{phos}}}{25.0243} & \frac{M_2}{25.0444} & \frac{M_3}{25.0643} \end{array}$$

B. Weight of each material layer

$$\begin{array}{cccc} \frac{M_1}{24.7072} & \frac{M_{\text{phos}}}{25.0243} & \frac{M_2}{25.0555} & \frac{M_3}{25.0643} \\ \frac{24.6615}{457} & \frac{24.7072}{3171} & \frac{25.0243}{201} & \frac{25.0444}{199} \end{array}$$

Convert to milligrams by placing decimal to left of last digit on right.

$$\begin{array}{cccc} 45.7 & 317.1 & 20.1 & 19.9 \end{array}$$

C. Derive  $\text{mg}/\text{cm}^2$  by the formula:  $\frac{\text{Weight}}{\text{Area}} = \text{mg}/\text{cm}^2$

Weight = each layer weight converted to mg.

Area = average area of half DMD =  $78.3 \text{ cm}^2$

$$\frac{45.7}{78.3} = .58 \text{ mg}/\text{cm}^2 \quad \frac{317.1}{78.3} = 4.05 \text{ mg}/\text{cm}^2 \quad \frac{20.1}{78.3} = .26 \text{ mg}/\text{cm}^2$$

$$\frac{19.9}{78.3} = .25 \text{ mg}/\text{cm}^2$$

Spray Log Entries (see samples)

Before, during, and after phosphor brushing entries are made in the spray log.

Before spraying

- A. No. = next highest number in book
- B. Date = present date
- C. Spray or silk screen = sp.
- D. Distance (from gun to panel) = 8 1/2"
- E. Gun type = 2
- F. Fan = 1/2 turn
- G. Pressure = 22 lbs
- H. Gear = 2
- I. Voltage = 80%
- J. Indexing = 1 1/2"
- K. Baking = 100 C

During Spraying

		<u>Remarks</u>	<u>Weight</u>
A. Layer #1	Needle = 10 o'clock	30 min nitrogen	M <sub>1</sub>
		60 min VAC	
B. Layer #2	Needle = 2 o'clock	30 min nitrogen	M <sub>2</sub>
C. Layer #3	Needle = 2 o'clock	30 min nitrogen	M <sub>3</sub>
		60 min VAC	

After Spraying

- A. Perform weight calculations as described in 46°C and shown in spray log entry sample (Table 7.14).

NO. 605

Table 7.14

DATE 6-25-79

[illegible]

Table 7.15

## Sample Spray Log Entry

605

	$M_o$	$M_1$	$M_{p \text{ Los}}$	$M_2$	$M_3$
9169-5	24.6615	24.7072	25.0243	25.0444	25.0643
9169-7	24.6378	24.6817	25.0000	25.0213	25.0400

	$M_1$	$M_{p \text{ Los}}$	$M_2$	$M_3$
9169-5	24.7072	25.0243	25.0444	25.0643
	<u>24.6615</u>	<u>24.7072</u>	<u>25.0243</u>	<u>25.0444</u>
	45.7	317.1	20.1	19.9
	.58 mg/cm <sup>2</sup>	4.05 mg/cm <sup>2</sup>	.26 mg/cm <sup>2</sup>	.25 mg/cm <sup>2</sup>
9169-7	24.6817	25.0000	25.0213	25.0400
	<u>24.6378</u>	<u>24.6817</u>	<u>25.0000</u>	<u>25.0213</u>
	43.9	318.3	21.3	18.7
	.56 mg/cm <sup>2</sup>	4.07 mg/cm <sup>2</sup>	.27 mg/cm <sup>2</sup>	.24 mg/cm <sup>2</sup>

TABLE 7.16

## D. Process Specification Information

Present Specifications

Rev. 1

Rev. 2

Rev. 3

1. Spray gun nitrogen supply:  
Pressure: 30 lbs. psi
2. Shuttle control:  
Clutch: on      Gear: 2  
Speed variac: 80%
3. PUA material:  
Recepie: LC 37108
4. Spray gun fan: #2 gun  
Setting: 1/2 turn open    Press: 22 lbs.
5. Spray gun needle valve:  

	Base	Top C.1	Top C.2
Setting(o'clock):	10	2	2
6. Spray gun vertical movement intervals:  
distance each shuttle pass: 1 1/2"
7. Nitrogen Bake: (post-base coat)  
Time: 30 min  
Temp: 100°C
8. Vacuum Bake: (post-base coat)  
Time: 60 min.  
Temp.: 100°C
9. Phosphic Brushing hot plate:  
Temp: 160°C
10. Phosphor:  
Recipie: WL 11212
11. Post phosphor bake:

	<u>Nitrogen</u>	<u>Vacuum</u>
Time	30 min	60 min
Temp.	100 C	100 C
12. Post Top Coat 1 Bake  
Nitrogen only  
Time: 30 min  
Temp: 100 C
13. Post Top Coat 2 Bake:

	<u>Nitrogen</u>	<u>Vacuum</u>
Time:	30 min	60 min
Temp:	100 C	100 C

#### 7.6.2 Conductive Epoxy Application

A. Equipment and materials needed for the application of epoxy are the following:

Balance	Fisher Scientific
Conductive Epoxy	Emerson & Cuming Inc.
	Eccobond Solder V-91
Tape	
Q-Tips	
VAC-Oven	
Alum. weighing dishes	

#### Process

The fundamental step in the epoxy application lies in the proper mixing of epoxy as outlined in the process specifications.

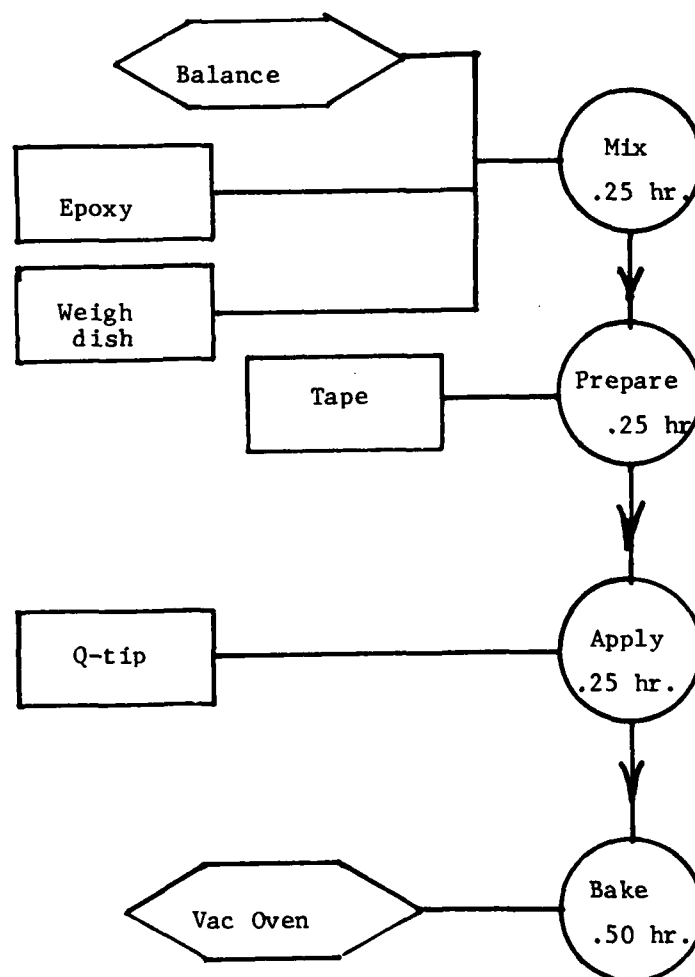
The half DMD s are then marked with phototape which is applied horizontally across the power finger side of the half DMD(s). The bottom edge of the tape is located approximately .015" above the phosphor edge.

A strip of tape is also applied horizontally across the power finger side of the half DMD. The top edge of the tape is located approximately .050" below the first strip of tape.

Conductive epoxy is then applied between the two strips of tape with a Q-tip that enables epoxy application. The conductive epoxy is then spread between the second and fifteenth blocks.

Following this step, the two strips of tape are peeled off and the panel is then baked in a nitrogen atmosphere (the process specifications).

The process time and flow information are delineated in Figure 7.82 and the process specification in Table 7.17.



Process Time

Mix	.25 hr.
Prepare DMD	.25 hr.
Apply	.25 hr.
Bake	.50 hr.
	<u>1.25 hr.</u>

Figure 7.82. Process time and Flow Information



TABLE 7.17

PROCESS SPECIFICATION

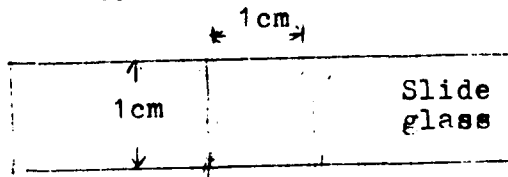
1. Conductive Epoxy  
Emerson & Cuming  
Eccobond V-91  
Mixed 5:1
2. Bake  
30 min. in nitrogen atmosphere

### Top Electrode Evaporation Fixture

DMD 1/2 panels to be processed for the top electrode are installed in the top electrode evaporation fixture. There are two types of fixtures: one for single 1/2 panels and one for double 1/2 panels. Both types of fixtures contain a recessed area the size of the intended panel(s) to be processed. Before installing the panel(s) into the fixture the ground contact on the panel is protected by covering with tape. After inserting panel(s) into fixture, the locating slides are set against the panel edges and locked into place. The masking edges are then placed over the edge contacts and locked into place. These edges protect the edge contacts on the panel(s) from evaporated  $\text{CdF}_2\text{-Au}$ . The top electrode evaporation fixture is now ready to be installed into the vacuum system.

### Evaporation of Top Electrode

1. The top electrode evaporation fixture clipped to the holding fixture in the laboratory vacuum system.
2. The  $\text{CdF}_2$  source is loaded with  $\text{CdF}_2$ . The Au source is checked for sufficient material.
3. A slide glass with two wires attached by conductive epoxy at 1 cm distance apart is clipped to holder and wires attached to internal leads.



4. The vacuum system is closed and pump down begun.
5. Evaporation is begun once vacuum reaches  $2.0 \times 10^{-6}$ .
6. The  $\text{CdF}_2$  source is connected and the variac is increased from 0 to 30% in 1 min. When a frequency shift of 200 cycles is observed the shutter is opened. When a 600 cycle frequency shift is observed the shutter is closed and the variac returned to zero. Details are recorded on the vacuum log form.

7. The Au source is then connected and the variac increased from 0 to 30% in 1 min. The shutter is opened at a frequency shift of 200 cycles and the ohm meter is observed. This meter is connected to the slide glass inside the vacuum. When the meter reads 30 ohms the shutter is closed and the variac returned to zero. The thickness is approx.: 1000 angstroms. Details are recorded on the vacuum log form.
8. The  $\text{CdF}_2$  source is once again energized and the variac set to 45% in 1 min. to clean the source. Details are recorded on the vacuum log form.
9. After enough time to cool the sources, the system is let up to atmosphere.
10. The panel(s) are removed from the vacuum system and coated with one wet coat of krylon clear spray point.
11. The DMD panel(s) is/are baked @  $90^\circ\text{C}$  for 15 min. to cure coat of Krylon.
12. The DMD panel(s) is/are removed from the top electrode evaporation fixture and the protective tape removed from the ground contacts.
13. The DMD panel(s) is/are now ready for pre-packaging testing.

### Materials and Equipment Needed for Top Electrode Procedure

- a) Vacuum system with holding fixture for DMD, panels
- b)  $\text{CdF}_2$  (Cadmium Fluoride)
- c) Au (Gold)
- d) Slide monitor (made in dept.)
- e) Multimeter
- f) Rate monitor - thickness monitor
- g) Krylon Clear paint.
- h) Oven
- i) Top electrode evaporation fixture

This process is outlined in Table 7.18.

TABLE 7.18

<u>Process Step</u>	<u>Equipment Needed</u>	<u>Est. Time</u>
1. Install panel(s) load sources attach slide	vacuum system, balance, slide glass monitor	1/4
2. Close system and pump down		Timed to pump over night.
3. Evaporations performed	rate monitor, ohmmeter	1/4
4. Cool down - let up at atmosphere		1/4
5. Spray panel(s) with krylon clear paint. Bake		1/4

Step 2 is timed so that  
an over-night pumpdown  
is allowed

TOTAL TIME: 1 hour

## 8. ENCAPSULATION

### 8.1 Panel Selection Procedure

After application of the electroluminescent powder and top electrode, each half panel was subjected to a viewability test, which determined the general panel characteristics and the defect count. The test fixture used enables the seaprate adjustment of source and gate voltages, as well as the a.c. voltage applied to the electroluminescent powder.

An arbitrary value of approximately 100 volts R.M.S. was applied to the electroluminescent powder and the bias voltages were adjusted in order to achieve optimum viewability with the lowest possible voltage. Pictures were then taken of the half panel with all elements on, all elements off, and all 5 x 7 dot patterns displaying the number eight.

The results of these measurements are shown in Table A and the voltages applied are listed along with a repair column. The - ANY - comment indicates a poor half-panel in which the bias adjustment has very little effect. The repair column indicates whether any repairs were made to the half panel after the application of the phosphor layer.

The pictures were used to select the fourteen "best" half panels. The best determination was a completely subjective evaluation of the defect count. Once these fourteen panels were chosen on bias voltages, they were matched according to the bias voltages.

The paired panels were then mounted in a test fixture. Again, an arbitrary a.c. voltage at 100 V R.M.S. was applied and the biases adjusted for optimum viewability. Then better pictures were taken with all elements on, all elements off, and each 5 x 7 pattern displaying the number 8. At this point, it became obvious that the brightness variation

TABLE A

Display Number	Repaired		Bias Voltages				EL
	Yes	No	S+	S-	B+	B-	
9169-7		X	10	6	10	11	100
9169-5		X	6	9	8	20	100
9159-6		X	5	5	7	11	90
9159-4		X	10	10	7	17	90
9159-3		X	8	1	8	11	90
9156-5		X	6	4	20	11	90
9156-4		X	7	1	22	11	90
9156-2		X	9	10	3	19	90
9151-5	X		10	5	12	15	80
9151-4	X		5	2	18	17	100
9151-3		X	7	5	4	10	100
9151-1		X	10	6	3	21	50
9131-4		X	13	2	8	14	90
9124-6		X		ANY			100
9124-2		X	9	10	12	16	100
9100-8	X		8	6	10	16	100
9079-2		X	10	5	9	10	100
9073-3		X	9	8	8	9	100
9072-2		X	8	6	14	11	100
9044-2		X	8	3	18	14	100
8342-3		X	5	4	13	5	100
8291-8		X	7	7	20	12	100
8291-6	X		3	7	11	15	100
			2	5	15	13	100
8290-5		X	3	11	8	19	100
			3	14	15	14	100
8277-3	MISSING		13	14	15	19	100
8270-2		X	6	5	14	13	100
8269-4	X		11	12	8	18	100
			12	10	7	17	100

TABLE A (con't.)

Display Number	Repaired		S+	S-	Bias Voltages		EL
	Yes	No			B+	B-	
8268-5		X	14	1	17	11	100
8261-4		X	9	4	12	12	100
8248-6	X		10	4	3	13	100
8248-3	X		7	5	8	11	100
8244-1		X	12	4	29	14	100
8241-3		X	7	47	24	21	100
8235-4	X		7	6	22	10	100
8228-8	X		4	6	11	12	100
8227-3		X	13	1	27	16	90
8227-2		X	4	7	7	12	100
8226-5		X		ANY			100
8219-4		X	6	9	5	20	100
8216-2	X		6	10	13	20	100
8205-4	X		6	11	15	19	100
8202-1	X		3	5	3	11	100
8199-5	X		14	1	8	14	100
8150-1		X	4	9	2	20	100
8138-1		X	3	11	12	20	100

in the half panels needed to be considered. This brightness difference was a result of the application of different electroluminescent phosphor mixtures in varying thicknesses.

Table B shows the results of this test. The table contains the original bias voltages used on the half panels as well as the actual values used on the combination. A column for a relative brightness measurement was added at this stage.

As previously mentioned the brightness of the individual half panels proved to be a very significant matching parameter. It should be noted that this brightness is a strong function of voltage and that the values listed in the table are for matching purposed only. The actual brightness could be equalized by a slight voltage adjustment. Unfortunately, the separate adjustment of half panel phosphor voltage was not a capability of our tester. Keeping this in mind, we arranged the panels according to brightness and conducted another set of tests, results of which appear in Table C.

The bias voltages, a.c. voltages, and brightness values for individual panels are taken from the previous test data, but are listed here for the sake of comparison. The actual voltages used for the combination are given. No brightness measurements were performed on the combinations. Since the relative brightnesses was equal, the actual brightness was just a function of voltage.

The matched pairs in Table C represent the final pairing. These panels were packaged as listed. In addition, 10 half panels were previously packaged; their panel numbers and bias voltages appear in Table D. Thus a total of 20 half panels or 10 full panels were packaged.



TABLE B  
SUGGESTED COMBINATIONS BIAS

	S+	S-	G+	G-	EL	B
8-138-1	3	11	12	20	100	.35
8-216-2	6	10	13	20	100	.15
Combination	7	11	9	20	90	
8-219-4	6	9	5	20	100	.22
8-228-8	4	6	11	12	100	.275
Combination	8	10	9	20	100	
8-247-3	7	5	8	11	100	.15
8-248-6	10	4	3	13	100	.11
Combination	7	11	8	19	90	
9-151-4	5	2	14	17	100	.63
9-156-5	6	4	20	11	90	1.13
Combination	8	9	8	16	90	
9-151-5	10	5	12	15	100	.74
9-159-4	10	10	7	17	90	1.1
Combination	9	7	6	20	90	
9-156-2	9	10	3	19	90	.72
9-169-7	10	6	10	11	100	1.25
Combination	15	4	14	17	90	
9-159-3	8	1	8	11	90	N/A
9-159-6	5	5	7	90	90	.63
Combination	11	1	9	19	90	

# SUGGESTED COMBINATIONS BRIGHTNESS

	S+	S-	G+	G-	EL	B
8-216-2	6	10	13	20	100	.15
8-248-6	10	4	3	13	100	.15
Combination	11	10	4	20	100	
8-219-4	6	9	5	20	100	.22
8-228-8	4	6	11	12	100	.275
Combination	8	10	9	20	100	
9-151-4	5	2	14	17	100	.63
9-159-6	5	5	7	11	100	.63
Combination	11	2	11	20	90	
9-159-4	10	10	7	17	100	1.1
9-156-5	6	4	20	11	100	1.13
Combination	6	10	7	20	90	
9-151-5	10	5	12	15	100	.74
9-156-2	9	10	3	19	100	.72
Combination	12	10	7	20	90	
Not Used:	8-248-3					0.15
	8-138-1					0.35
	9-169-7					1.25
	9-159-3					N/A

# PACKAGED PANELS

Display Numbers	Repaired		S+	S-	Bias Voltages		EL	
	Yes	No			G+	G-		
8261-4		X	5	5	10	13	100	#25
8269-4	X							
8205-4	X							
8235-4	X		3	7	12	10	100	#26
9033-2	X							
9036-5	X		10	10	4	19	100	Not
9010-6		X						
9079-1		X	12	1	7	15	100	
8239-2		X						
8240-2		X	7	8	3	12	100	

## 8.2 Riston Process

### 8.2.1. Storage and Handling prior to Final Sealing.

Storage and handling procedures should be carefully observed in order to ensure proper final sealing. The equipment required for this consists of a (i) dry box (capable of maintaining a nitrogen environment over extended periods of time), (ii) racks for storage (which can hold the substrates in a vertical position and can keep them separate). Corning Glass generally ships the substrates in special containers which are suitable for storage.

It is imperative that until the final sealing of DMD panels, these panels should be stored in a clean, dry, nitrogen atmosphere. Any surface contamination or moisture will seriously affect the quality of the Riston process. Moreover, the DMD panel should never be handled with naked hands prior to final seal. Fingerprints will have a negative effect on all process steps prior to final sealing.

### 8.2.2. Riston Lamination Equipment.

The equipment needed for the Riston Lamination includes

- a. Vapor Degreaser
- b. Riston laminator
- c. Room lighting that will not activate Riston material
- d. Filtered nitrogen supply with ionized nozzle
- e. Riston photopolymer film resist
- f. Light proof storage boxes
- g. Single edge razor blades
- h. Glass test sample plate, 3.10" x 7.10"

For a more detailed description of the equipment see Appendix II.

#### Process:

Since Riston is sensitive to normal lighting conditions, the room is generally put in a "yellow light". Thirty minutes prior to use, the laminator is pre-heated, and operating temperature is specified in the process specification section. Then a roll of Riston is placed in the center of the Riston Supply Roll. Enough Riston is pulled off the roll

to be threaded and taped to the polyethelyne take-up roll. Figure 8-1 illustrates the proper threading procedure. The Polyetheylene Take-up Roll is then lowered in the slots provided until it rests on the Riston Supply Roll. The Riston Supply Roll drives the Polyethylene Take-up Roll through this contact. Then the "Pressure/Gap Adjustable Knob" is turned to the maximum closed position. Pressure setting is specified in the Process Specification section and the next step is the insertion of a clean, clear piece of glass, 3.10" x 7.10", into the laminator narrow width forward until it stops. The Speed Control is then checked for the proper setting; the proper laminating speed is specified in the Process Specification section. The operator can then reach behind the laminator and grasp the Riston extending from behind the laminating rolls. While holding the Riston with one hand, the operator can turn on the Main Motor Switch. This results in the glass piece being drawn between the lamination rollers. The operator must maintain a grip on the Riston from behind the laminator and follow the feed motion until the glass piece clears the rollers by approximately 4 inches. Then, the operator cuts the Riston behind the rollers after turning off the Main Motor Switch. This is done with a single edge razor blade. Enough Riston must be left behind to provide a grip for the next piece to be processed. The glass piece is used as a sample to judge the quality of lamination, which is specified in the Process Specification Section. Then the DMD panel to be laminated is placed in the vapor degreaser, and the degreasing time is specified in the Process Specification Section. After extraction from the vapor degreaser the DMD panel is blown free of particles with a nitrogen ionized gun. After all this, the DMD panel is placed on the laminating table with the circuit side up and the butting edge to the left. It is then pushed into the laminating rolls until it stops. The operator then reaches behind the laminator and grasps the Riston behind the laminating rolls. When the Main Motor Switch is turned on the DMD panel will begin to feed into the rollers. The operator maintains his grip on the Riston and follows the feeding motion until the DMD panel is free from the rollers by approximately 4 inches. The Main Motor Switch is then turned off. The Riston is then cut with a single edge razor blade leaving enough Riston behind the rollers for the next piece, after which the

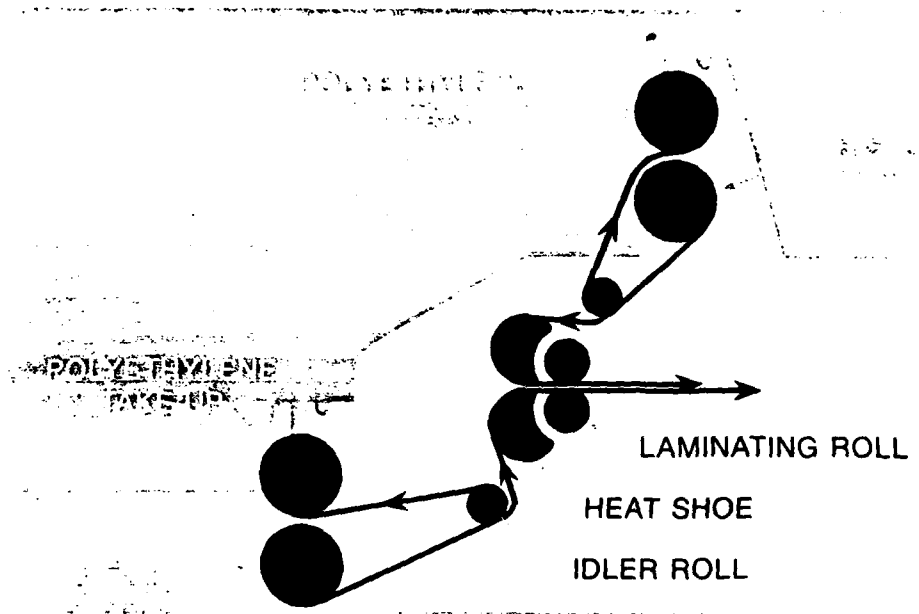


Figure 8.1 Thread up diagram

panel is placed on the laminator table with the Riston side down, and the excess Riston trimmed off. The butting edge and the edge opposite it are trimmed to the edge of the glass. The remaining edges are trimmed leaving approximately 1 inch of Riston excess on each edge. These "tabs" are used to hold the panel on the exposure table. The laminated panel is now inspected and must be defect free and possess excellent adherence. If any defects exist or the adherence is poor, the Riston is pulled off and the process repeated with adjustments made in pressure or temperature, or with a new supply roll, if necessary.

If the Riston has been in contact with the heat show for a excessive period of time, the laminating quality will decrease. It is good practice to use the laminator as quickly as possible when making multiple laminations. If the lamination is acceptable the panel is stored in a light proof box until exposure. Storage time is specified in Process Specification section. The process for Riston lamination and the procedure is schematically presented in Figure 8-2, and the process specification information appear in Table 8-1.

#### 8.2.3. Riston Exposure.

The following materials and equipment are needed by Riston exposure:

1. Exposure unit.
2. Room lighting that will not activate Riston material.
3. Microscope and stand.
4. Mask 13 EL insulator photomask
5. Single edge razor blades.
6. Anti-static brush.
7. Black paper.
8. Clean, blank DMD substrate.
9. DMD substrate clean and blank with edges rounded.
10. Two strips of 1" x 8" printed circuit board material.

The Manufacturer's literature on the equipment is in Appendix III.

#### Process:

The exposure unit is turned on 15 minutes prior to use for the purpose of warmup, even though in DMD processing only the top

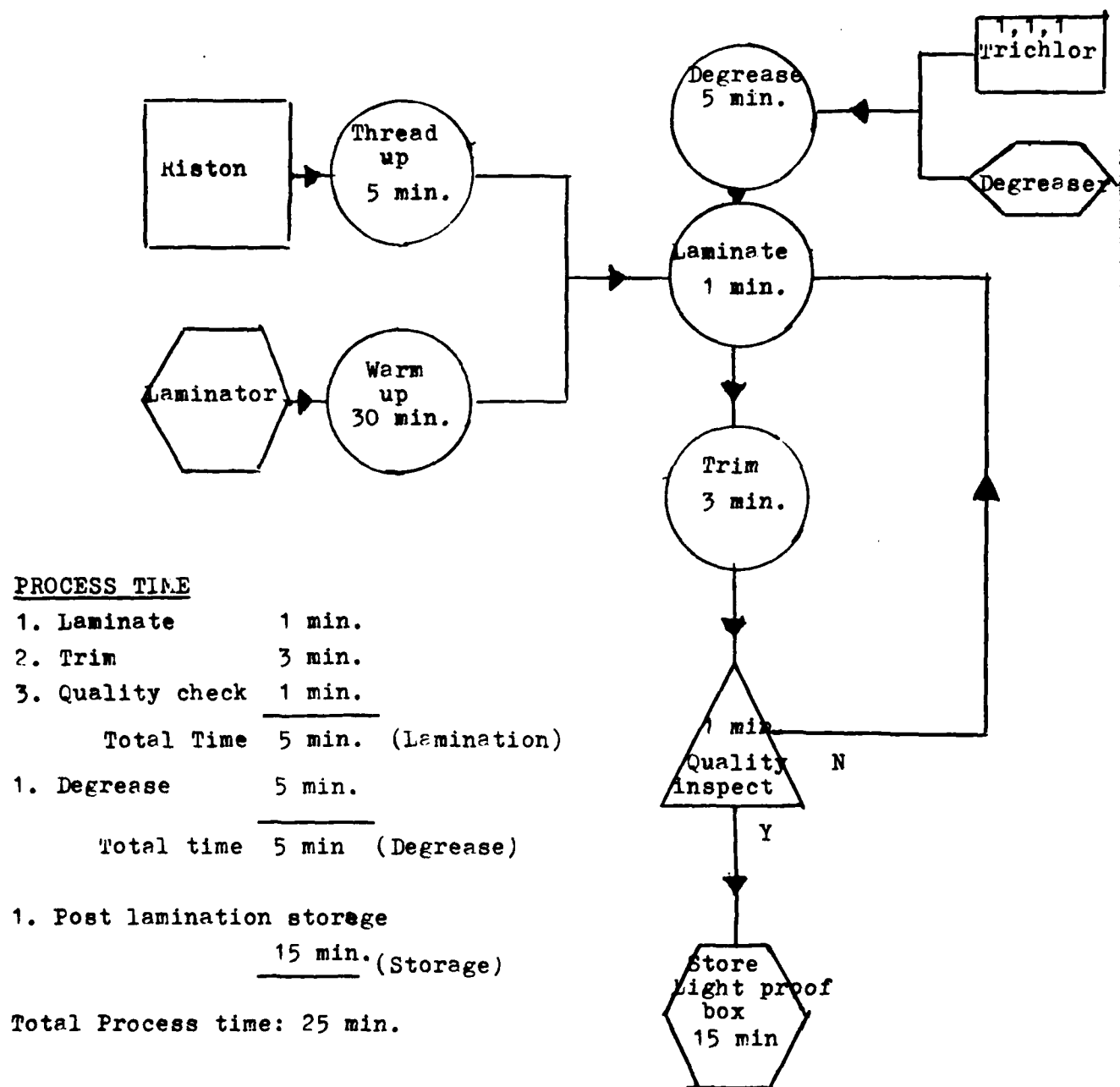


Figure 8-2. Process time and flow information in Riston Lamination.



TABLE 8-1

Process Information for Riston Lamination

Present Specifications	Revision 1	Revision 2	Revision 3
1. Laminator roll temp. 230 + 10°F			
2. Riston Type: X113 S Du Pont			
3. Pressure/Gap Adjustable Knob setting: Maximum closed position			
4. Speed Control setting: 4 fpm.			
5. Degreasing time: 5 min. Agent: 1, 1, 1 Trichloroethane Hours per batch: Not yet determined			
6. Lamination quality: No ripples No bubbles No holes Tight adhesion to panel			
7. Test glass: Dow Corning 7059 3.10" x 7.10"			
8. Post lamination storage time: 15 min.			

exposure lamp is turned on. By pushing the frame release switch the exposure frame is released. Then the exposure frame glass is brushed free of particles with the anti-static brush and the room is put in a "yellow light" condition. Next, the DMD panel to be exposed is removed from the light proof box and placed in the center of the glass on the exposure table. One inch "tabs" of excess Riston are used to hold the DMD panel to the frame. Once this is done, the DMD panel is placed with the Riston side up and the butting edge to the right; the tabs are then pressed to the glass. The butting edge of a clean, clear DMD substrate is then mated with the butting edge of the DMD panel to be exposed which provides support for the photomask. Mask 13 EL Insulator mask is placed on top of the Riston laminated DMD panel, and the clean, clear DMD substrate with the smooth edges is centered above the photomask. The smooth edges prevent puncture of the plastic top frame cover. The binocular microscope is then swung into position over the Riston laminated panel for alignment. After this step, the black paper centered beneath the glass table is lowered and the "yellow" back light turned on. A copy of the Mask 13 EL insulator photomask is shown in Figure 8-3. The small dark squares that delineate the alphanumeric characters are centered over the DMD panel to be exposed. The mask is aligned from left to right and top to bottom. The microscope is used to cement the top and bottom corner mask squares, in the first row, left side, over the respective EL pads on the panel. If positioning is correct the row of EL pads can appear on the right side of the DMD panel without a mask square above them. The alignment is done by manually moving the photomask while viewing through the microscope. The microscope is scanned across all sections of the mask to assure the centering of mask squares over EL pads on the DMD panel. When the masks are aligned, two strips of printed circuit board material, 1" x 8" are placed as follows: one on the left side of the table, vertically, one inch from the DMD panel, the other horizontally, one inch from the DMD panel at the top. These strips facilitate the vacuum action when the exposure table top is lowered. The next step is to carefully lower the exposure table top and clamp and turn the vacuum switch on. The vacuum draws the exposure table top tight to the glass table thus clamping the mask and DMD panel. Once again, the microscope is used to check photomask alignment.

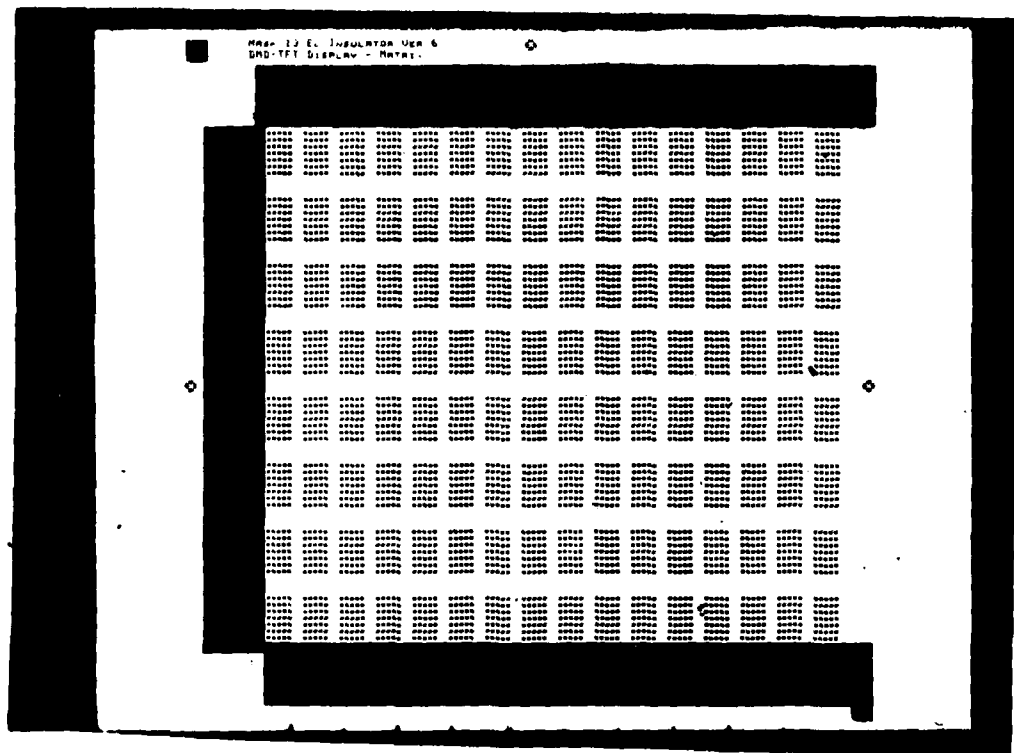


Fig. 8.3 Photo copy of Mask 13 insulator photomask used in exposing Riston on DMD panels.

If the photomask has moved the alignment procedure must be repeated. If alignment is correct, the "yellow" backlight is turned off and the black paper beneath the glass table is raised and taped into position. The Riston "tabs" that hold the DMD panel to the table are covered with black tape to prevent their exposure. The tape is placed atop the plastic exposure table top. The exposure timer is set, and exposure time is specified in Process Specification Section. The table is pushed into the unit until it catches. After the exposure time, the Frame Release Switch is pushed and the table will eject. The black tape is removed from the top cover. The Vacuum Switch is turned off and the top unclamped and raised. The photomask and the glass pieces are removed and stored. The Riston "tabs" are then carefully lifted from the glass table with the aid of a single edge razor blade and "tabs" are then cut close to the edges of the DMD panel. Finally, the exposed DMD panel is then stored in a light proof box for 15 minutes before developing.

Process time and flow information for Riston Exposure are delineated in the Figure 8.4 and the process specification information is given in Table 8.2.

#### 8.2.4. Riston Development

The equipment and materials needed for Riston development are the following:

1. Riston developer.
2. Room lighting that will not activate Riston material.
3. 1,1,1 - Trichloroethane.
4. Developer immersion holder.
5. Filtered de-ionized water.
6. Nitrogen supply and ionized gun.
7. Single edge razor blades.

Manufacturers equipment description literature presently in use are included in Appendix 5.

#### Process:

Once the water supply valve to the developer is opened, the Power switch is turned on. Then the developer timer is set, as has

# Process time and flow information

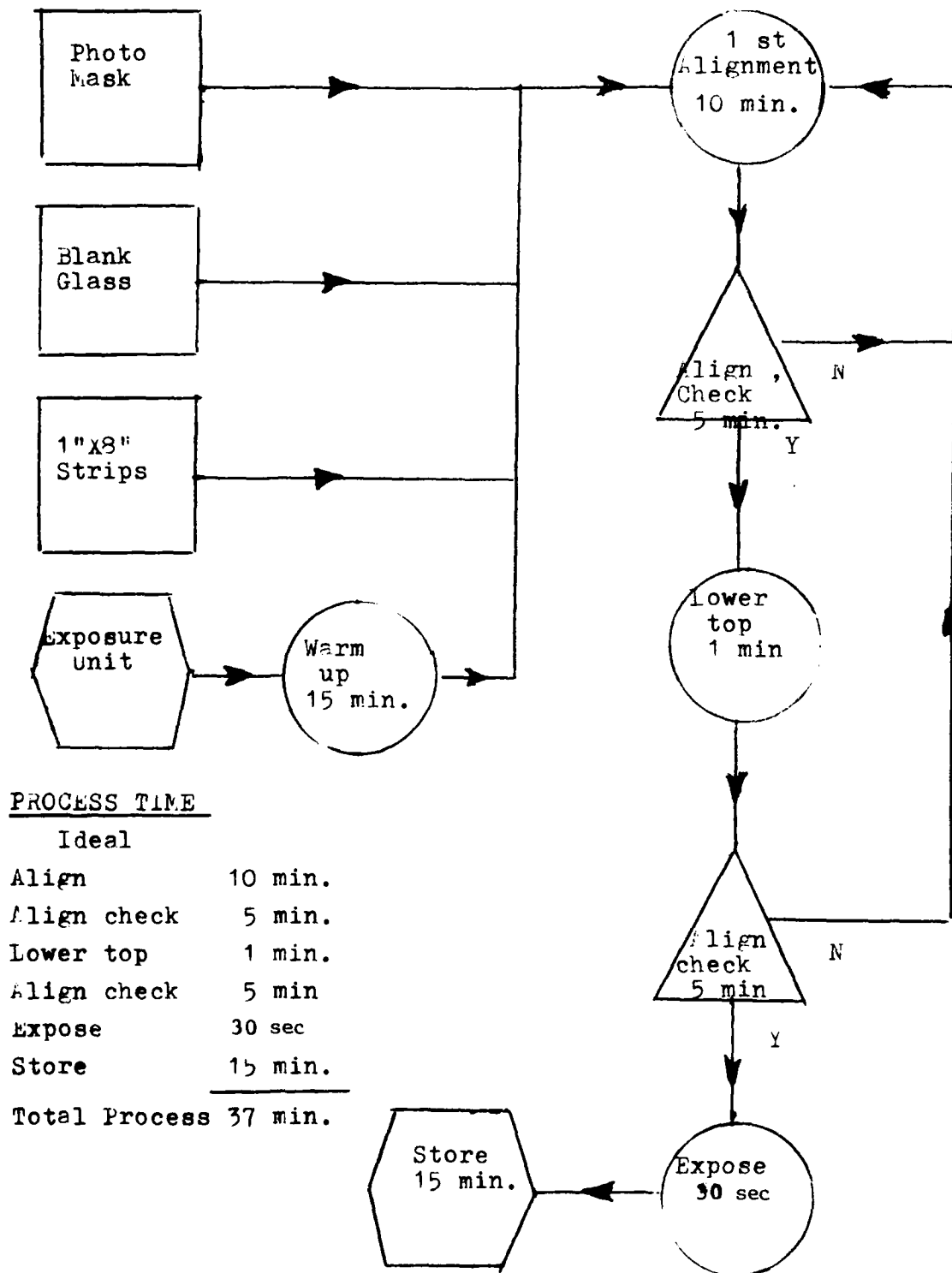


Figure 8.4 Process Time and Flow Information for Riston Exposure.

TABLE 8.2

## Process specification information.

Present specifications	Revision 1	Revision 2	Revision 3
1. Mask 13 EL Insulator Photomask Ver.6	Mask II EL Insul. Ver. 2 4-1-79		
2. Exposure time: 1 min.	4-1-79 30 SCS		
3. Butting glass for mask support: Dow Corning, 7059 3.10" X 3.55"			
4. Mask cover glass: Dow Corning, 7059 3.10" X 3.55" Edges and corners ground smooth.			
5. vacuum assist strips. Printed circuit board material 1' X 3"			
6. black tape: 3M 33 tape 1" wide.			

been discussed in the Process Specification section. After this step is complete, the start button on the timer is pushed to activate one development cycle before using. Next, the DMD panel to be developed is removed from the light proof box and the top Mylar covering on the Riston is carefully removed. Usually a corner can be loosened with a single edge razor blade and the sheet removed by hand. The DMD panel is immediately placed in the immersion holder and immersed in the development tank. Then the cycle is started by pushing the button on the timer. When the cycle is completed the holder is immediately removed and the DMD panel rinsed with filtered de-ionized water. The DMD panel is then quickly dried off with a nitrogen ionized gun. It is essential that these steps be performed rapidly in order to remove a panel from the developer through rinsing.

After development, the DMD panel is not sensitive to normal room lighting. The development inspection is now performed and inspection specifications appear in the Process Specification section. If any defects occur, the panel must be stripped in the vapor degreaser until all traces of Riston are gone. The panel then has to go through the Lamination process.

The process time and flow information for Riston Development is schematically represented in Figure 8.5 and Table 8.3.

#### 8.2.5. Vacuum Bake

For this step, the equipment and materials needed are as follows:

1. Vacuum oven:                      National Appliance Co.  
    Model 5831-4  
    115 VAC
- 2 Vacuum source.
3. Two heat sinks:  
    4" x 8" x 1"

#### Process:

The developed DMD panel is placed on a cold 4" x 8" x 1" aluminum block used for a heat sink; both the panel and the heat sink are placed in the cold vacuum oven. The oven, however, is placed under vacuum only for 20 minutes. Then the heat is turned on and allowed to

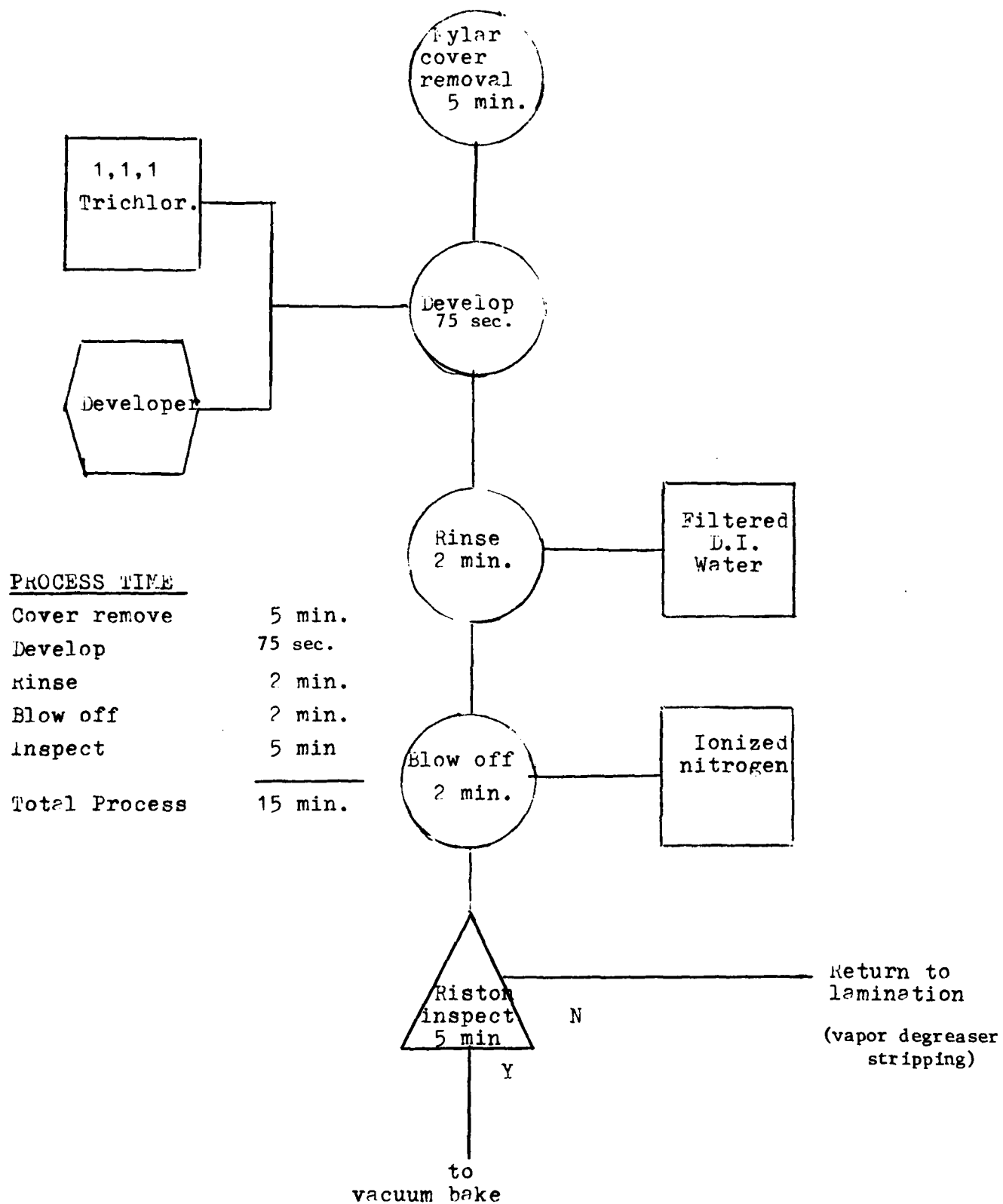


Figure 8.5. Process time and Flow Information for Riston Development.



Table 8.3

## Process specification information for Riston Development

Present specifications	Revision 1	Revision 2	Revision 3
1. Developing agent: 1,1,1 Trichloroethane			
2. Development time: 1 min.	10-1-78 75 sec.		
3. Rinsing agent: Filtered Deionized water, 500 micron filter.			
4. Blow off: Filtered nitrogen with ionized gun.			
5. Developing agent life: not yet determined			
6. Development quality: 1. Sharp borders. 2. EL apertures open. 3. No peeling. 4. No bubbles.			

rise at 40°C for 20 minutes. Following this, the temperature is then set for 80°C and the panel baked for 20 minutes. After one hour of vacuum treatment, and when the temperature gradually rises, gradual temperature rise, the DMD panel is removed from the oven. The Riston is inspected for defects as specified in the Process Specification section. If no defects are present, the panel is then ready for phosphor application. However, should there be defects, the panel has to be stripped of the Riston.

The process time and flow information for vacuum baking is shown in Figure 8.6.

# Process time and flow information

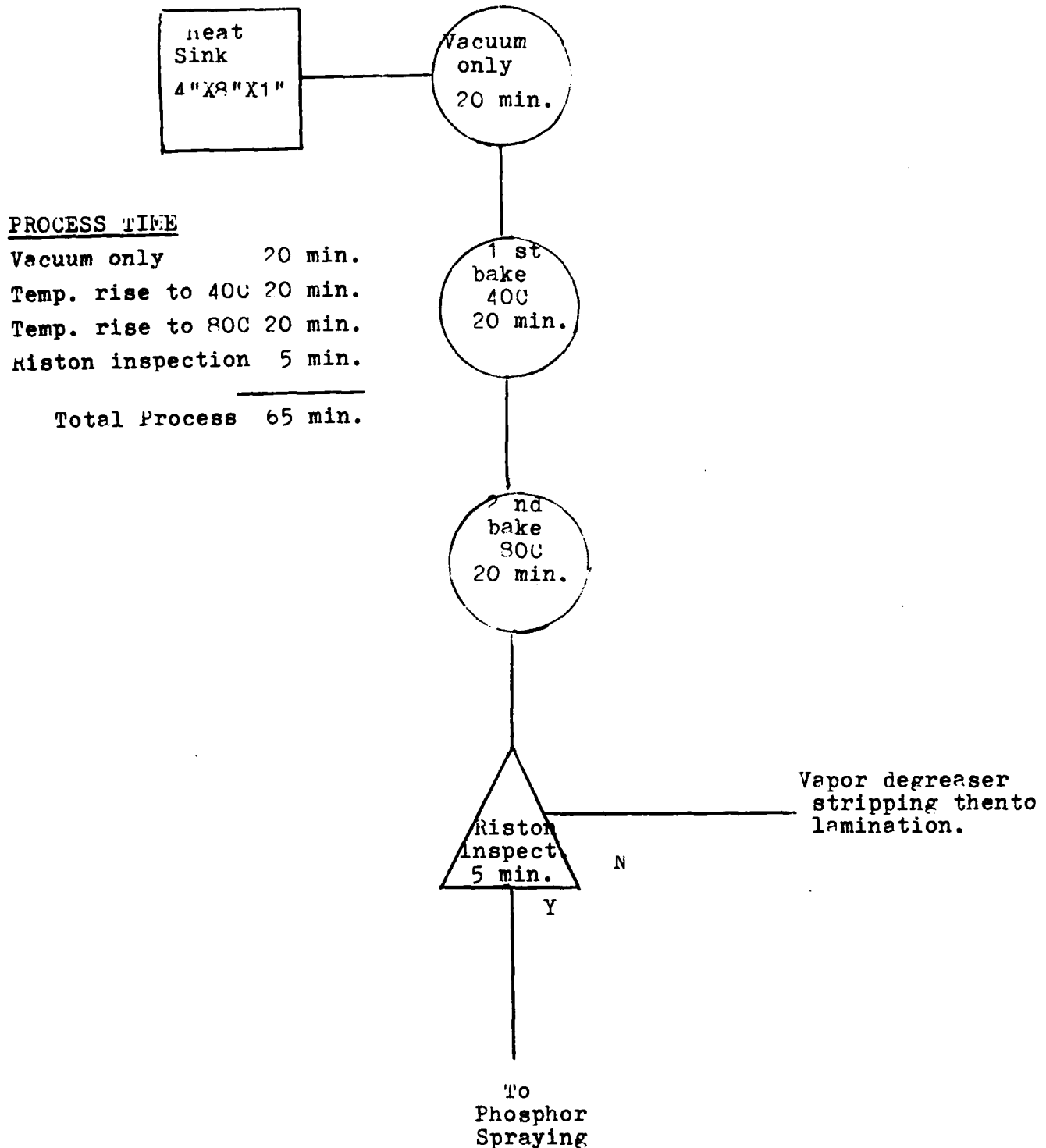


Figure 8.6 Process time and flow information for Vacuum Bake

Table 8.4

Process specification information of Vacuum Bake

Present specifications	Revision 1	Revision 2	Revision 3
1. vacuum without heat: 20 min.			
2. 1 st heat rise: 40 C 20 min.			
3. 2nd heat rise: 90 C 20 min.			
4. heat sink: Aluminum block 4" X 3" X 1"			
5. Riston inspection: 1. No bubbles 2. No loss of adhesion			

### 8.3 Encapsulation Process

#### 8.3.1 Encapsulation of Panels

After the Riston, phosphor and top semitransparent electrode steps have been completed, 1/2-DMD panels tested and matched, they are aligned and attached to a rear glass, cover or base plate, and then covered with a top glass cover or window which, together with a plastic encapsulant, gives a sealed package.

The encapsulation process begins with application of a double adhesive tape to the back cover glass, Fig. 8.7. Initial alignment of the two half panels is performed with aid of an alignment fixture with magnifier, Fig. 8.8. The critical element is making sure the rows of EL elements, that is, rows of the active, light-emitting areas of the elemental cells, on each of the two halves are in line where the two panels abut. Figure 8.9 illustrates proper and improper alignment. Back cover guides, attached to the same fixture although not alone in Fig. 8.8, are then adjusted to position the back cover glass in relation to the two aligned halves so that its positioning is as nearly symmetric as possible, and the back cover applied, Fig. 8.10. The panel is then removed from this fixture, a protective layer of one-sided adhesive Teflon tape is applied over the edge contacts of the assembled pair of 1/2-panels, Fig. 8.11, and mounted in the packaging fixture, Fig. 8.12, on top of a thin foam pad to cushion the assembly. Side rails are then attached to this fixture by hand-tightened cap screws, a silicone RTV potting compound poured on the surface, and the top glass window carefully placed in position, one end first so as to sweep all air bubbles to the opposite end as the cover is gradually pressed into place. This assembly is simply held together by the jig until the silicone RTV has set, thus completing the encapsulation process. These alignment and packaging steps are summarized in Fig. 8.13, which again shows the alignment fixture with panels, the top cover packaging fixture with side rails in place, and, in cross section, the completed DMD package.

Dwg. 7721A65

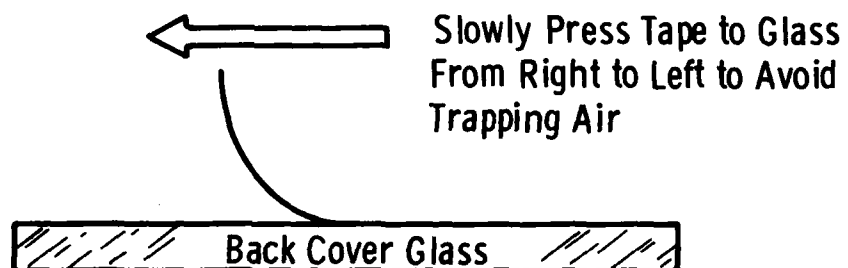
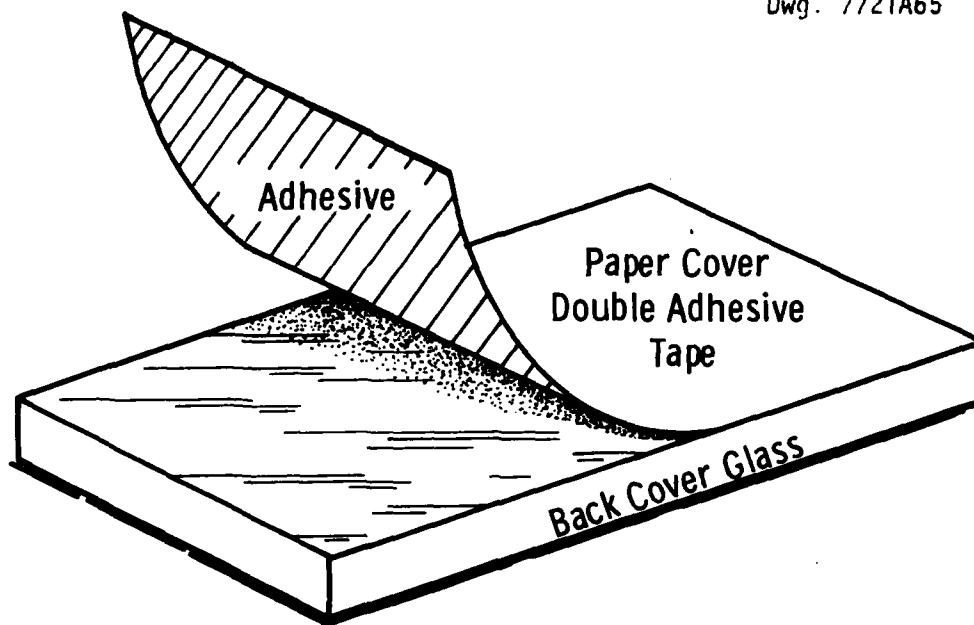


Figure 8.7 Application of double adhesive tape to back cover glass.

Dwg. 7721A68

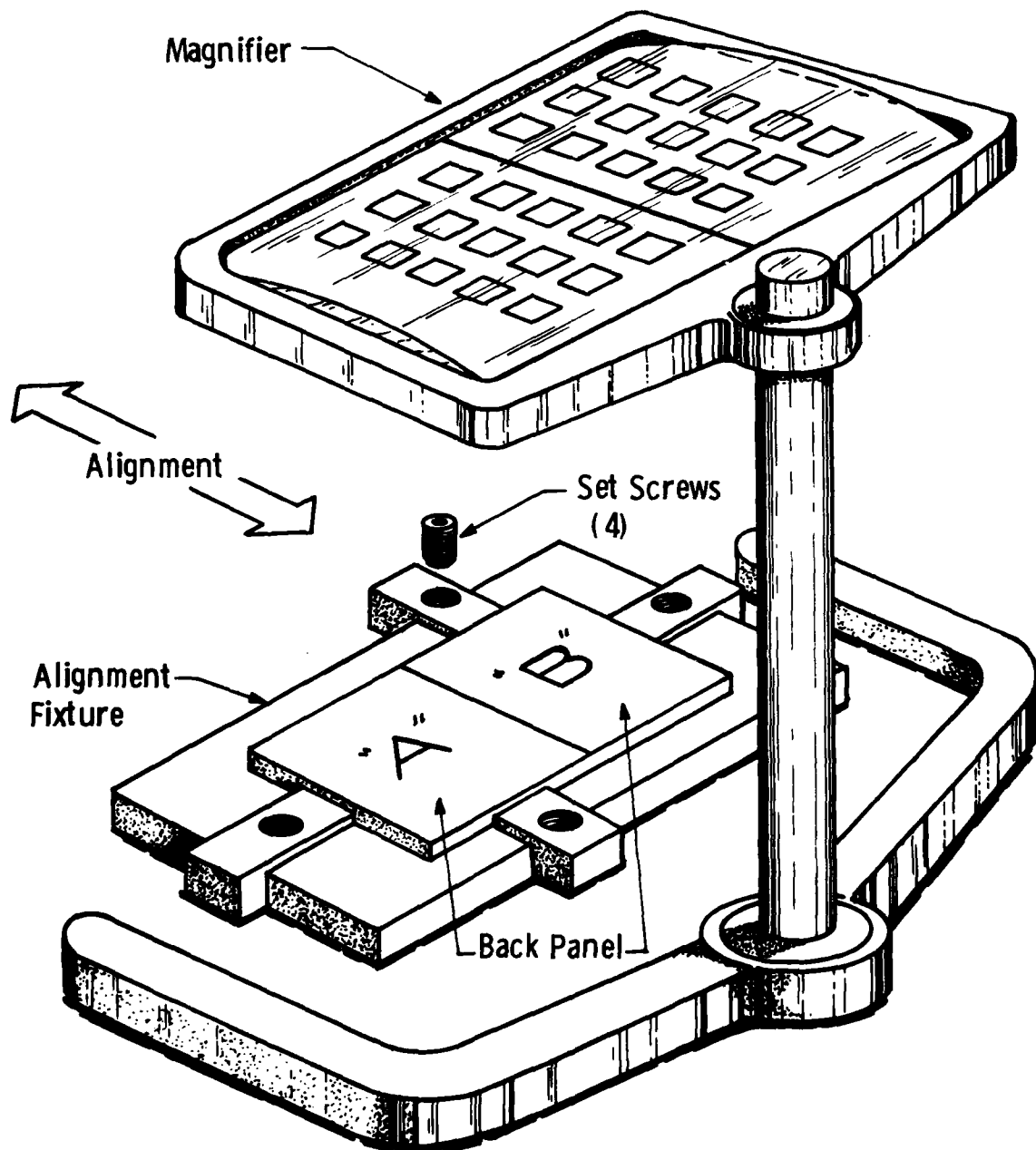


Figure 8.8 Panel abutment and alignment.

Dwg. 7721A70

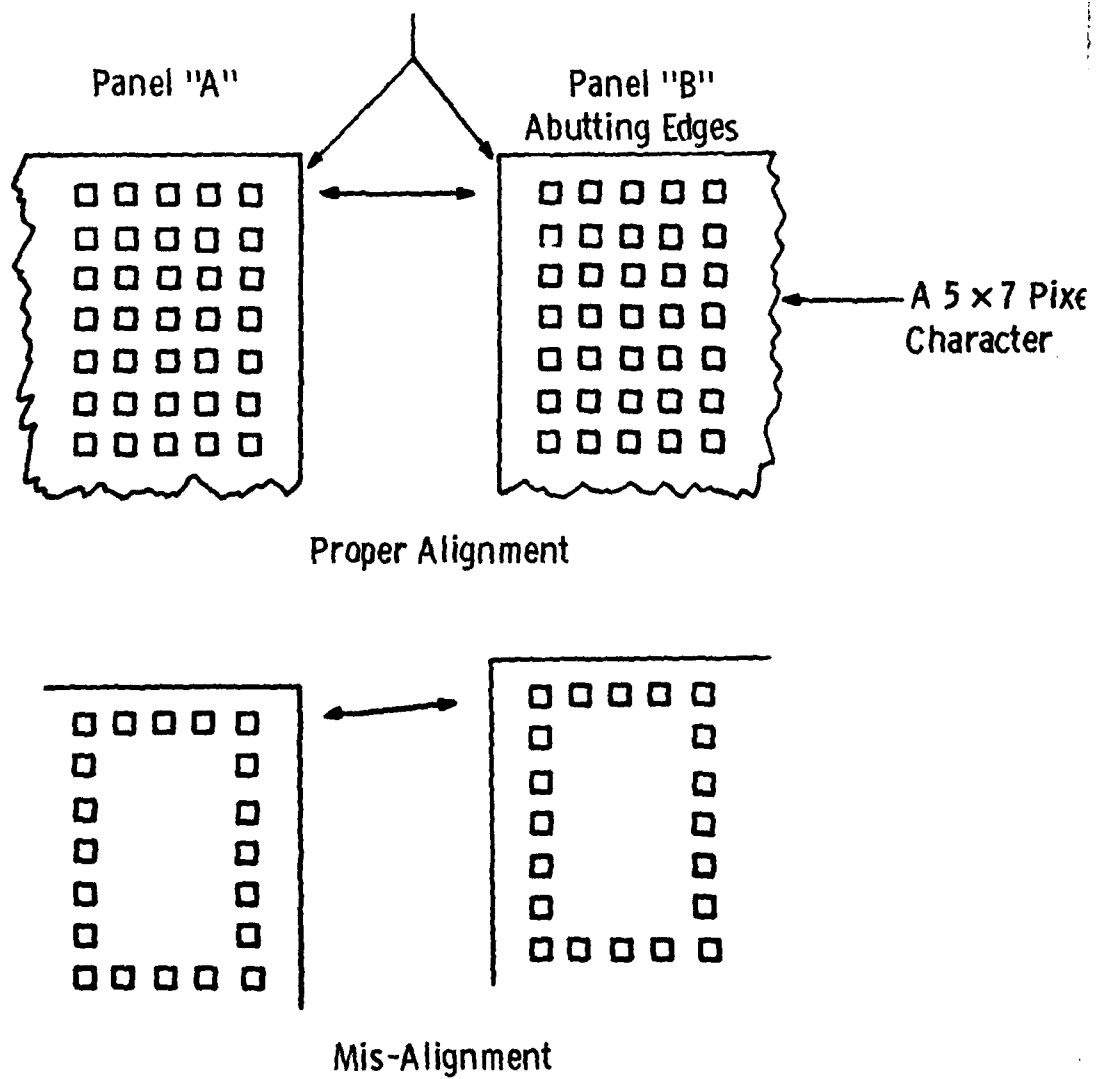


Figure 8.9 Proper alignment vs misalignment of panels



Dwg. 7721A67

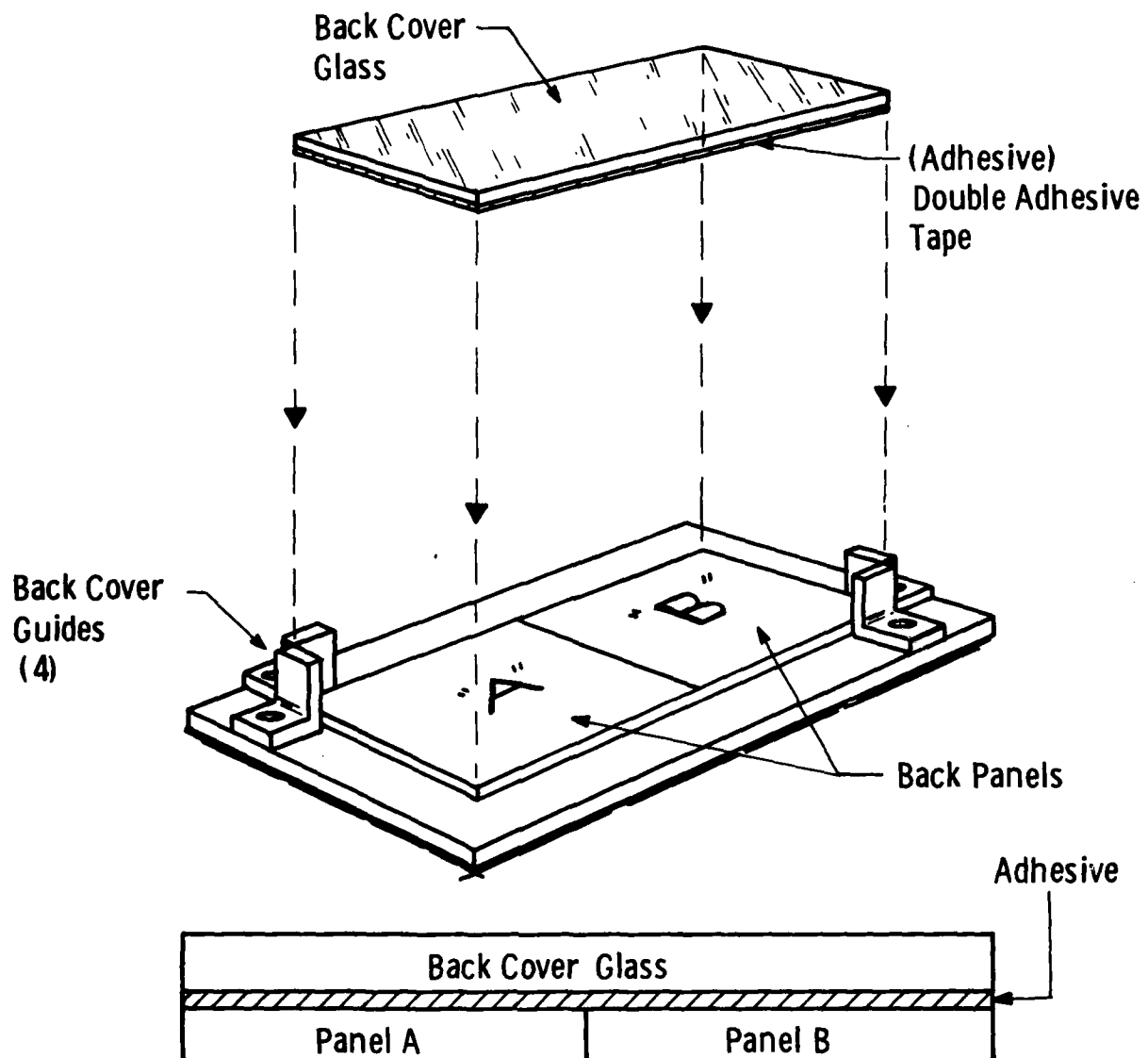


Figure 8.10 Back cover application.

Dwg. 7721A64

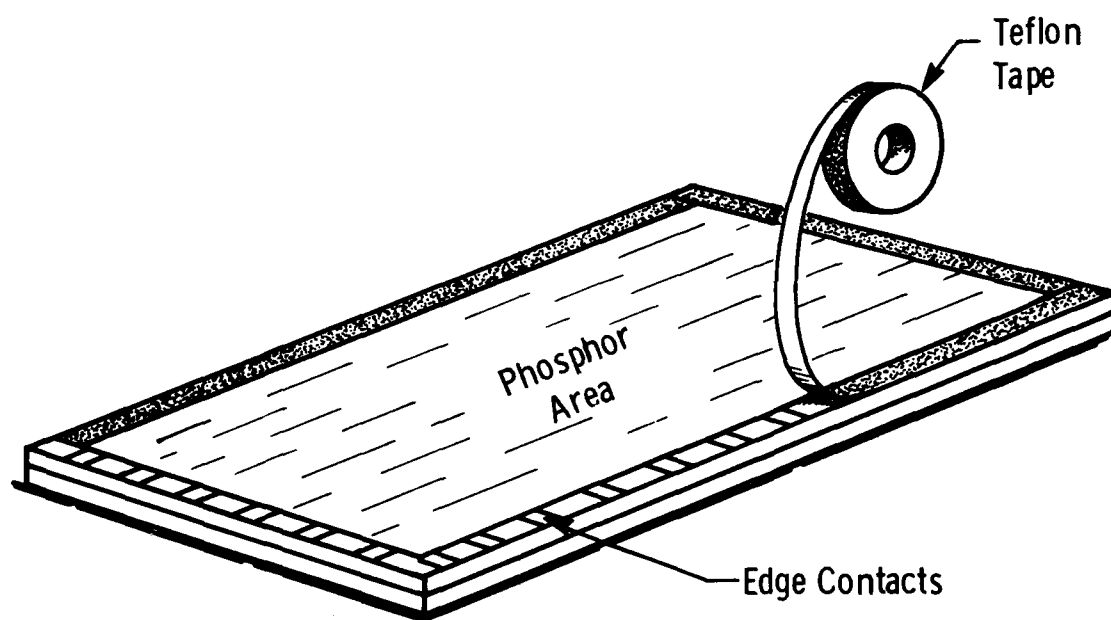


Figure 8.11 Application of Teflon tape to edge contacts.

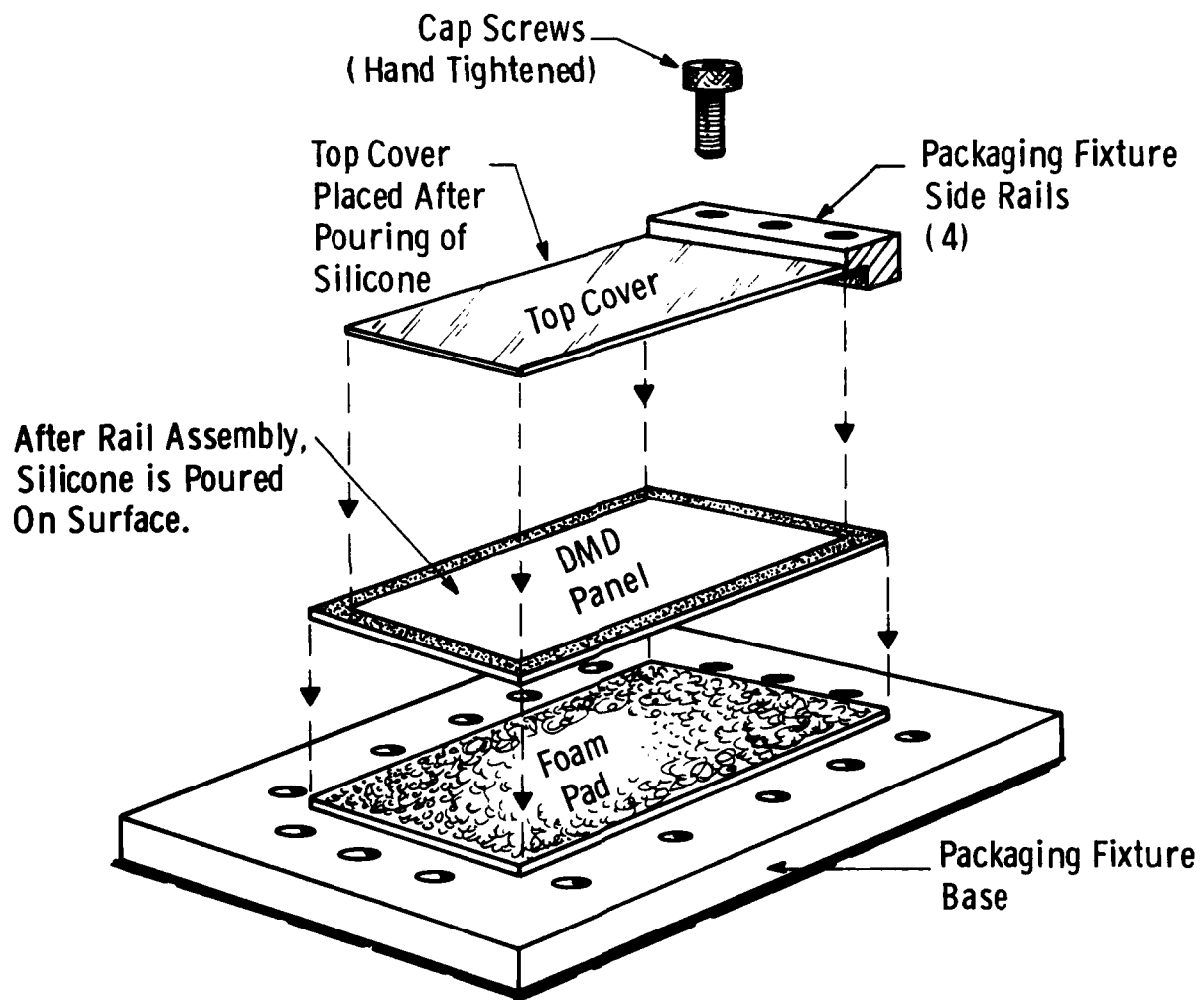
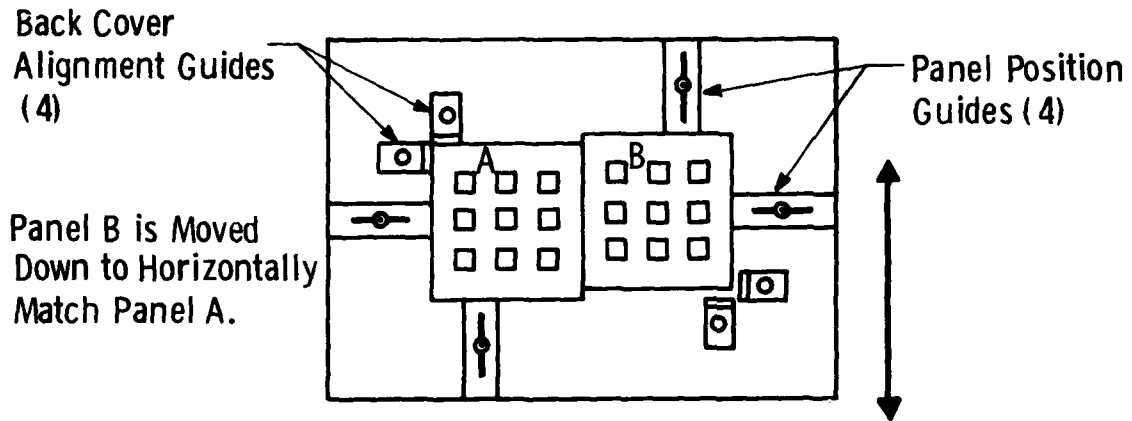
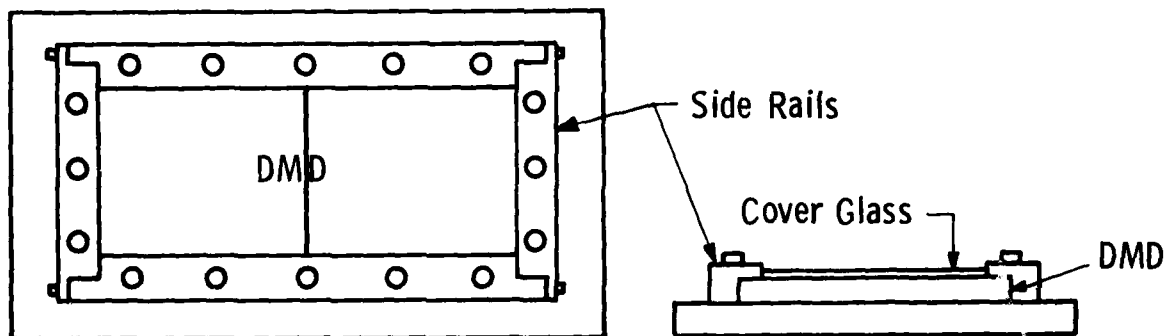


Figure 8.12 Packaging fixture.

Dwg. 7721A66



Half Panel Abutment Fixture



Top Cover Packaging Fixture

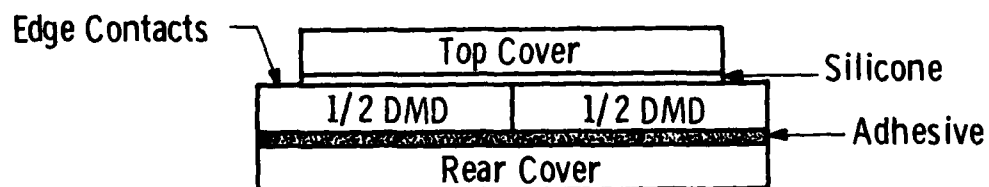


Figure 8.13 DMD Package.

## 9. DRIVE ELECTRONICS

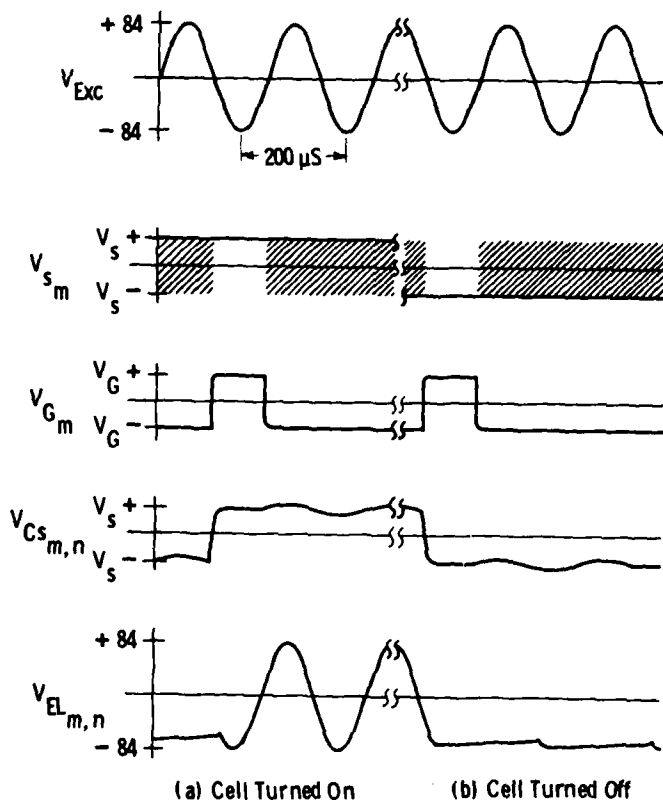
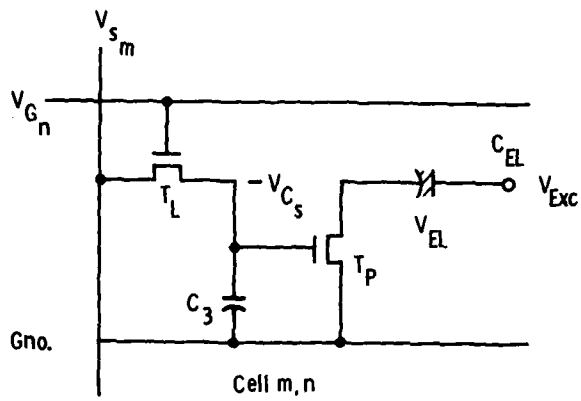
In this section are discussed both the electrical drive - waveforms and circuits - needed to power the phosphor and to control the active matrix of the TFT-EL display, and also the logic and signal processing circuits needed to display alphanumeric information. At the Westinghouse laboratories, the development of this auxiliary circuitry has not been pursued vigorously as compared with the development of the active matrix circuit itself, and early drive circuitry designed for alphanumeric TFT-EL displays over seven years ago has been used with only minor modification until quite recently. During the period of the present contract, however, about five new and different exercisers have been designed and built, two of which were developed in connection with other concurrent programs. A better understanding of the needs of the TFT addressing/control matrix was reached in the pursuit of these new designs, some aspects of which were referred to earlier in Section 2.4.3. Further aspects of meeting panel requirements and the improved panel operation resulting will be discussed in the following material. The most significant finding can be briefly stated here, however, namely that under optimal driving conditions, the logic transistors  $T_L$  in the TFT matrix have demonstrated superior ON/OFF conductance ratios as high as  $10^6$  or  $10^7$  to 1. This in turn puts a new, previously un-noted, complexion on matrix design and suggests possibilities for fabrication simplification as well as for reduced frame rates and attendant savings in power and data rates. In particular, display data storage for up to 2 minutes and flickerless displays operating at refresh or frame rates have been demonstrated. Beyond this, several improved, high-efficiency resonant drive EL excitation supplies have been designed, and methods for counteracting TFT drift under negative bias have been implemented.

The MM&T program has required design and construction of two test exercisers, referred to as the ON/OFF exerciser and the viewability exerciser. Progress was made on a third exerciser based on low frame rates, and a breadboard model was constructed and operated. The following sections describe these designs in turn, preceded by a discussion of matrix drive requirements. Finally, factors which are believed to be imperative in future high efficiency TFT-EL displays are summarized at the end of Section 9.5.

### 9.1 Electrical Drive Requirements

The basic requirements of the TFT matrix of the TFT-EL display for electrical drive and line-at-a-time addressing have been referred to several times earlier, notably in Sections 2.1 and 2.4. Some of the waveform amplitudes required depend on timing considerations and effects of induced voltages, the latter having been discussed in some detail in Sections 2.4.2 and 2.4.3. The three basic signals that must be supplied to the panel are illustrated in Figure 9.1, which also includes the cell schematic for reference. To turn the (m,n)'th cell ON, a video high level,  $V_{S+}$ , is applied to the m th source bus, at which time a logic high level  $V_G+$  applied to the n th gate bus serves to turn on logic transistor  $T_L$  and set the voltage  $V_{CS}$  on storage capacitor  $C_S$  to the video level  $V_{S+}$ . At that point, the power transistor  $T_P$  is turned ON, and the full excitation voltage  $V_{EXC}$  is applied to the electroluminescent element  $C_{EL}$ . A peak-to-peak voltage of 168V (-84V to +84V or 60V rms) has been assumed here for purposes of illustration. When the EL element is to be turned OFF, a video low level,  $V_{S-}$  is impressed on the m th source bus, the n th gate bus again pulsed positively, and the low video level thereby set on capacitor  $C_{S, mn}$ . At this point, assuming a negative-going transition of  $V_{EXC}$  is in progress, transistor  $T_P$  continues to conduct in the inverted configuration (drain negative with respect to the gate and acting as source) until the negative peak is passed. After this, conduction ceases, and  $C_{EL}$  remains in a negatively charged condition, except for a small DC leakage current through the phosphor which discharges it slightly between succeeding negative peak excursions of the excitation waveform,  $V_{EXC}$ .

Curve 721930-B



**Fig. 9.1 – Typical TFT-EL display cell waveforms**

In the figure, the slight undulation shown on the  $V_{cs}$  waveform is due to capacitive pickup from the excitation electrode, as explained in Section 2.4.2. Similar wiggles are omitted from the gate and source bus waveforms, under the assumption that the driving impedance is sufficiently low to attenuate such induced signals (see Table 2.5). If the EL excitation is of square waveform instead of sinusoidal, pickup on the gate and source buses can be appreciable because of the short transition times and comparatively high induced currents. Resulting waveforms similar to those shown in Figure 9.2 exhibit a large positive or negative spike on both gate and source buses, requiring a much larger range of control voltages to keep the logic transistors  $T_L$  of the array out of conduction when not addressed. The first alphanumeric exerciser, mentioned earlier and described further in Section 9.2, employed such a square wave drive for EL excitation, with the result that quite large biases and voltage swings were necessary for panel operation. Table 9.1 compares the high and low logic levels typical for this older exerciser, for the viewability exerciser (Section 9.3) which uses a square-sine EL excitation, and for the tv exerciser developed under a separate program, also using square-sine EL excitation and which was the basis for a new exerciser design (Section 9.5).

It should be noted that the effect of a very short positive spike induced on a gate bus and repeated at the line or  $V_{EXC}$  frequency can make the logic transistors appear to have considerably larger leakage or OFF currents than its DC characteristics would support, and can easily lead to unwarranted conclusions about transistor performance and requisite transistor and cell design.

The capacitive loads which the excitation electrode, source buses and gate buses present to the drive circuits were detailed in Section 2.4.3 and Tables 2.5 and 2.6. The drive currents are proportional to rate-of-rise of the pertinent waveforms, but are limited by bus and driver impedances. Of principal concern is that the driver has a low enough impedance to suppress induced transients and to swing the gate or source bus potential from logic positive to logic negative or reverse in a time short compared to the line access time, i.e., short compared to 200  $\mu$ S.



Curve 721928-B

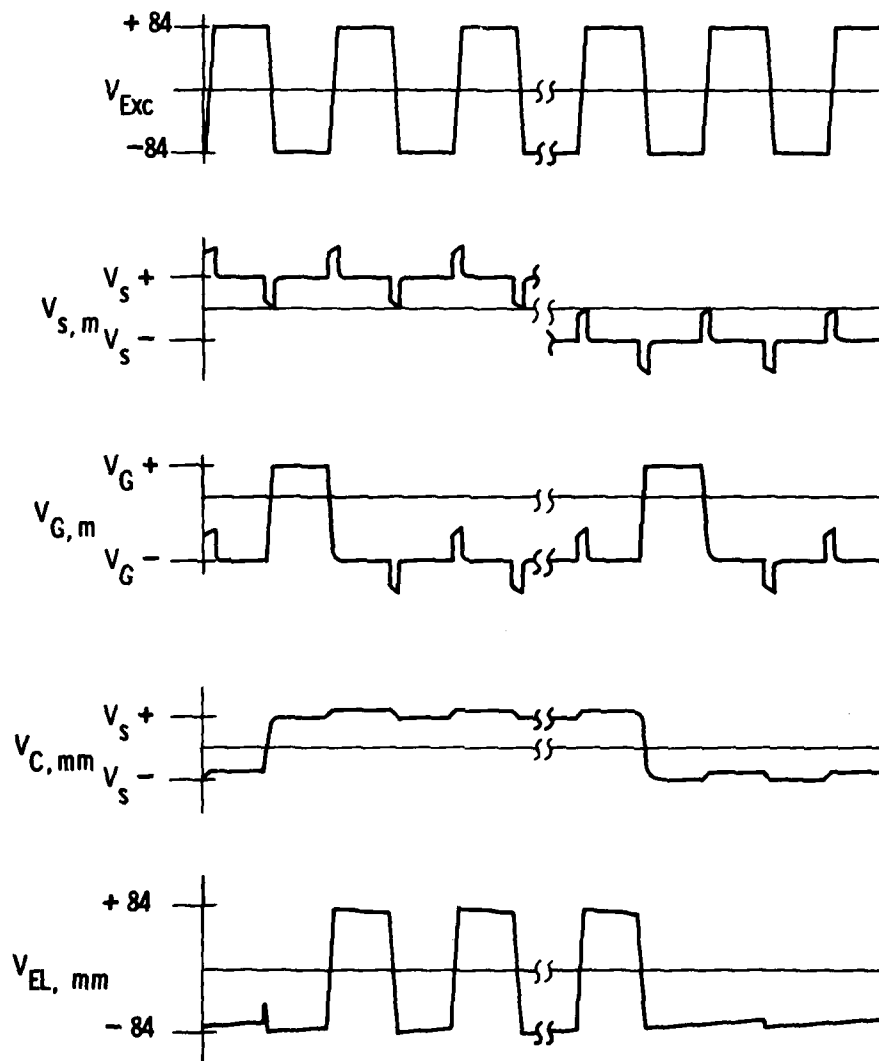


Fig. 9. 2 – TFT-EL display waveforms with square wave EL excitation

In this regard, a maximum transition time of 50  $\mu$ S has been the aim of recent exerciser designs.

TABLE 9.1

TYPICAL CONTROL VOLTAGE RANGES  
FOR TFT-EL DISPLAY ALPHANUMERIC EXERCISERS

	Original Exerciser	Viewability Tester	TV Exerciser
$V_{EXC}$	168 V <sub>p-p</sub> , Square (5 $\mu$ S $\tau_T$ ) <sup>1.</sup>	168 V <sub>p-p</sub> , Square-Sine (50 $\mu$ S $\tau_T$ ) <sup>1.</sup>	168 V <sub>p-p</sub> , Square-Sine (50 $\mu$ S $\tau_T$ ) <sup>1.</sup>
$V_S^+$	+20	+10	+5
$V_S^-$	-10	-10	-5
$V_G^+$	+20	+10	+10
$V_G^-$	-40	-20	-8

1. Transition Time; Refer to Tables 2.5 & 2.6

9.2 Prior Approach

The first alphanumeric exerciser used for TFT-EL displays made at Westinghouse is shown in Figure 9.3. This exerciser was made in 1972 under Army contract #DAAB 07-72-C-0061. It was designed for demonstrating the capability of these displays for alphanumeric presentations, and its complexity was minimized by addressing all character rows simultaneously; all rows thus contained the same character string. This organization is shown in the block diagram of Figure 9.4. Selectable line refresh rates are provided at 62 Hz, 125 Hz, and 250 Hz. Bias voltages and EL excitation amplitude are set by adjustable power supplies. A square wave EL excitation supply of 50-watt output capacity is



Figure 9.3 First Alphanumeric Exerciser Showing Keyboard and Early TFT-EL Display

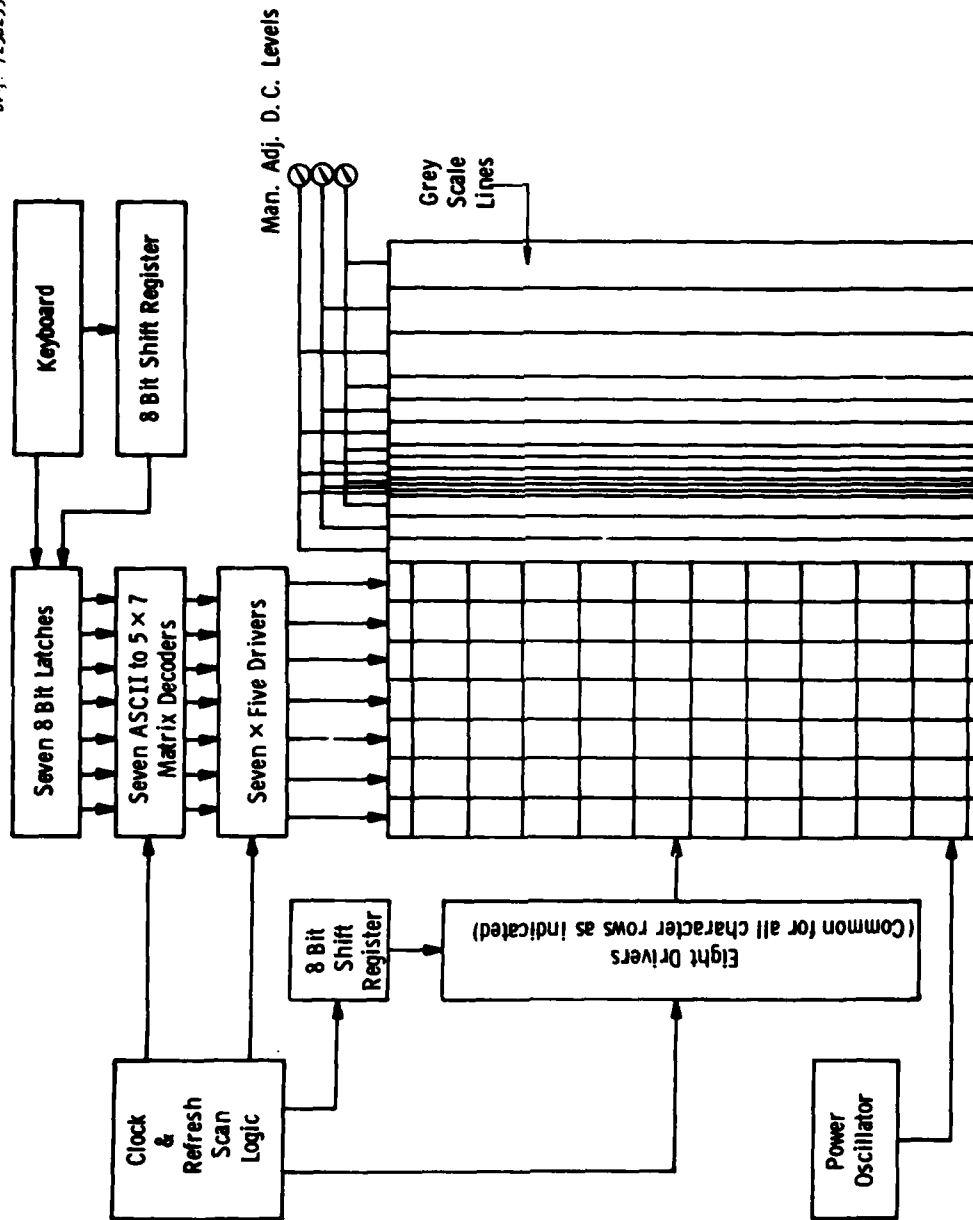


Fig. 9. 4 - Logic block diagram of first TFEL display exerciser

used. The source and gate driver impedances of this exerciser can be inferred from their schematic diagrams, shown in Figure 9.5, and are summarized in Table 9.2 following. Inasmuch as each gate bus driver is controlling a set of eight or more buses, the reactive load impedance is eight times lower than that of a single bus, and the driver impedance of 43 K $\Omega$  for the unaddressed gates is incapable of attenuating the spikes induced during the  $V_{exc}$  transition, amounting to about 20V. The need for keeping the positive spikes from turning on the logic Transistor accounts for the larger  $V_g$  - (shown in Table 3.1-1) which is required in the use of this exerciser.

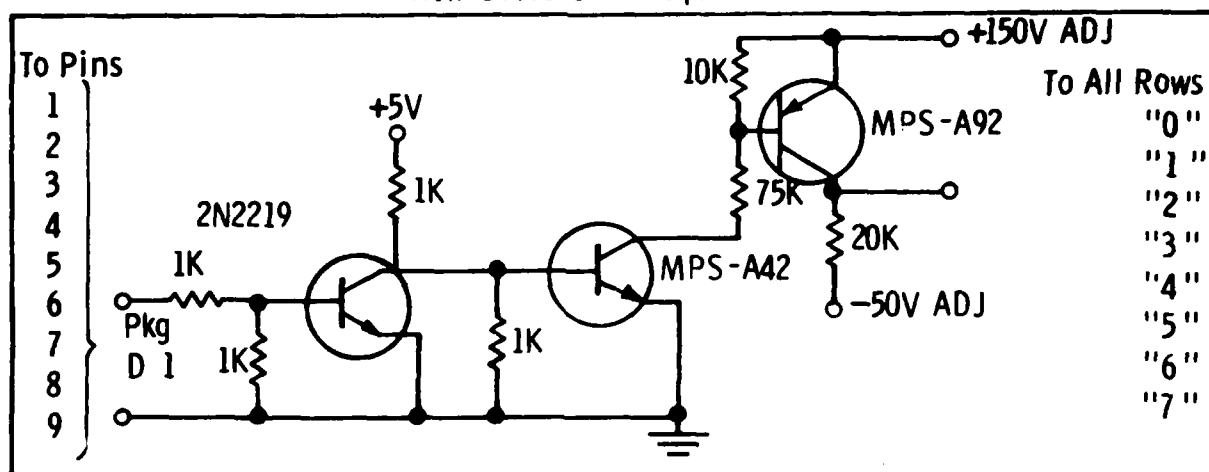
Inasmuch as the DMD viewability tests required in the present programs specify single random characters to be displayed in each of the character positions, this original exerciser, which could not provide the requisite signals, could not be used, and a new "viewability exerciser" was designed and built, as described in following Section 9.3.

TABLE 9.2

DRIVER IMPEDANCES, FIRST TFT-EL DISPLAY EXERCISER

Driver For	Impedance, OHMS	
	Logic High (+)	Logic Low (-)
Column (Source)	70	20,000
Row (Gate)	3200	43,000

# Row Drivers 8 Required



# Column Driver 35 Required

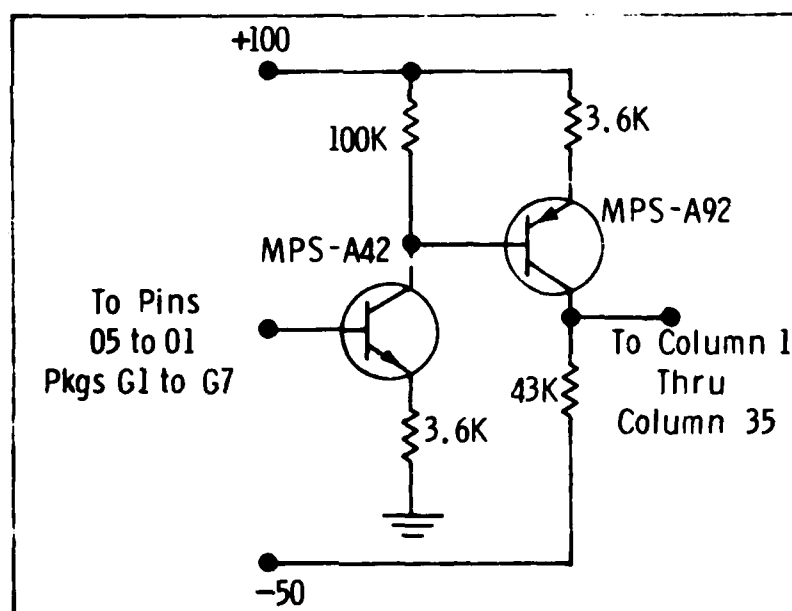


Fig. 9.5 – Row and column driver circuits for first alphanumeric TFFEL display exerciser

### 9.3 Viewability Exerciser

#### 9.3.1 Specifications and Characteristics

With reference to the required features and characteristics of an exerciser to drive the DMD display in accordance with the desired performance, the technical requirements document SCS-501 dated 2 May 1975 entitled "Thin Film Transistor Addressed Display" governs. The desired operational characteristics are described in Section 3.5, the display viewability in Section 4.5.2, and the power dissipation test in Section 4.5.3 of this document. These sections are reproduced below for reference:

#### 3.5 Operational Characteristics.

3.5.1 Electrical Input. - Signal and power input shall be accomplished by means of evaporated electrodes on the left and right sides and top or bottom of the display.

3.5.2 Display Recognition. Display characters shall be viewable and recognizable in an ambient light intensity of 2000 foot candle (fc) impinging upon the display) the display contrast ratio, defined as the ratio of the luminance of an "on" light emitting element in darkness, to the luminance of a neighboring "off" element or neighboring dark space (whichever is greater) should be 20 as a minimum. This shall be measured in accordance with the provisions of Paragraph 4.5.2.

3.5.3 Power Dissipation. At the luminances set to satisfy 3.5.2 with all resolution elements "on", power dissipation in the display panel shall not exceed 2.0 watts. With full power supplied to the panel, and all elements "off", power dissipation shall not exceed 1.0 watts. Thus, with all 256

characters "on" total power dissipation in the display will be less than 1.5 watt. This shall be measured in accordance with the provisions of Paragraph 4.5.3.

3.5.4 Electrical Drive. The side and bottom electrodes represent x-y addressing of any of the 77 by 222 or 17,094 resolution elements. Each resolution element shall contain two thin film transistors and one storage capacitor to provide the x-y function, to provide the electroluminescent drive, and to provide short term storage. The display shall be capable of presenting all 256 characters at a repetition rate as low as 30 frames per second.

4.5.2 Display viewability.

4.5.2.1 Display characters shall be inspected for recognition in an ambient light intensity of 2000 foot candles (fc) impinging on the display. All of the 256 available 5x7 dot configurations shall be checked for at least 2 of the set of 128 ASCII characters so that all characters are viewed and all dot configurations are checked. (See 3.5.2). Recognition shall be measured by presenting the ASCII characters on the display to 6 objective subjects, with no vision deficiencies. The characters shall be displayed in a random manner and a score of correct readings made. A maximum error rate of 3% is acceptable.

4.5.2.2 One of the 256, 5x7 dot configurations shall be checked for all ASCII characters. (See 3.5.2).

4.5.2.3 In normal room lighting, 50 fc impinging upon the display, the display contrast ratio (defined as ratio of luminance of an "on" light emitting element in



darkness to luminance of neighboring "off" element) shall be inspected at 9 positions equally spaced in the display. (See 3.5.2).

- 4.5.3 Power Dissipation Test. With all elements of the display turned on to satisfy 3.5.2 requirements, total power dissipated by the display shall be measured. With all elements off, and full power supplied to the display, power dissipation shall be measured. (See 3.5.3).

A viewability exerciser for evaluation of DMD display operation and performance was designed, built and used for these purposes. To demonstrate the display capability, this exerciser allows a full set of upper and lower case alphanumeric characters to be entered from a keyboard, provides various geometric test patterns, including all elements on, all off, bar and checkerboard patterns, and moving horizontal line or border between on/off regions, and the inverse of these characters or patterns, i.e., black on white background. Adjustable electroluminescent phosphor brightness and adjustable bias levels for the operating circuits are provided, as well as a measurement system for the dissipative electroluminescent power. In order to conduct viewability tests as outlined in Section 4.5.2 of SCS-501, a computer interface linked the exerciser to a Hewlett-Packard Model 2100-S, the computer attached to the Pilot Facility, thereby enabling automatic writing of single characters or character sequences in arbitrary positions on the panel, and automatic recording of the results of character viewing by various test subjects as they indicate character recognition by actuating appropriate keys on the entry keyboard.

#### 9.3.2 Operation

The viewability exerciser together with keyboard and DMD panel test fixture is shown in Figure 9.6, and an overall block diagram in Figure 9.7. The test fixture is connected to the exerciser by flexible ribbon cables and all the active electronic driving circuits are housed within the exerciser chassis. A closeup view of the control panel of the

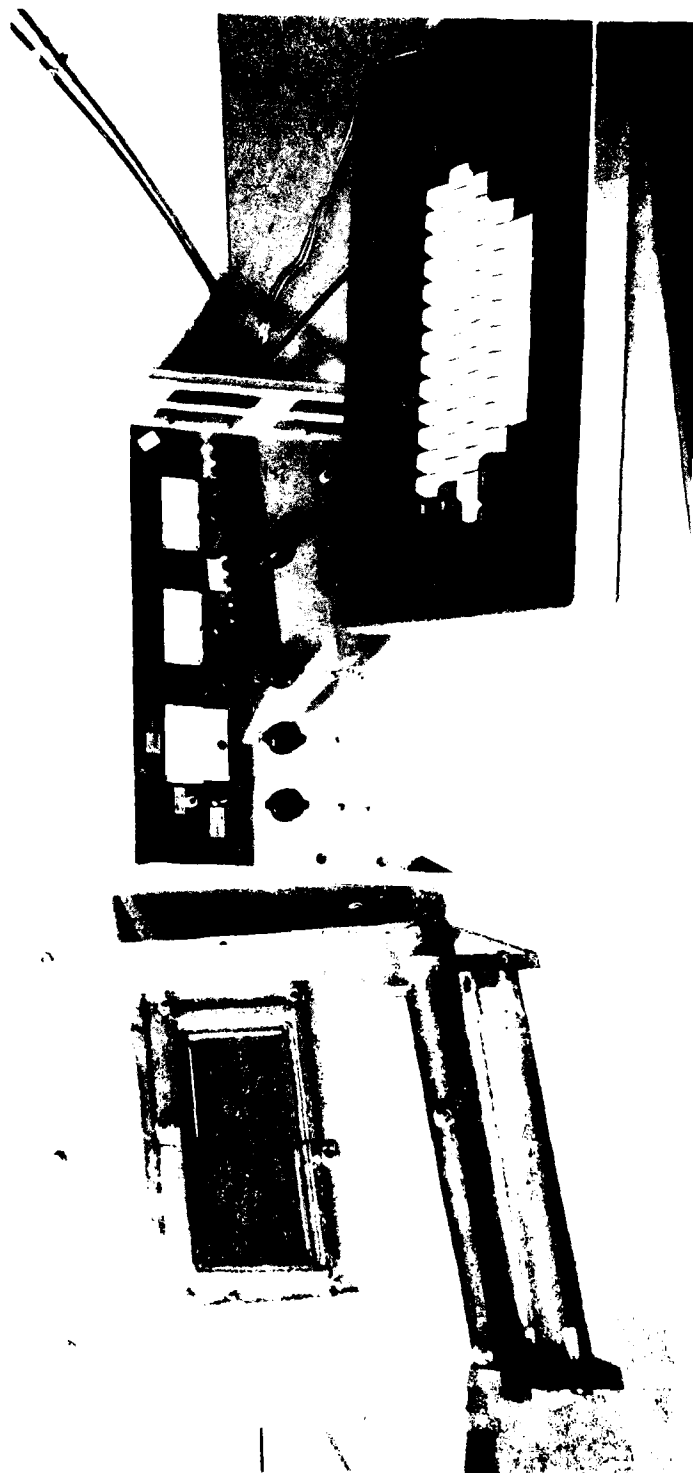


Figure 9.6 Viewability Test Setup, with DMD Panel in Test Fixture, Exerciser, and Keyboard

AD-A096 635

WESTINGHOUSE RESEARCH AND DEVELOPMENT CENTER PITTSBU--ETC F/6 13/8  
MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY--ETC(U)  
FEB 80 M W CRESSWELL, P R MALMBERG, J MURPHY DAAB07-76-C-0027

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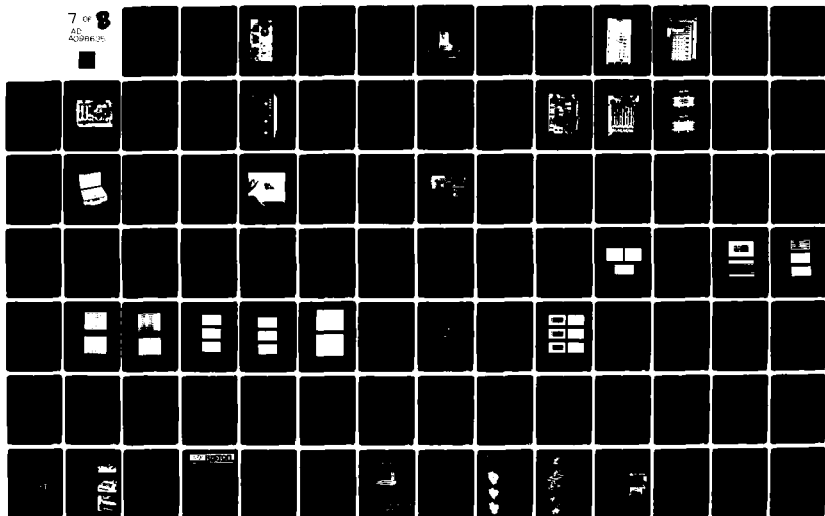
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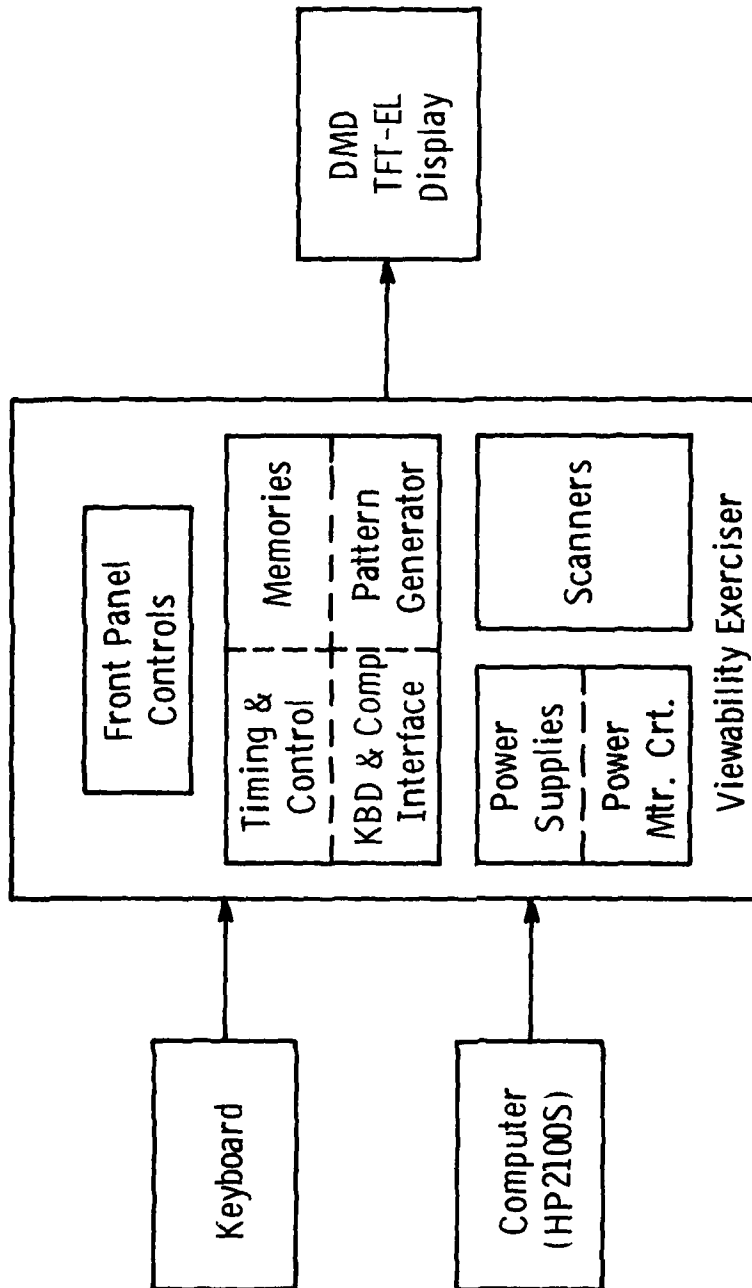


Fig. 9.7 -- Viewability test system, block diagram

exerciser is shown in Figure 9.8. The function of the various switches and controls are described in following Table 9.3.

Table 9.3

VIEWABILITY EXERCISER - FRONT PANEL CONTROL FUNCTIONS

<u>Label</u>	<u>Control</u>	<u>Function</u>
Pattern Select	8 position rotary switch	Selects various patterns
Column Shift	4 position rotary switch	First 3 positions are for column shift in AN character mode. Fourth position selects pattern mode.
Row Shift	4 position rotary switch	Provides 4 row shift positions.
DC Voltage Adjustment	4 potentiometers, 4 position switch, and meter	Adjusts SP-SN-GP-GN voltages over a 0-60V range; meter reads any one of the four as selected by the switch.
Pattern Select	2 position toggle switch	Inverts video for alternate rows of selected pattern.
Pattern Motion	2 position toggle switch	Controls motion of selected pattern; pattern stationary in UP position.
Repeat	3 position toggle switch	Repeats single characters entered from keyboard; momentary repeat (UP), single characters (MIDDLE), continuous repeat (DOWN).
Page	2 position toggle switch (momentary)	Starts entered message at the top left corner of panel.
Invert	2 position toggle switch	Inverts video for AN characters or selected pattern.
Keyboard-Computer	2 position toggle switch	Selects keyboard or computer entry.

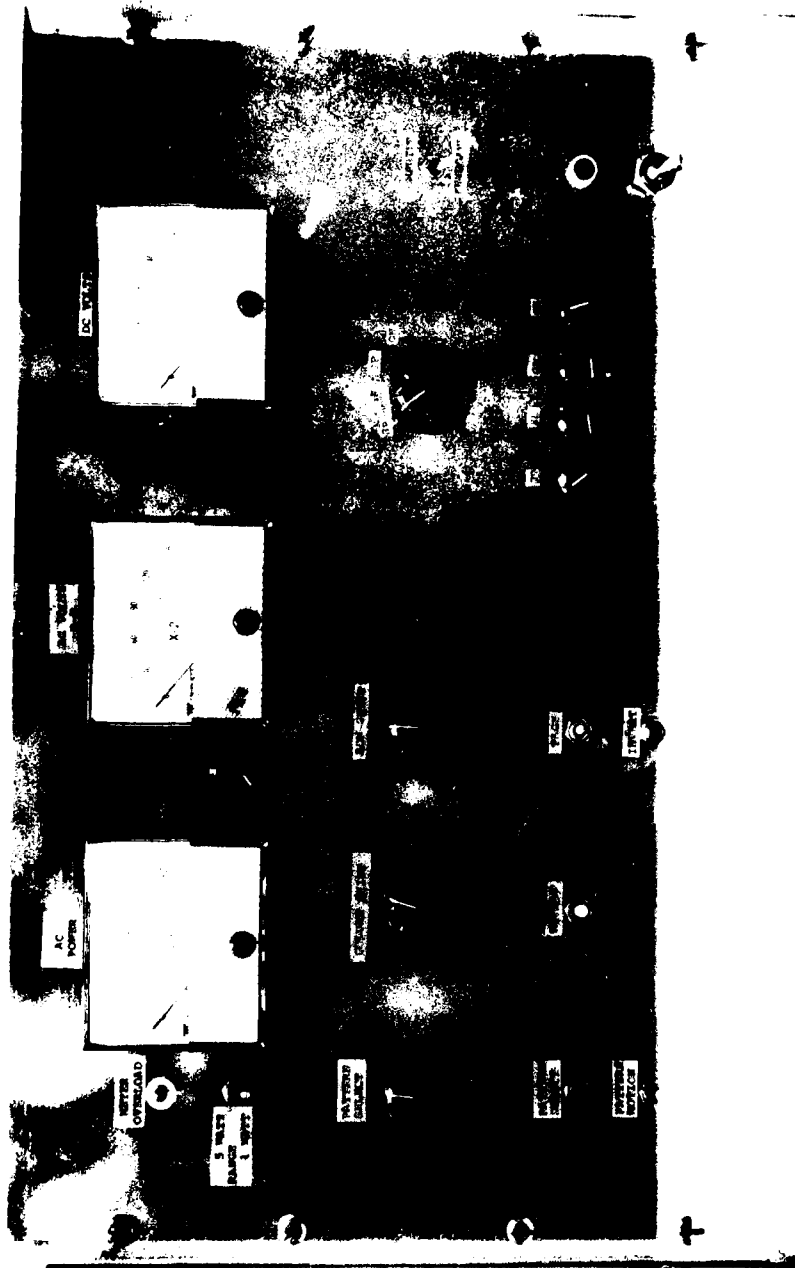


Figure 9.8 Viewability Exerciser, Control Panel

<u>Label</u> (cont'd)	<u>Control</u> (cont'd)	<u>Function</u> (cont'd)
AC Voltage	potentiometer and meter	Meter indicates P-P AC voltage (+ 2) applied to panel, adjusted by potentiometer.
AC Power	2 position toggle switch, meter	Indicates EL power consumed by panel; 1W and 5W full scale ranges selected by toggle switch.

When the exerciser is in the local or keyboard mode, alphanumeric characters entered from the keyboard are placed on the display in successive positions in each row and as each row is filled, a line feed and carriage return are effectively executed so the next character appears on the next line in the left-most position. To start a new set of characters at the left end of the first line, a homing instruction is executed by depressing momentarily the page toggle switch. Repetition of a single character is obtained by operating the repeat switch and then holding down the desired key on the keyboard. To obtain the various geometric patterns, the column shift control is placed in the extreme clockwise position and the desired pattern selected with the pattern select control. The pattern select and pattern motion toggle switches produce variations of the selected patterns.

In the computer mode, the exerciser accepts a seven bit ASCII code for the desired character and an eight bit character position address from the computer as well as a character strobe which places that information in the display refresh memory. When the viewability exerciser is used under computer control with the response of the test subject entered by keyboard, the keyboard used is that of a Hewlett-Packard Model 2640-B terminal which is tied into the HP 2100S computer. Viewability test software was developed to place random characters at chosen positions on the DMD panel, to record the keyboard responses of the test subject, to compare the responses with the displayed character, and to provide a suitable printout summarizing the test results for that subject.

A view of the back of the DMD panel test fixture is shown in Figure 9.9. This figure shows the printed circuit interface which extends from the panel to the ribbon cable connectors which are mounted on the reverse side of the mounting board and to the pins of which the printed circuit connector is soldered. The ribbon cable bundle which connects the panel test fixture to the exerciser consists of twelve 39-conductor ribbon cables which terminate at either end at ribbon cable connectors. The DMD panel is pressed and held against the printed circuit fingers by a transparent clamping frame secured by six wing nuts. A strip of resilient rubber is placed under the tips of the fingers so as to apply a continuous pressure of the finger on the DMD panel. Two sets of connections are provided, one for the right half of the DMD panel and the other for the left half of the DMD panel.

#### 9.3.3 Detailed Description

In Figure 9.10 is shown a detailed block diagram of the visibility exerciser wherein the basic blocks shown in the simplified block diagram of Figure 9.7 are expanded to show the functional components required to perform the various tasks of the major blocks. The design of the exerciser is governed largely by the organization of the character generator ROM (read-only-memory) which outputs five lines of video data for the five dots in the specific row of the alphanumeric character being called for by the seven bit ASCII code. This data is in turn distributed to the 160 dots in the 32 characters in each row as well as to the  $31 \times 2 = 62$  dots which serve as spacing between adjacent characters. A system clock which runs at about 500 kHz is counted down by an eleven bit binary display counter and by an eleven bit row counter. The display counter provides the character address to the display refresh memory and the character row address to the character generator ROM. The row counter provides the address of the dot row in the display being addressed and is decoded by a seven bit-to-seventy-seven line decoder followed by seventy-seven buffer amplifiers to drive the gate busses in the display. The video data output of the character generator ROM is presented in five bit



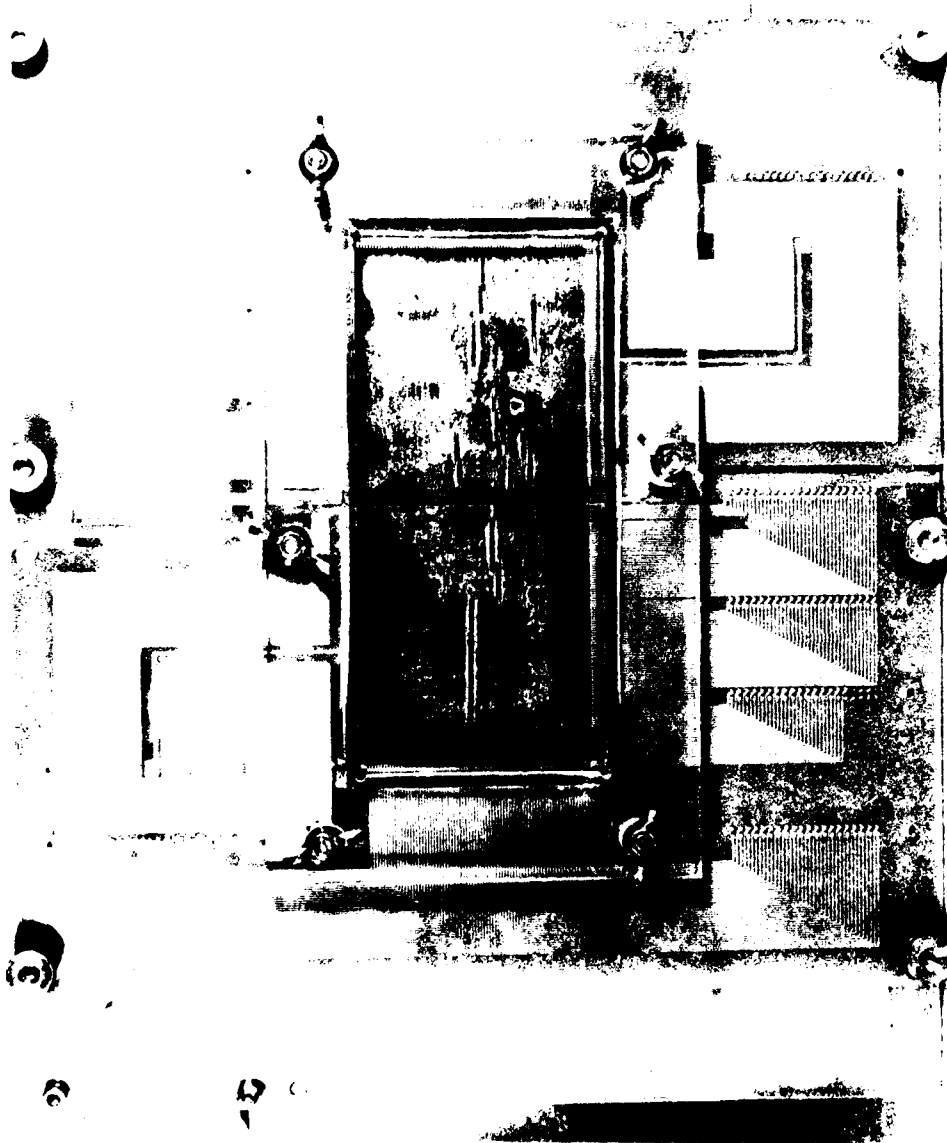


Figure 9.9 DMD Panel Test Fixture, Rear View

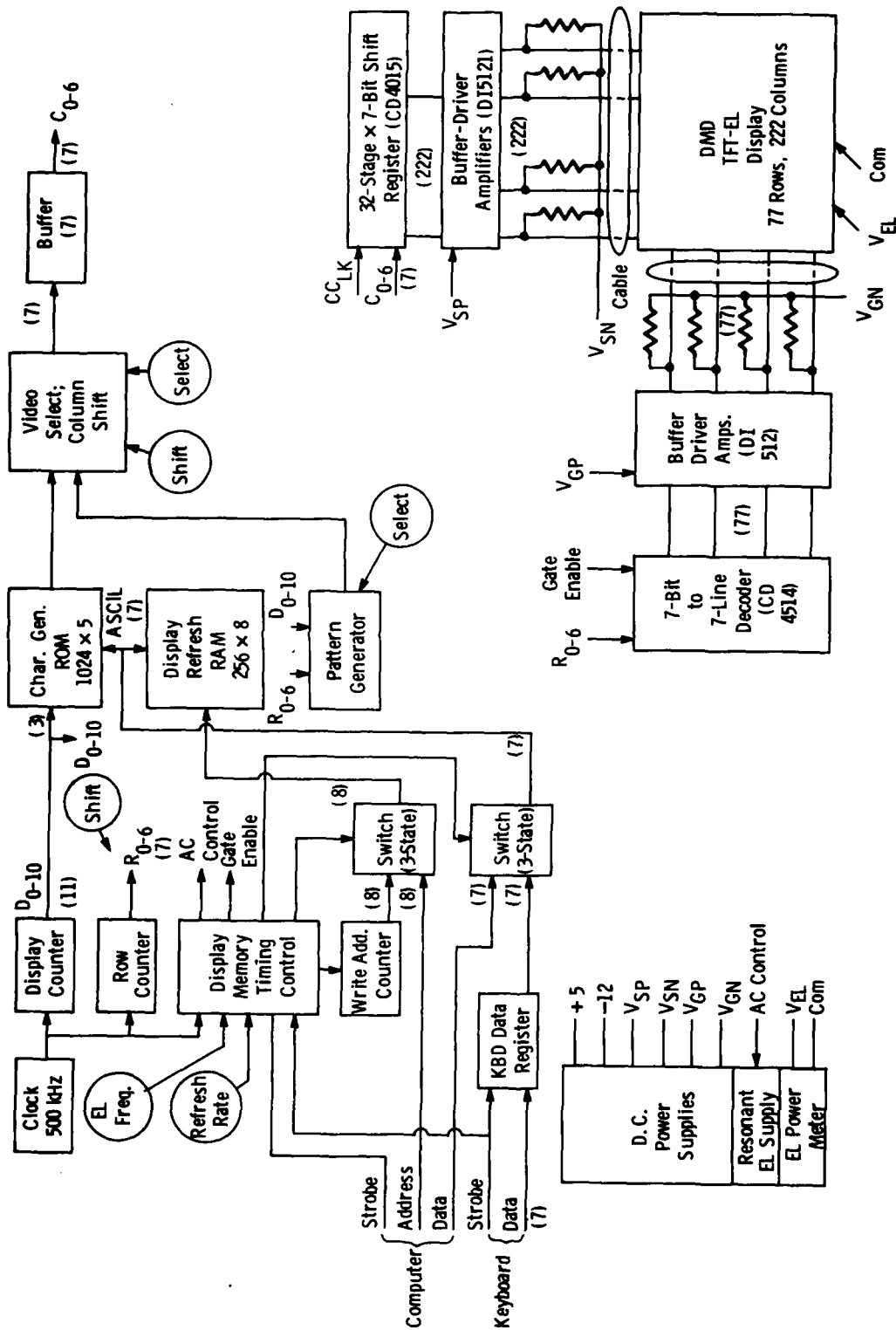


Figure 9.10 - Viewability exerciser, detailed block diagram

parallel format and is passed on to the horizontal scanner by way of a pattern selection switch and seven buffer amplifiers.

The horizontal scanner consists of a seven bit parallel by 32-stage shift register which is clocked at the character rate so that the five data bits plus the two spacing bits are loaded in sequence into the shift register. The latter is interfaced to the display by 222 buffer amplifiers which serve to drive the source busses in the array. A 100 kilohm resistor on each source bus is returned to the  $V_{SN}$  supply bus and provides the negative return for the source drivers. Similarly, 100 kilohm resistors are tied between each of the gate busses and the  $V_{GN}$  supply terminal to provide a negative return for the gate busses. After the data is shifted into the horizontal scanner, the clock is interrupted during the gate strobe, at which time the selected gate bus is driven positive to load the selected line of the display with the video information. The video selection switch allows either the character video information to be selected and passed on to the horizontal scanner or else the video signal supplied by the pattern generator. A set of seven inverters can be selected by a switch so as to provide either positive or negative video to the display.

The computer interface provision of the viewability exerciser permits computer-supplied character addresses and codes to determine the contents of the display refresh memory. Suitable buffer registers permit this to be done in synchronism with the internal timing of the exerciser. The logic circuitry, which includes the timing and control, keyboard and computer interface, memories, and pattern generator are mounted on one logic circuit board, shown in Figure 9.11. A separate circuit board contains the scanner or address circuitry and is shown in Figure 9.12.

Because the EL phosphor represents a load to the power supply consisting of primarily a large capacitance with a small lossy component, it is necessary to drive that EL load in a resonant manner so that the energy stored in the capacitance is not lost to switch resistances. In the present exerciser as in previous designs at this laboratory, this resonant drive is provided by a switched inductor as represented in the block diagram of Figure 9.13(a). Logic control signals designated ACP

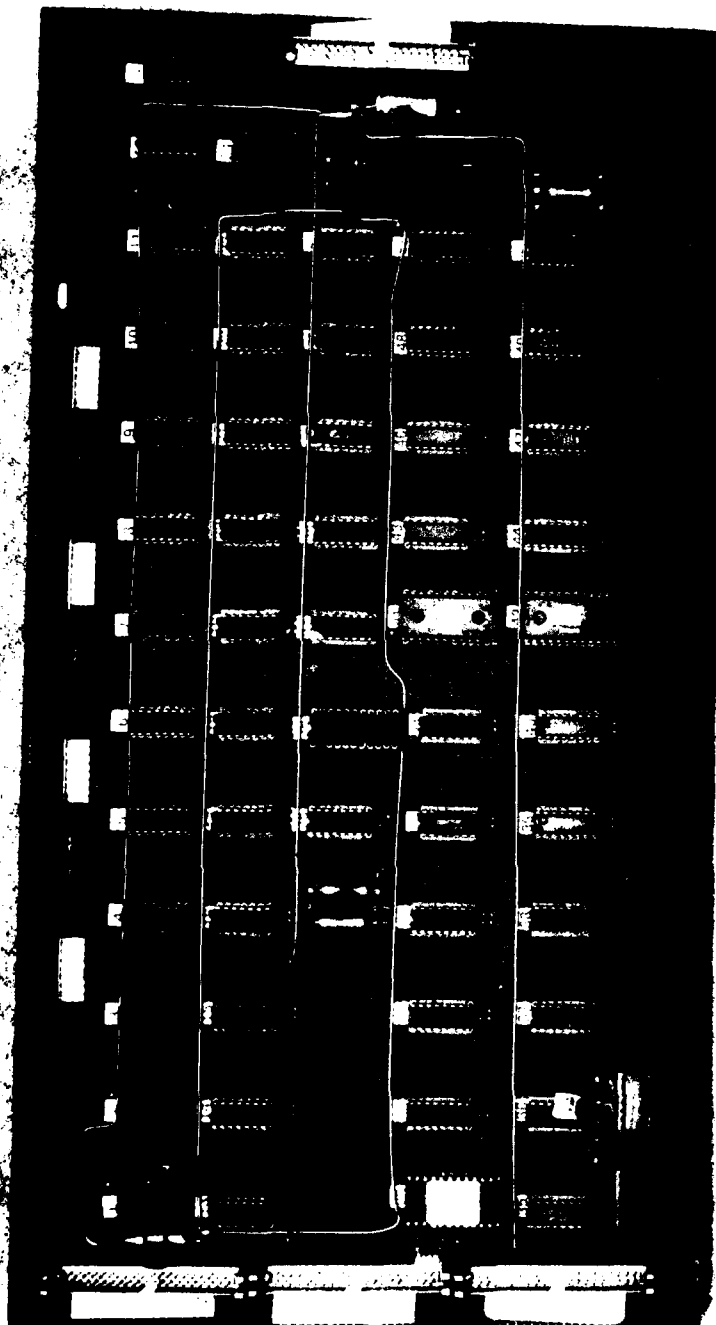


Figure 9.11 Viewability Exerciser - Logic Circuit Board  
(Timing and Control, Interface, Memory, Pattern  
Generator)

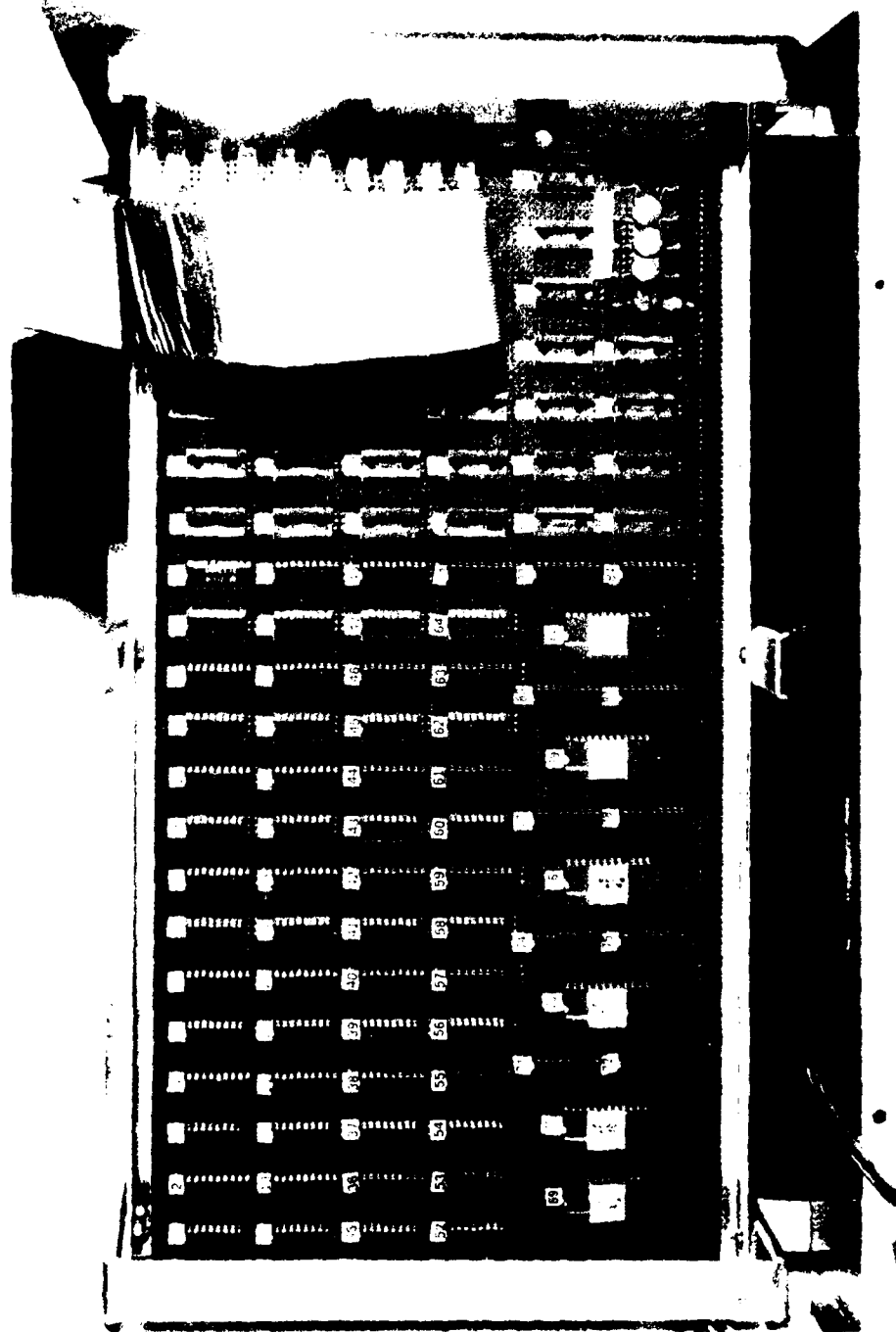
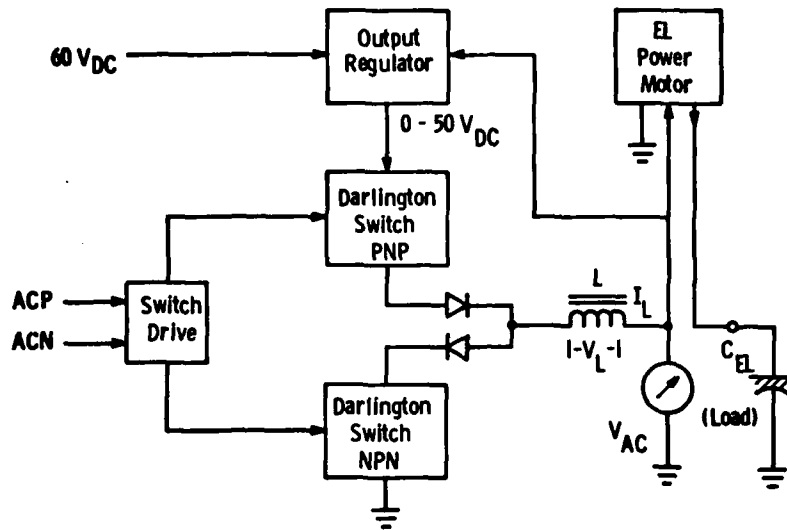


Figure 9.12 Viewability Exerciser - Scanner Circuit Board



(a) Block Diagram

Fig. 9. 13(a) — AC supply for EL phosphor

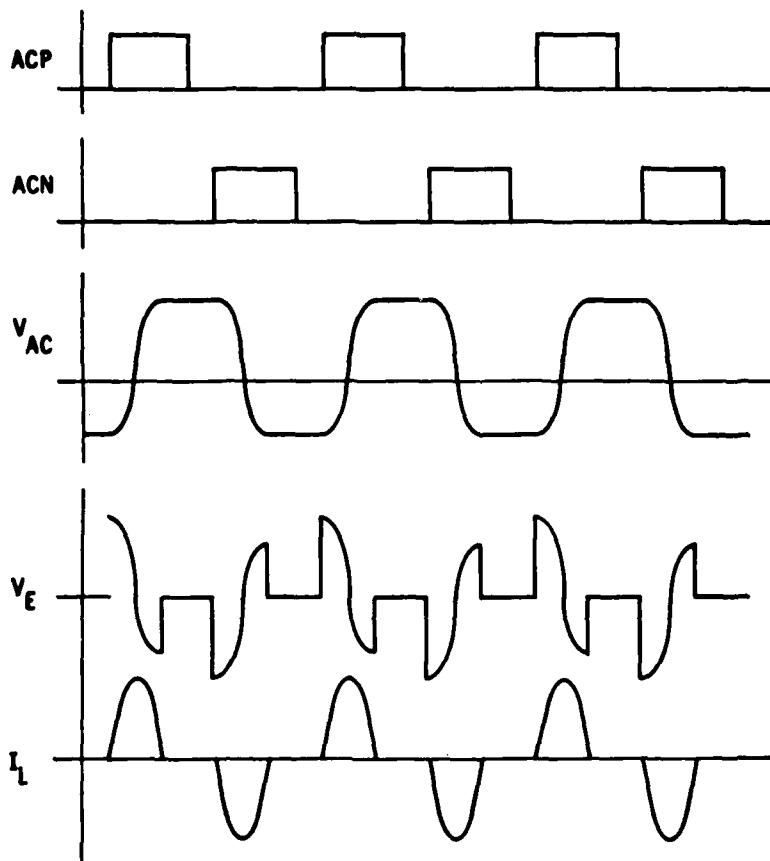


Fig. 9. 13(b) — Operating waveform

and ACN actuate in turn a PNP transistor switch to pull one end of the inductor in the positive direction and an NPN switch to pull it in the negative direction. These are non-overlapping waveforms which are separated by a short period to insure that each switch has time to come out of saturation before the opposing switch is turned on, thus affording high peak currents between the supply and ground. Isolating diodes between the switches and the inductor permit the inductor at each half-cycle to go to zero voltage at that time when the current reaches its zero value. Waveforms that describe the operation of the inductive supply are shown in (b). Losses in the load are made up by switching the inductor alternately to ground and to a positive supply voltage which is regulated to give the required AC output voltage. The power meter is inserted in series with the high potential lead of the power supply so that the ground return of the display will not be interrupted by any measuring device or shunt resistor. Basic circuit for the power meter is shown in Figure 9.14. A  $\pm 15V$  regulated and isolated power supply floats on the high voltage lead from the AC supply and powers an analog multiplier which multiplies a potential taken from the voltage divider  $R_{DH}$  and  $R_{DL}$  and a voltage taken from a current shunt -  $R_{S1}$  or  $R_{S1}$  in parallel with  $R_{S5}$  - thereby providing two ranges of power measurement for the EL power. A calibrating resistor  $R_{cal}$  is provided to enable the meter to be calibrated against a known resistive load. Overall accuracy of the meter when used with the non-linear EL load is estimated to be about  $\pm 2\%$ . A photograph of the power metering circuit board is shown in Figure 9.15.

Dwg 17.1A61

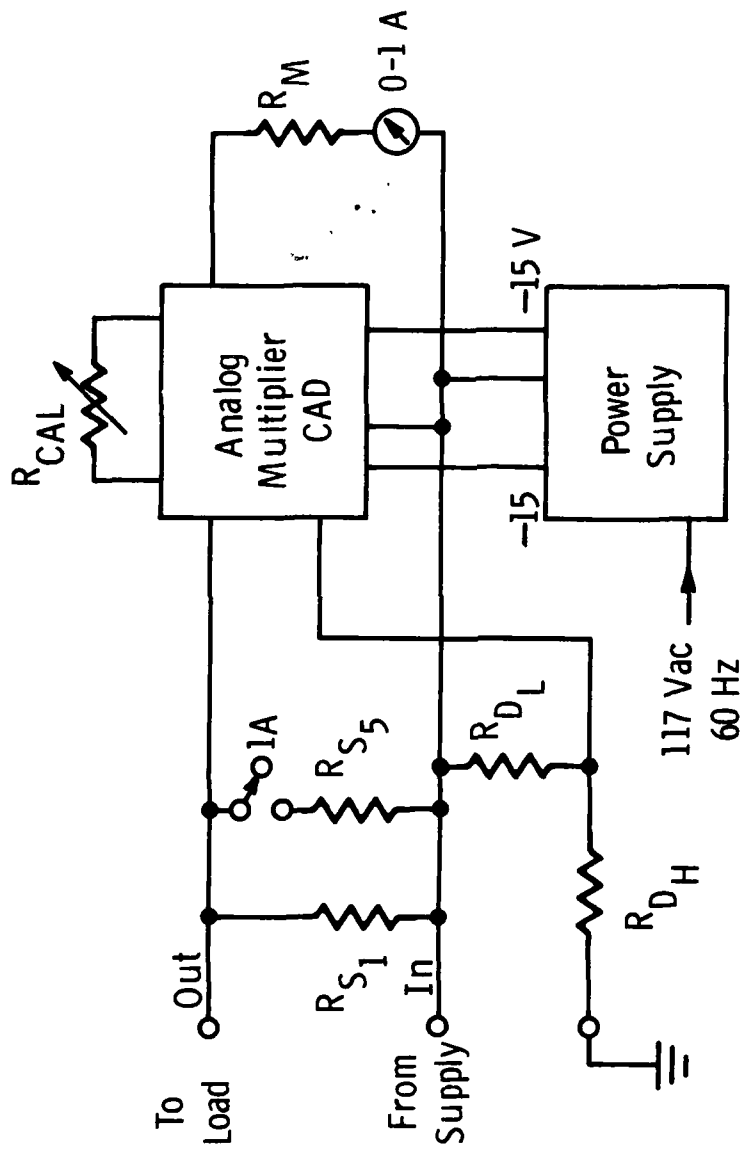


Fig. 9. 14 — AC power meter — basic design



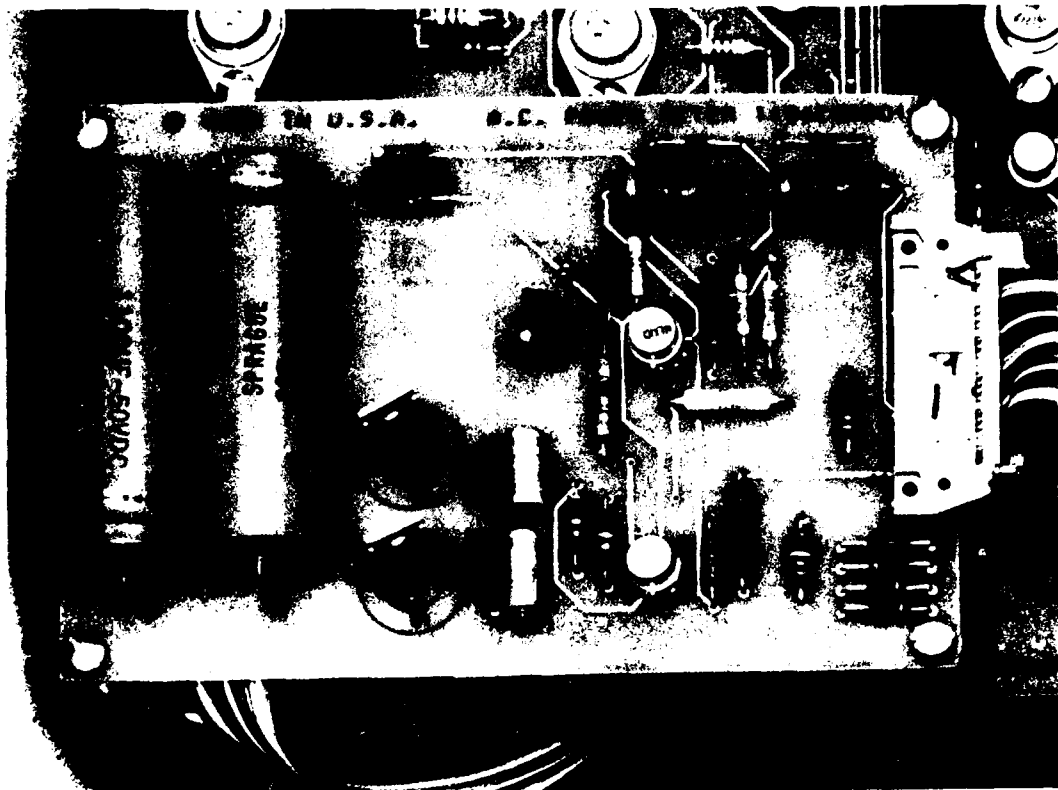


Figure 9.15 AC Power Meter Circuit Board

Detailed schematic diagrams for the viewability tester consist of a set of six drawings as listed in the following table.

Table 9.4

Viewability Tester Schematic Drawings

<u>Title</u>	<u>Drawing Number</u>
1. Logic Board	1290J32
2. Driver Board	1290J31
3. AC Power Supply	8534D50
4. DC Power Supplies	1688D85
5. AC Power Meter	1154C08
6. Chassis	2626C18

In addition to the AC power supply for the EL phosphor, regulated DC supplies for +5 volts logic, -12 volts logic,  $V_{sp}$ ,  $V_{sn}$ ,  $V_{gp}$ , and  $V_{gn}$  are included in the exerciser chassis to power the various functions.

#### 9.4 On-Off Exerciser

For the purposes of testing DMD prototype panels for performance under various environmental conditions a minimal test apparatus was required that would effectively simulate actual operating conditions of the display but would not involve the complexity of providing alphanumeric information on the display. For this purpose an On-Off exerciser was designed to be used in conjunction with a test stand in which the DMD panels were mounted and connected in such a fashion that all of the gate buses were joined to a single bus and all of the source buses were likewise joined to a single bus. The control signals provided these two buses consisted of either an all-On or an all-Off video signal for the source buses and a writing or positive pulse for the gate buses. Different repetition frequencies and duty cycles are selectable which simulate the type of signal a single gate bus would be driven by in an operating alphanumeric display. The On-Off exerciser therefore includes the various power supplies, power meter, and timing circuits necessary to drive the DMD panel in this simplified mode. A photograph of the front panel of the On-Off exerciser is shown in Figure 9.16. The three meters on the panel (reading from left to right) display ac power to the panel in two scales: 1 watt or 5 watts full scale, ac volts: 0-150 rms, and bias voltages of 0-50 volts for each of four supplies, selected by the switch underneath. The other controls are a five-position gate pulse frequency selector switch at the left and next to it a nine-position duty cycle switch. Tables 9.4.1 and 9.4.2 give the repetition frequencies and duty cycles for various positions of these two controls. At the lower part of the panel is a control for the ac voltage and four controls for the bias settings. A block diagram of the On-Off exerciser is shown in Figure 9.17. Two oscillators or clocks are used to determine the frequency of the ac voltage

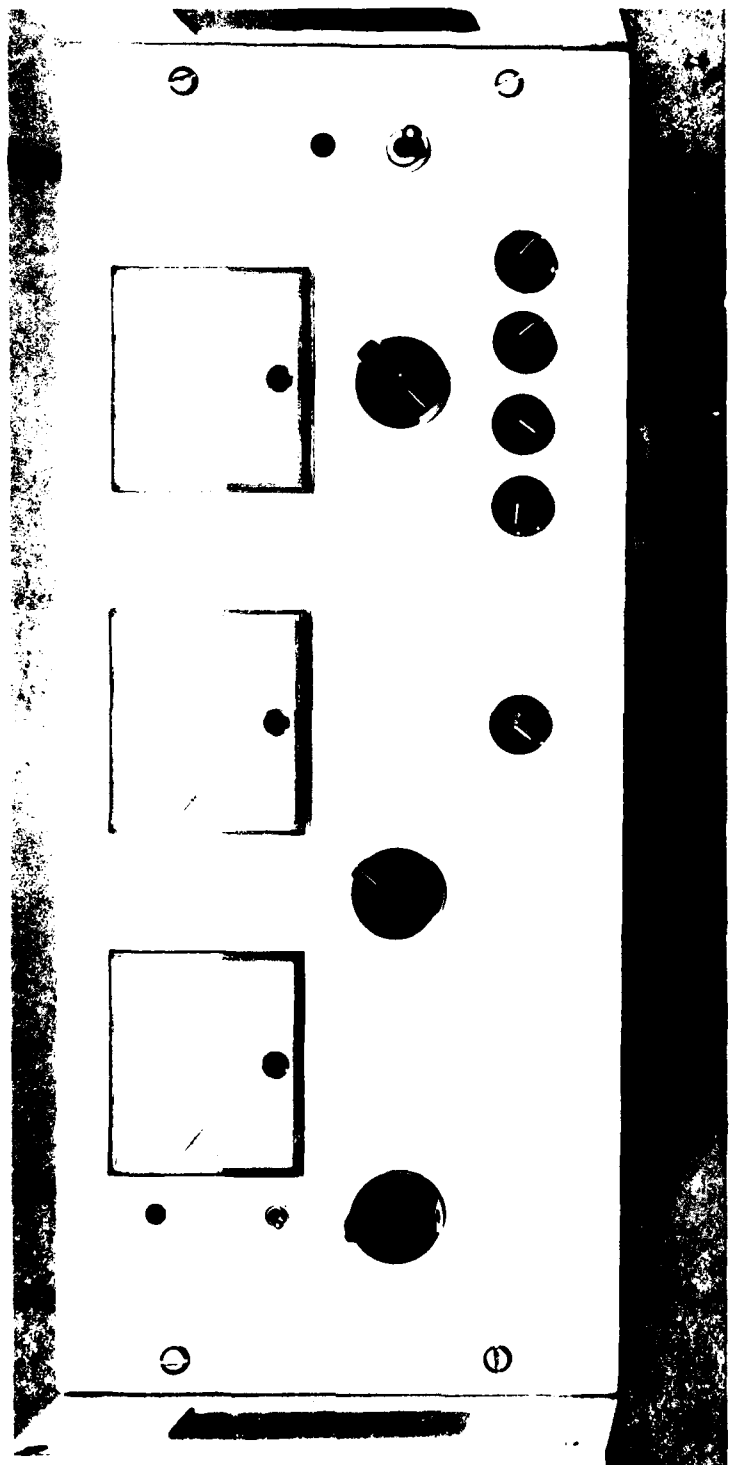


Figure 9.16 ON-OFF Exerciser, Control Panel

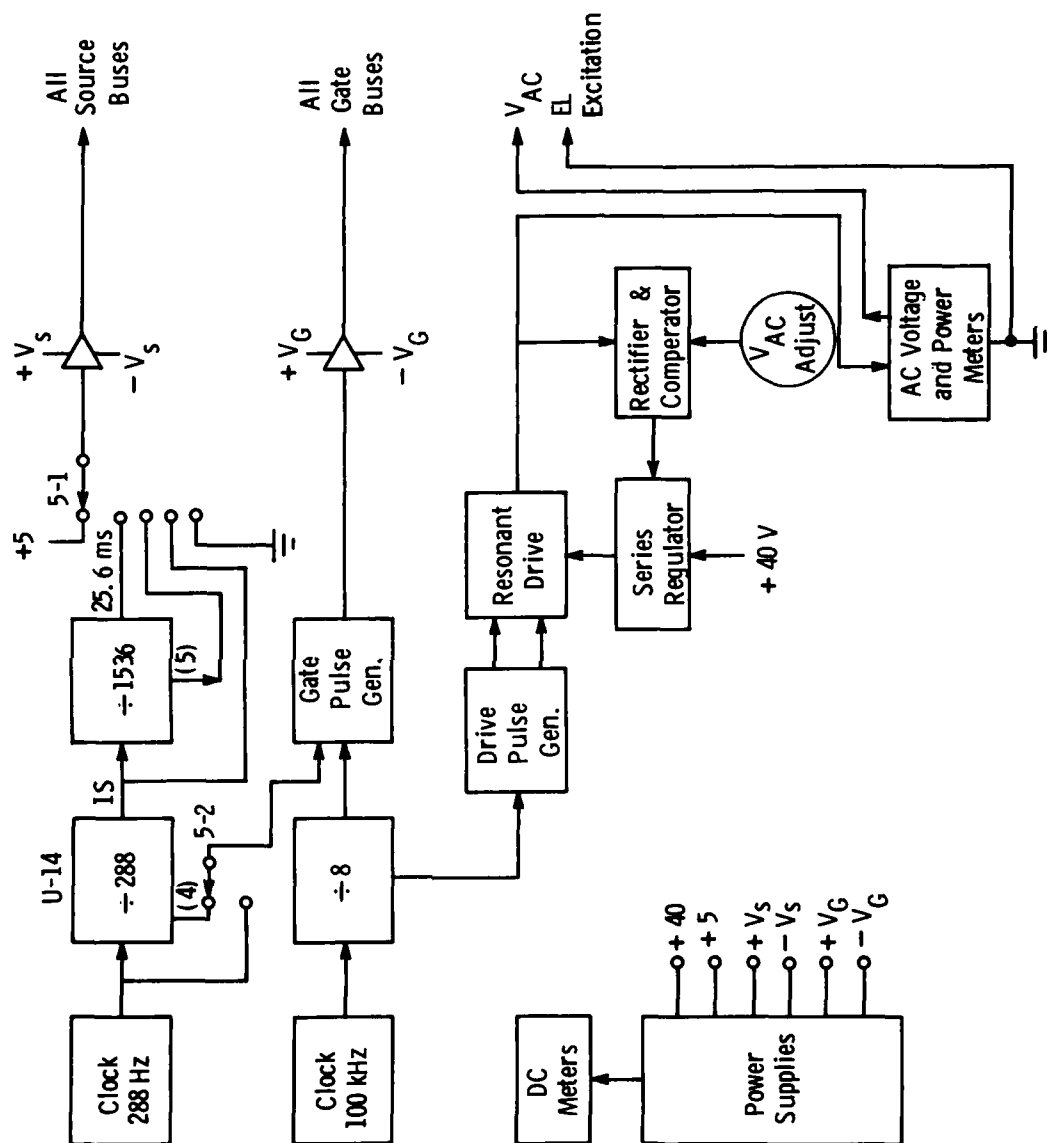


Fig. 9.17 - On-off exerciser, block diagram

supply, the rep rate of the gate pulses, and the On-Off duty cycle of the video data fed to the source buses. Figure 9.18 shows the basic On-Off waveforms thus provided to the source buses in tandem and to the gate buses in tandem. The On-duty cycle is given by the ratio of  $\tau_1/\tau_1 + \tau_2$  as shown in Table 9.6. The gate pulse repetition frequency is given by  $1/\tau_g$  and the various choices are listed in Table 9.4.1. The AC power supply, the DC power supplies, and the AC power meter circuits are all identically the same as those used in the viewability tester described in the previous section. Figure 9.19 shows the top view of the circuit board which contains the timing and logic and the AC power supply. The resonating inductor is a ferrite pot core in a metal case shown at the right of the board. The DC power supplies are mounted on a single circuit board which is shown in Figure 9.20. The DMD panel test fixture for the parallel source and parallel gate drive used with the ON-Off tester is shown in Figure 9.21 (a) rear view and (b) front view. Schematic diagrams for the On-Off exerciser are listed in Table 9.7.

TABLE 9.5  
GATE PULSE REPETITION FREQUENCY

<u>Switch (S-2)</u> <u>Position</u>	<u>Frequency (<math>1/\tau_g</math>)</u> <u>(sec<sup>-1</sup>)</u>
1	144
2	72
3	36
4	18
5	288

TABLE 9.6

## ON-OFF EXERCISER - ON DUTY CYCLE AND PERIOD

<u>Switch (S-1)</u> <u>Position</u>	<u>Duty</u> <u>Cycle</u>	<u>Period</u> <u>(Sec)</u>
	$\frac{\tau_1}{\tau_1 + \tau_2}$	$\tau_1 + \tau_2$
1	1.0	$\infty$
2	0.5	4
3	0.5	8
4	0.5	16
5	0.5	2
6	0.9	1
7	0.5	32
8	0.2	1536
9	0.0	$\infty$

TABLE 9.7

## ON-OFF EXERCISER - SCHEMATIC DIAGRAMS

<u>Title</u>	<u>Drawing Number</u>
Logic Circuits and AC Power Supply	1688D98
DC Power Supplies	1688D85
AC Power Meter	1154C08

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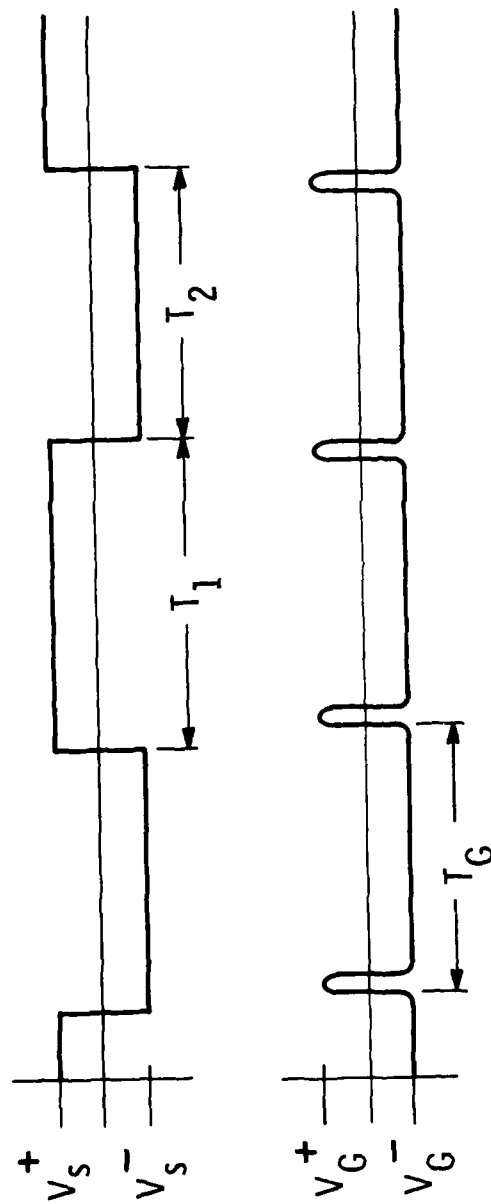


Fig. 9.18 ~ On-off exerciser ~ source ~ gate timing waveforms



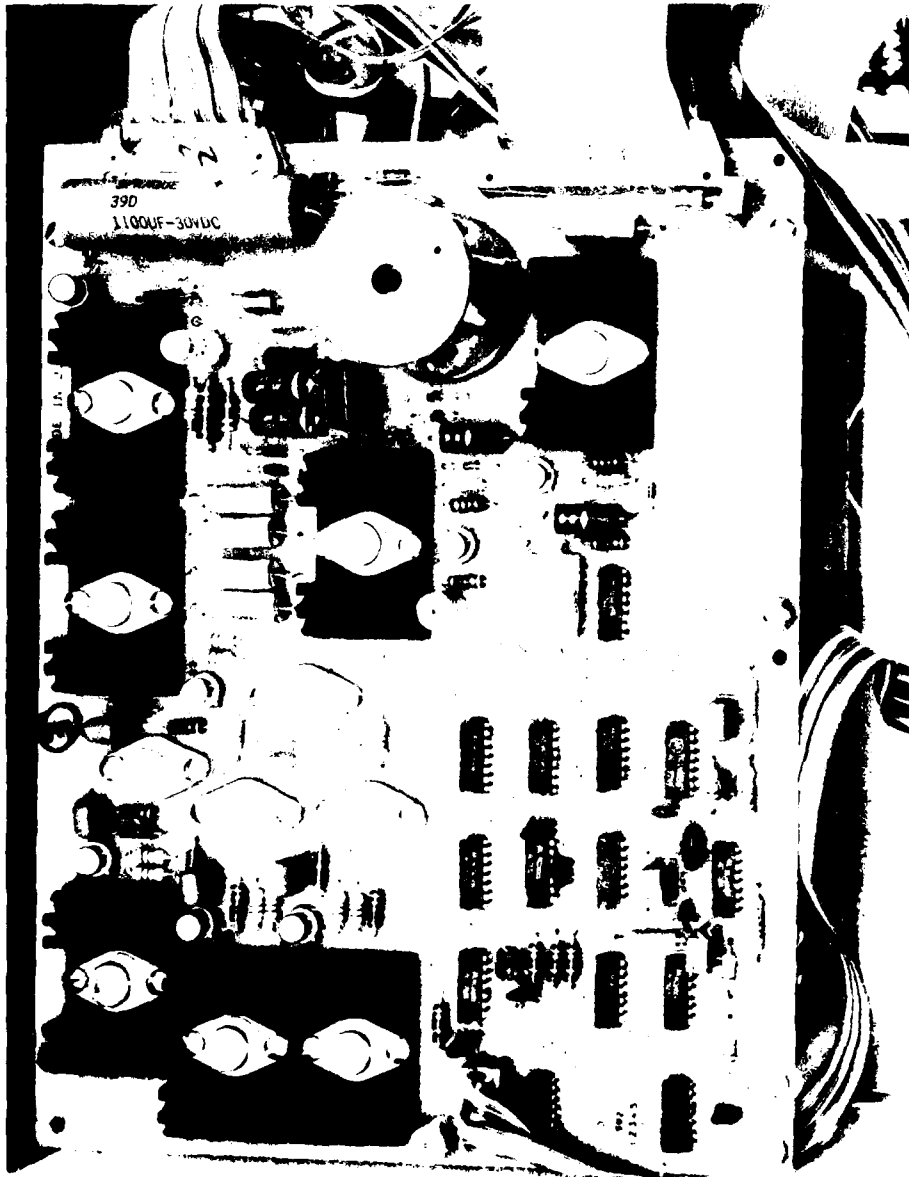


Figure 9.19 ON-OFF Exerciser, Logic and AC Supply Board

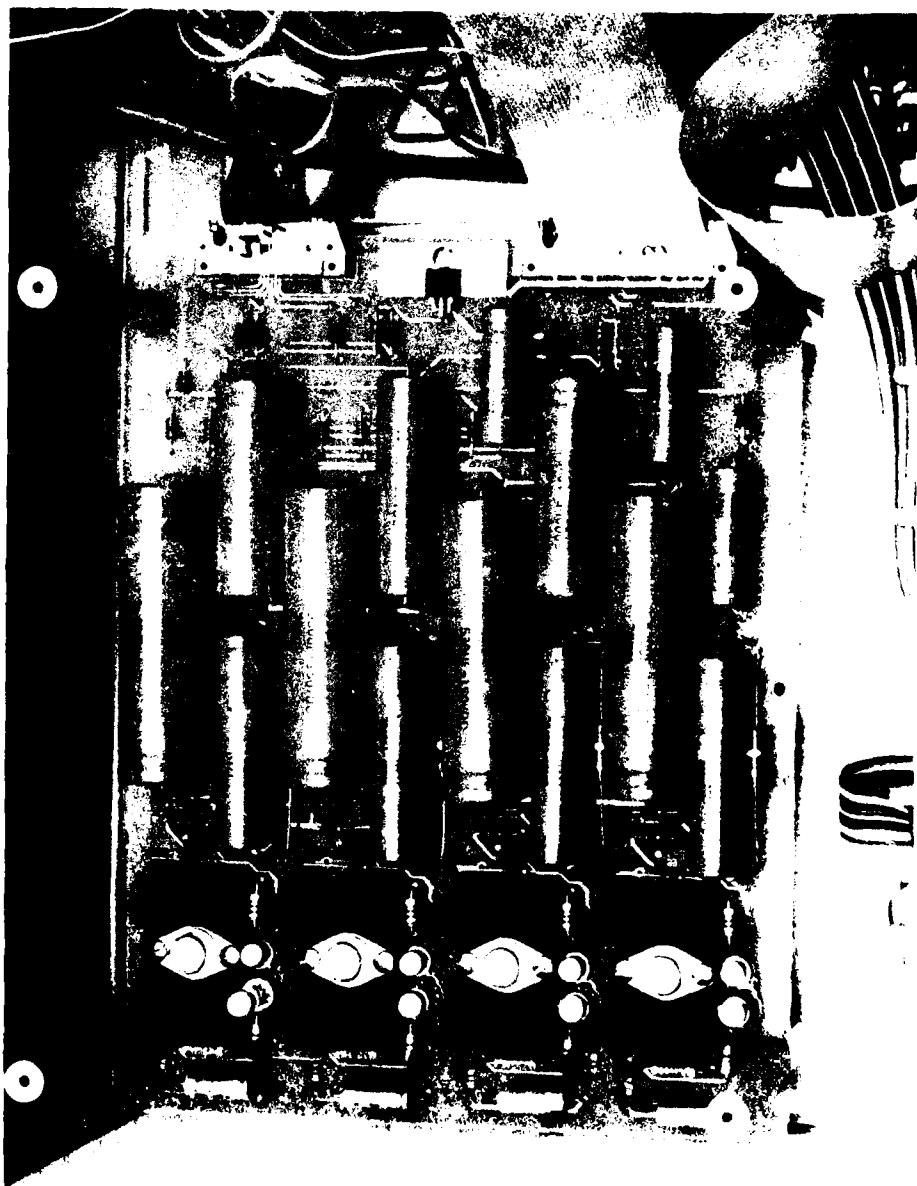
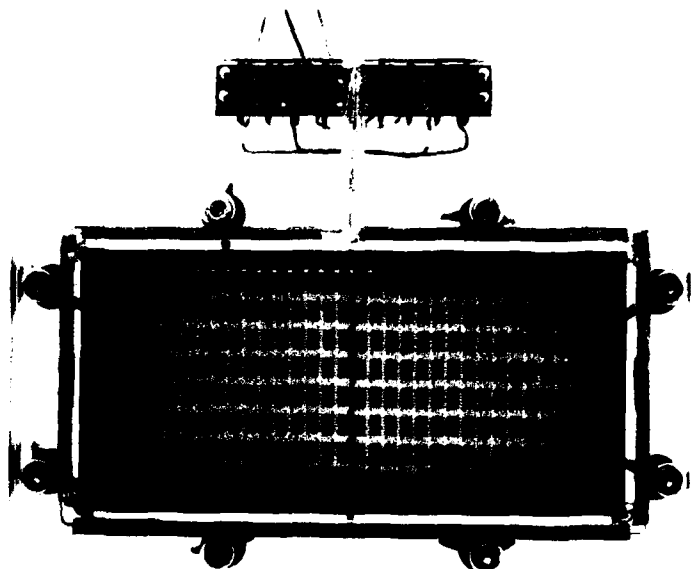
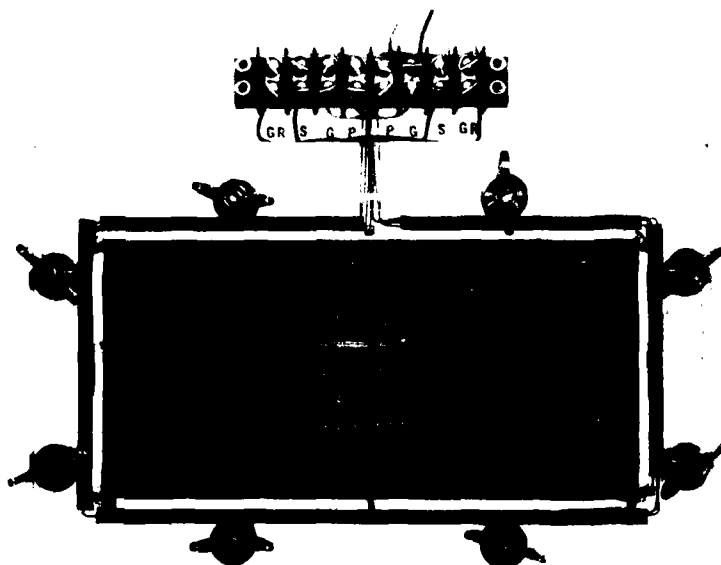


Figure 9.20 ON-OFF Exerciser, DC Power Supply Board



(a) Rear view



(b) Front view

Figure 9.21 Panel mount, ON - OFF Exerciser

### 9.5 The New Exerciser

The experience gained in developing various TFT-EL display exercisers and demonstrators has given rise to a better understanding of the needs and capabilities of these panels and how to drive them to the best advantage. In particular, the use of driving waveforms for the EL excitation properly coordinated with logic waveforms for gate and source buses has been shown to result in greatly improved operation of the display, reduced driving voltages for these buses and much greater latitude for the positive and negative rail potentials for the corresponding drivers or scanners. Especially instructive were the results of two programs undertaken to provide display demonstrators - Army contract DAAB07-77-C-0905, Multi-legend Display Switch, and MIT purchase order No. SR-33810, Monochrome Display Panel. In the first named program a concept of stabilizing the operation of the TFT s in the display matrix was first employed. The idea is to ensure that every TFT is operated periodically with the gate positive as well as negative with respect to the source, regardless of the message content of the display. The logic or switch transistors in the matrix already operate in this fashion inasmuch as most of the time they are in the OFF condition and are turned ON only during the time the gate bus for a particular line is pulsed positively. The power transistors on the other hand may remain in either the ON or OFF condition for long periods of time in the case of the display of a fixed message, and the gradual drifts which still exist in present day TFT s may over a period of hours cause the display to lose contrast. The method employed is illustrated by Figure 9.22 which shows the relationship of the excitation voltage to the waveforms imposed on the source and gate buses. When the high voltage excitation is in the most negative point of its swing, where it remains for some 50 microseconds, all source buses are raised to the logic 1 level which impresses a positive gate voltage on the power transistors in the addressed row for that period of time. However, no light is emitted by the electroluminescent elements at this stage because during the negative swing of the excitation voltage, the drain to source voltage is very low. Thus

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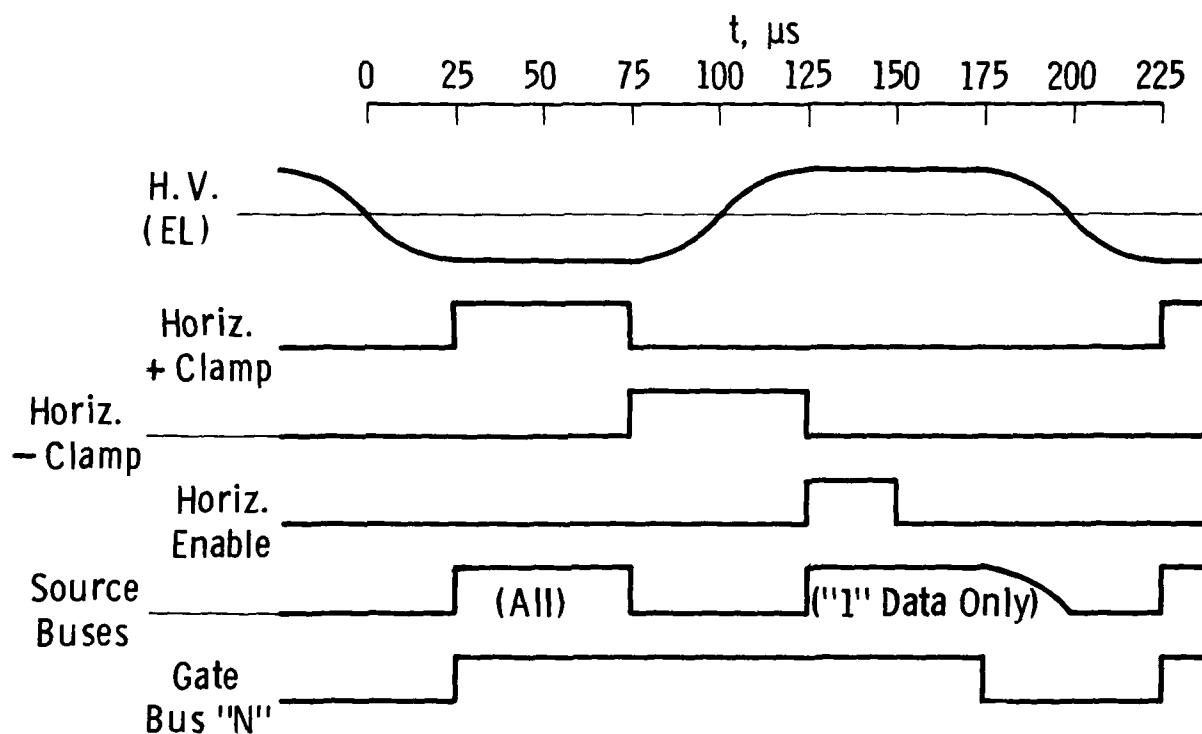


Fig. 9.22 — EL excitation, gate bus , and source bus waveforms for stabilizing TFT operation.

whether the transistors are previously ON or OFF, turning them ON at this time does not involve a significant swing in voltage applied to the electroluminescent phosphor and therefore no light is emitted. During the transition of the excitation from the low level to the high level, all source buses are held in the 0 logic state and all power transistors in the addressed row are turned OFF for the 50 microsecond period. Thus, in each frame refresh time, each row of display elements is written to a logic 1 for 50 microseconds and then to a logic 0 for 50 microseconds, thereby fully exercising the output transistors in both gate positive and gate negative conditions once per frame. Finally, during the positive quiescent state of the phosphor excitation waveform, the source buses are brought to the logic 1 and 0 state required for the current display, and just before the following negative transition of the excitation waveform, the gate bus is returned to the negative state and the logic or switch transistors are returned to their OFF condition for the addressed row. A photograph of the equipment first using this method is shown in Figure 9.23.

The second program mentioned had as its objective the design and fabrication of a television type display using a TFT-EL panel of a type previously developed under Army contract and displaying 128 lines of 160 elements each, at 30 elements per inch spacing. During the design of this unit it was felt that inasmuch as the TFT's used in the array can be switched between the full OFF and full ON states with only a small voltage swing on the gate, it should be possible to design control and scanner circuitry that could be operated at fairly low logic and signal levels, basically within the 0 to +18 volt range of conventional CMOS circuits. Such operation was, in fact, obtained during this program. It was found that in order to avoid the induced transients in the bus systems of the display due to the high voltage, high frequency waveform existing on the phosphor excitation electrode, as discussed earlier in Section 2.4, it was necessary to perform all logic operations or writing of video information into the display during that part of each line period during which the excitation

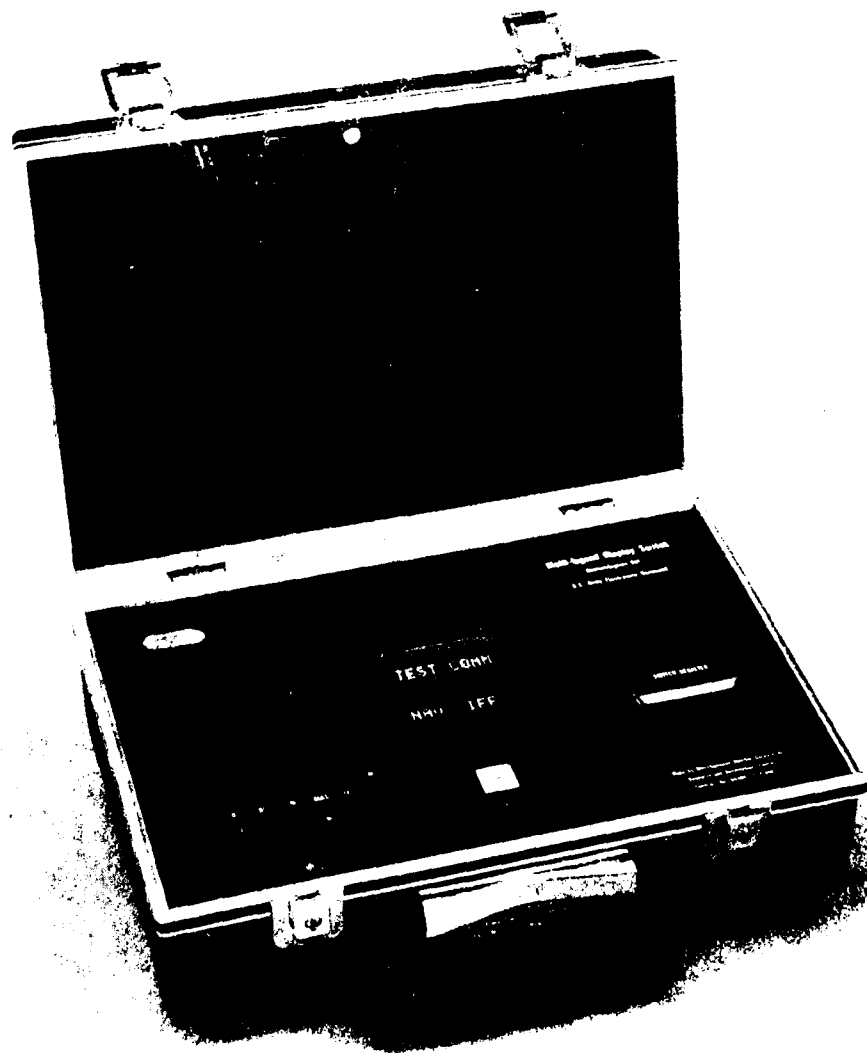


Figure 9.23 M-3 Demonstration Set

waveform was held at a quiescent, negative level. After the writing of each line is completed, the phosphor waveform executes a full sinusoidal excursion from the negative point to the positive point and back again before the next line is addressed. By this means, a very significant improvement in the performance of this panel was obtained, as compared with all previous methods of exercising TFT-EL panels. The most striking result, apart from the ability to run the source and gate buses within the 0 to +18 volt swing obtainable with commercial CMOS integrated circuits, was the ability to store a TV frame with full grey scale on the panel for upwards of thirty seconds, simply by interrupting the frame write operation. Since the brightness levels for the various picture elements are determined by the voltages stored on the capacitor in each cell, the fact that these voltages did not change by more than 1 volt during that period was clear evidence that the logic or switch transistors, when operated in this fashion, exhibited a leakage or OFF current of only one picoampere ( $10^{-12}$  A). The relative timing of the EL excitation waveform and the video distribution and gate bus bar waveforms are shown in Figure 9.24. In the TV panel the video information is stored on the stray capacitance of each vertical source bus bar by means of a commutation sequence which couples the video bus to each of the source buses in turn. When all source buses have thus been written with the appropriate video signal levels, the gate bus is pulsed ON to transfer those levels from the source buses into the cell capacitances of the addressed line. All of this takes place while the EL excitation remains at the most negative value in a quiescent state. Thus, even small voltages which might be induced in the source buses (which in this instance are left floating during the distribution of the video information) is eliminated and essentially zero effect of the EL excitation on the picture grey scale is served. A photograph of this panel showing a TV image which was held static for some ten seconds during the time exposure is shown in Figure 9.25. It was immediately evident that the ability to store video information within each cell for many seconds implied a capability for TFT-EL panels of this type to be refreshed at very low frame rates without flicker. This capability,



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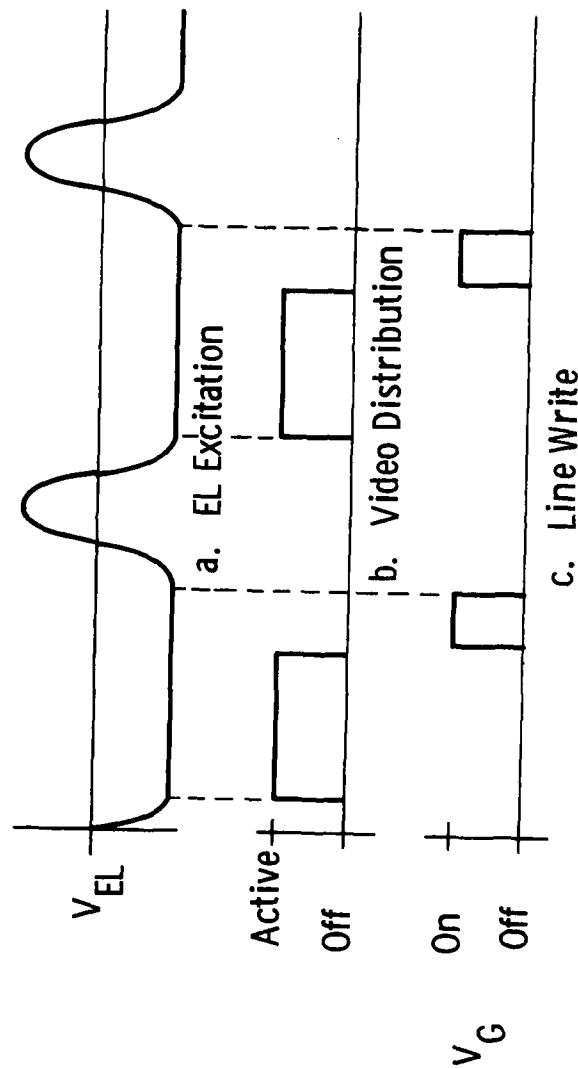


Fig. 9.24 — Timing of EL excitation and logic operations to minimize interrogation beebers



Figure 9.25 TFT-EL Panel with Stored TV Frame

combined with the relatively low logic levels needed to control the panel, would permit low power CMOS circuits and low data rates to be used with a message display and thereby permit the use of the TFT-EL panel at a total power level essentially equal to that required by the phosphor alone. A breadboard prototype of a DMD half-panel exerciser designed to take advantage of this operation strategy was designed and built. A block diagram for this exerciser is shown in Figure 9.26. As part of the plan to minimize power in peripheral circuits, EPROM's which could be held in a low-power standby mode when not accessed were programmed (1) as a character generator to convert from ASCII code to 5 x 7 dot character video, and (2) with ASCII data for 8 pages of text to serve as a built-in source of display material.

A photograph of the breadboard is shown in Figure 9.27. The CMOS integrated circuits used in the source and gate bus drivers, i.e. serving as horizontal and vertical scanners, were 32-line liquid crystal display drivers type HLCD0438 made by Hughes Aircraft. Unfortunately, the impedance of the output lines of these circuits was quite high, namely more than  $10^5$  ohms, and excessive electrostatic pickup from the EL excitation electrode was experienced even though the operating strategy described earlier and illustrated in Figure 9.24 was employed. The result of this interference was to prevent the display from being operated satisfactorily except at very low brightness levels at which the excitation voltage was small enough that these effects did not predominate. Several ways of overcoming this difficulty are possible, the most obvious being to replace the 32 line LCD driver trips with lower impedance output shift and store chips which are also available but at fewer lines per package. Inasmuch as part of the induced voltage arises from a slow ascending ramp of voltage on the EL phosphor during the logic operation due to leakage in the phosphor, a second alternative is to use a transistor switch to clamp the EL waveform to the most negative level during the logic operations. During the course of this program, neither of these solutions could be applied. Nevertheless, with the knowledge gained on how this

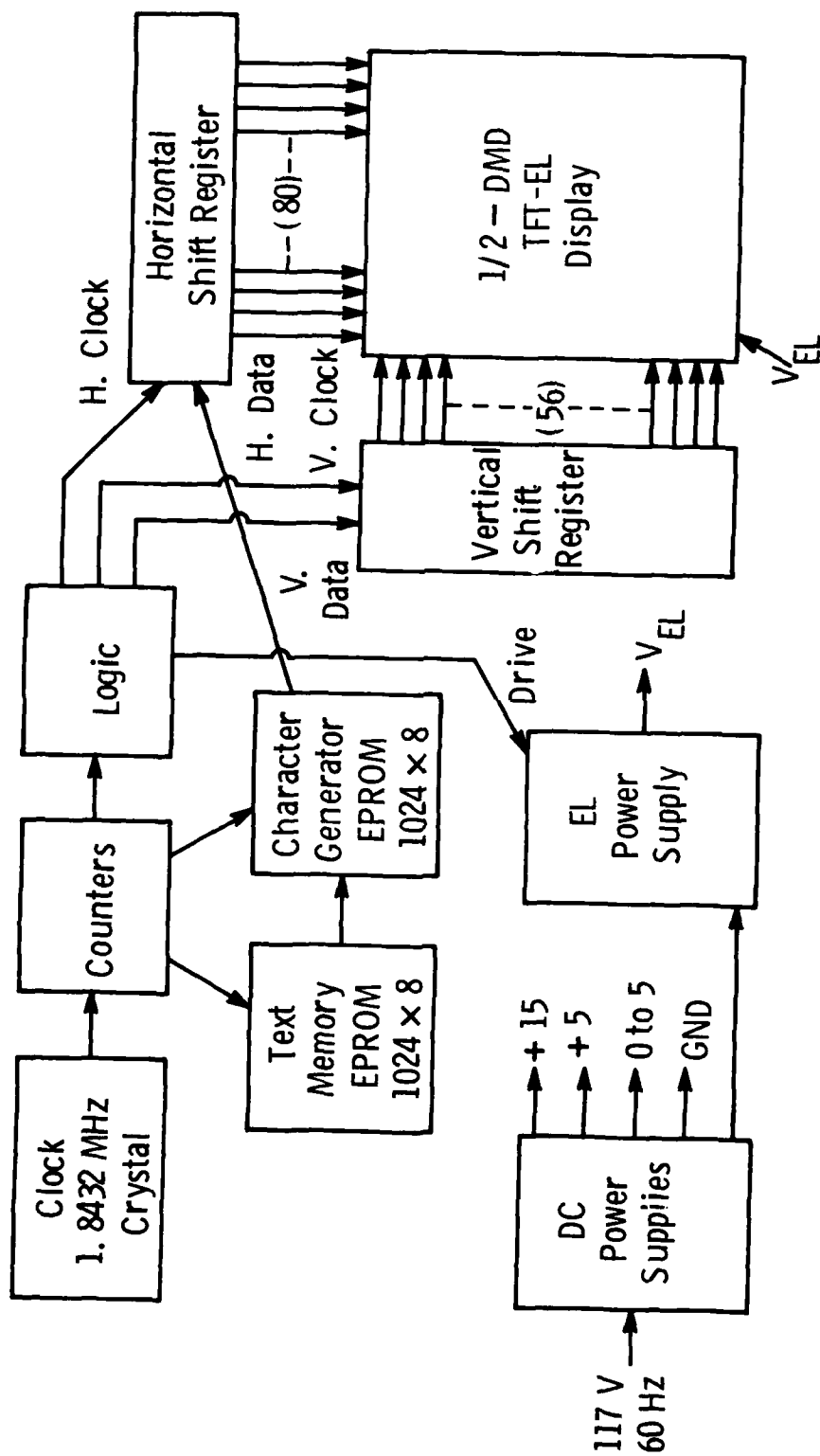


Fig. 9.26 -- New DMD exerciser -- block diagram

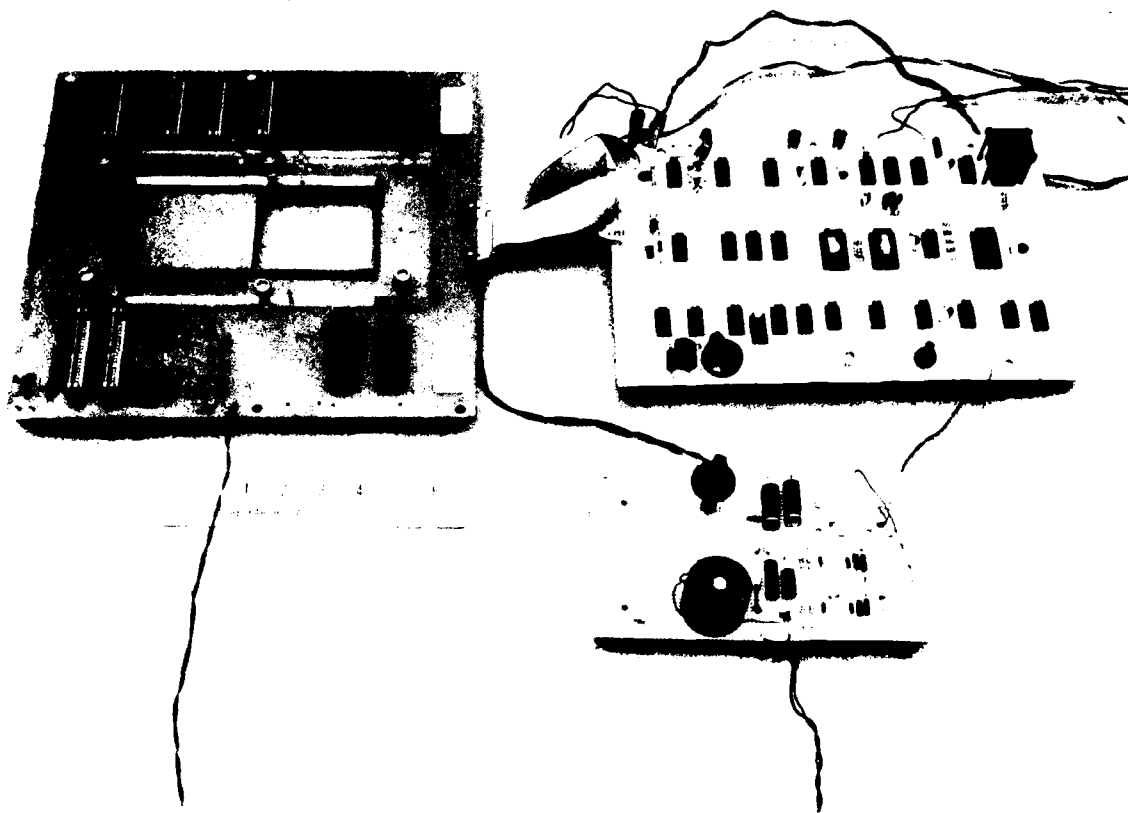


Figure 9.27 New DMD Exerciser, Breadboard Model

operation can be achieved it is possible to estimate what are the achievable power requirements for a DMD type 256 character display with optimal design. Such an estimate is given in Table 9.7 along with the characteristics of the former exerciser as used with the DMD display and the breadboard model as used with a half DMD display. The principal power component is the phosphor excitation power supply. The estimate for a future design assumes a thin film EL phosphor efficiency of 1 lumen per watt and a power supply efficiency of 70%. It is possible that the figures presented may be improved on still further in the case of a dimmed display through the use of very low EL excitation frequencies, which should be feasible using new TFT-TFEL display panel architectures.

A summary of the principal factors that must be addressed in designing a TFT-EL display system for maximum efficiency is given in Table 9.8. These factors have been referred to and discussed earlier except for the TFT scanners (Item 6). Dynamic operation of TFT logic circuits of the multi-phase, non-ratio type results in the maximum efficiency for a given frequency of operation, voltage swing and load capacitance. The  $V_{el}$ -logic circuit isolation referred to in line 5 of the table has been obtained thus far principally by the electronic means discussed in this section. When a digital display similar to the DMD is designed using TFEL phosphor however, a revision of the display architecture will naturally occur and may well lead to an electrostatic shield between the phosphor and the TFT circuitry, thereby affording optimum isolation of these two principal display components.

TABLE 9.7

## DMD Display System Characteristics

Characteristics	Former Exerciser	New Exerciser (breadboard)	Future Design
Frame rate	60 Hz	5 Hz	2 Hz
El excitation			
voltage, P-P	240 V	180V	180V
frequency	8 kHz	5kHz	500 Hz
waveform	square	sine pulse	sine-square
El phosphor type	powder, sprayed	powder, brushed	thin film
El brightness	20 fL	20 fL	40 fL
Video signal swing	25 V	10 V	5 V
Gate signal swing	60 V	15 V	10 V
DC power budget			
EL, bright	20 W	6.8 W	1.5 W*
dim	10 W	3.0 W	0.2 W
Scanners	5 W	1.0 W	0.1 W
Timing, logic, memory	4 W	1.4 W	0.1 W
Total, from			
batteries - bright	29 W	9.2 W	1.7 W
dim	19 W	5.4 W	0.4 W

\*Assumes 1.0 L/W phosphor efficiency,  
50% EL power supply efficiency

TABLE 9.8

Principal Requirements of TFT-EL Display Design for High Efficiency

1. Resonant drive,  $V_{EL}$  supply
2. Duty cycle modulation of EL
3. Low EL frequency
4. Short, high conductance leads and bus bars
5. Isolation of  $V_{EL}$  and logic circuit
6. Dynamic operation of TFT scanners
7. CMOS control logic



## 10. TESTS OF COMPLETED PANELS

The original test specifications of the MM&T Contract are given in Document SCS-501, Technical Requirements, Section 3 - Requirements, and Section 4 - Quality Assurance Provisions, which are as follows:

### 3. REQUIREMENTS

3.1 Display Size. The display shall consist of two 3.40"  $\pm$  .05" x 3.55"  $\pm$  .05" glass substrates containing the display elements, butted together and adhered to an approximate 2.90" x 6.60" glass cover sheet sized to overlap the display area. The display area on each substrate shall be a rectangle, 2.90"  $\pm$  .05" by 3.30"  $\pm$  .03" situated in such a manner that there shall be a minimum 0.25" border around a 2.90"  $\pm$  .05" by 6.60"  $\pm$  .06" actual display area when the two substrates are butted together. (See Fig. 1). An optional backing sheet is permissible.

3.2 Display Format. The display shall contain 77 by 222 display elements. Each element shall be a rectangle, with the rectangles uniformly distributed in each dimension. The dimensions of each rectangular light emitting element shall be a minimum of .015" by .021". This results in the capability for 256 alphanumeric characters with a 5 by 7 dot configuration. The boundary between substrates shall not disturb this format.

3.3 Alphanumeric Characters. Each of the 256 5 by 7 dot configurations shall be capable of displaying a full set of 128 ASCH characters.

3.4 Weight. Display weight shall be a maximum of 5 oz.

### 3.5 Operational Characteristics.

3.5.1 Electrical Input. Signal and power input shall be accomplished by means of evaporated electrodes on the left and right sides and top or bottom of the display.

3.5.2 Display Recognition. Display characters shall be viewable and recognizable in an ambient light intensity of 2000 foot candle (fc) impinging upon the display. In normal room lighting (50 fc impinging upon the display) the display contrast ratio, defined as the ratio of the luminance of an "on" light emitting element in darkness, to the luminance of a neighboring "off" element or neighboring dark space (whichever is greater) should be 20 as a minimum. This shall be measured in accordance with the provisions of Paragraph 4.5.2.

3.5.3 Power Dissipation. At the luminances set to satisfy 3.5.2 with all resolution elements "on", power dissipation in the display panel shall not exceed 2.0 watts. With full power supplied to the panel, and all elements "off", power dissipation shall not exceed 1.0 watts. Thus with all 256 characters "on" total power dissipation in the display will be less than 1.5 watt. This shall be measured in accordance with the provisions of Paragraph 4.5.3.

3.5.4 Electrical Drive. The side and bottom electrodes represent x-y addressing of any of the 77 by 222 or 17,094 resolution elements. Each resolution element shall contain two thin film transistors and one storage capacitor to provide the x-y function, to provide the electroluminescent drive, and to provide short term storage. The display shall be capable of presenting all 256 characters at a repetition rate as low as 30 frames per second.

3.6 Operation Temperature. The display shall be capable of operation over an ambient temperature range of  $-45^{\circ}\text{C}$  to  $72^{\circ}\text{C}$  without degradation of operational characteristics of 3.5 (See 4.5.4).

3.7 Operating Humidity. The display shall be capable of operation at a relative humidity of up to 95% without degradation of operational characteristics of 3.5 (See 4.5.5).

3.8 Operating Altitude. The display shall be capable of operation at an altitude of 30,000 feet and storage at an altitude of 50,000 feet without degradation of operational characteristics of 3.5 (See 4.5.6).

3.9 Shock. The display shall withstand shock when tested in accordance with Paragraph 4.5.7. The display shall not chip, crack or shatter as a result of the drops.

3.10 Vibration. The display shall withstand vibration when tested in accordance with Paragraph 4.5.8. The display shall be free of vibrational resonance below 55 Hz.

3.11 Life Test. Display shall meet all requirements of 3.5.2 after 600 hours life test as described in 4.5.9.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection. The contractor is responsible for the performance of all inspections specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. Inspection records of the examinations and tests shall be kept complete and available to the government as specified in the contract. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.2 Classification of Inspection. Inspection shall be classified as follows:

- (a) First article inspection (does not include preparation for delivery) (See 4.3).
- (b) Quality conformance inspection. (See 4.4).

4.3 First Article inspection. First article testing shall be as follows:

- (a) Two displays shall be subjected to the tests of 4.5.1, 4.5.2 and 4.5.3.
- (b) One of these displays shall be subjected to the tests of 4.5.4 thru 4.5.8.
- (c) Both displays shall then be subjected to the life test of 4.5.9.

4.3.1 Failures. No failures are allowed in first article displays.

4.4. Quality conformance inspection. This inspection shall be performed on 8 displays selected from the pilot production.

4.4.1 Group A inspection. Group A inspection shall consist of the tests of 4.5.1, 4.5.2 and 4.5.3. All eight displays shall be subjected to Group A inspection. No failures are allowed.

4.4.2 Group B inspection. 3 of the 8 samples which have been subjected to Group A inspection shall undergo life test in accordance with 4.5.9. One each of the remaining 5 samples shall be subjected to Temperature (4.5.4), Humidity (4.5.5), Altitude (4.5.6), Shock (4.5.7) and Vibration (4.5.8). No failures are allowed.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in 4.5.1 thru 4.5.9.

4.5.1 Visual and mechanical inspection. Displays shall be inspected for conformance with Paragraphs 3.1, 3.2, 3.3 3.4 and 3.5.4.

4.5.2 Display viewability.

4.5.2.1 Display characters shall be inspected for recognition in an ambient light intensity of 2000 foot candles (fc) impinging on the display. All of the 256 available 5 x 7 dot

configurations shall be checked for at least 2 of the set of 128 ASCH characters so that all characters are viewed and all dot configurations are checked. (See 3.5.2). Recognition shall be measured by presenting the ASCH characters on the display to 6 objective subjects, with no vision deficiencies. The characters shall be displayed in a random manner and a score of correct readings made. A maximum error rate of 3% is acceptable.

4.5.2.2 One of the 256, 5 x 7 dot configurations shall be checked for all ASCH characters. (See 3.5.2).

4.5.2.3 In normal room lighting, 50 fc impingent upon the display, the display contrast ratio (defined as ratio of luminance of an "on" light emitting element in total darkness to luminance of neighboring "off" element) shall be inspected at 9 positions equally spaced in the display. (See 3.5.2)

4.5.3 Power Dissipation test. With all elements of the display turned on to satisfy 3.5.2 requirements, total power dissipated by the display shall be measured. With all elements off, and full power supplied to the display, power dissipation shall be measured. (See 3.5.3).

4.5.4 Operating Temperature. Displays will be placed in a chamber and the temperature lowered to  $-45^{\circ}\text{C}$ ,  $+0^{\circ}$ ,  $-5^{\circ}\text{C}$ . After temperature equilibrium is reached, the displays will be operated and power dissipation shall be measured in accordance with 4.5.3. Following this, the displays will be returned to  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$  and allowed to reach temperature equilibrium after which the test of 4.5.2 will be run. The displays will then be brought to  $72^{\circ}\text{C} +5^{\circ}$ ,  $-0^{\circ}\text{C}$  and allowed to reach equilibrium after which power dissipation will be measured in accordance with 4.5.3. Following this measurement, the displays will be returned to  $25^{\circ} \pm 3^{\circ}\text{C}$  and allowed to reach equilibrium after which they shall be subjected to the tests of 4.5.2. Power shall be off during change from one temperature to another. (See 3.6).

4.5.5 Humidity. Displays shall be maintained at  $40^{\circ}\text{C} \pm 2^{\circ}\text{C}$  and a relative humidity of 90-95% for 96 hours. While still in the chamber power dissipation will be measured after which displays will be removed and tested in accordance with 4.5.2. (See 3.7).

4.5.6 Altitude. Displays shall be brought to a pressure equivalent to 30,000 feet and maintained for 5 minutes after which the power dissipation shall be measured in accordance with 4.5.3. Following this, the displays shall be turned off and the pressure lowered to simulate an altitude of 50,000 feet. The displays shall be maintained at this pressure for 5 minutes and then lowered to room ambient conditions at which pressure the displays shall be subjected to the tests of 4.5.2 (See 3.8).

4.5.7 Shock. The displays shall be subjected to the test of Method 516.2, procedure V of MIL-STD-8103. (See 3.9).

4.5.8 Vibration. The displays shall be subjected to the test of Method 514.1 procedure XI of MIL-STD-S10B. (See 3.10).

4.5.9 Steady state life. Displays shall be operated in an ambient of  $77^{\circ}\text{C} + 5^{\circ}\text{C} - 0^{\circ}\text{C}$  for 600 hours. The displays will be cycled by turning all elements "on" for 50 minutes of each hour and "off" for 10 minutes of each hour. Power dissipation shall be measured at least once each day. After the 600 hours has elapsed, displays will be tested in accordance with 4.5.2. (See 3.11).

In November 1978, amendments to the contract were discussed and later submitted and approved to permit optimal final results to be obtained from an attenuated program, in consideration of the Westinghouse decision to terminate its display R&D effort. These modifications had the effect of focussing the remaining effort on improvements in the manufacturing method, and as a consequence of minimizing comprehensive testing of the display samples.

These amendments included the following:

2. Hardware

Delete: Two confirmatory samples and pilot production run of 20 pcs at 10 pc per month rate.

Add: 5-10 samples tested per Section 3 below - no specified rate.

3. Test Sequence

Delete: Existing test requirements for confirmatory samples and pilot run.

Add:

A. All samples to pass the following: (Asterisks denote changes from current version of SCS-501 attached. Refer to Section 4 below).

4.5.1\* Visual and mechanical inspection

4.5.2\* Display viewability

4.5.3 Power dissipation

4.5.4 Operating temperature

B. Minimum of two samples from above

4.5.2.3 Contrast

4.5.5\* Humidity

4.5.6 Altitude

4.5.7 Shock

4.5.8 Vibration

4.5.9\* Steady state life.

4. Test Specifications

Refer to asterisked items in Section 3 above.

4.5.1\* Display size: Existing product conforms to all geometrical requirements in SCS-501 Item 3.1 except for Cover Glass. Contract specifies 2.90" x 6.60". We are using 3.09" x 6.73" and would prefer to continue to do so.

#### Display Weight

SCS-501 Item 3.4 specifies a maximum weight of 5 oz. Existing product weights 5.6 oz. We would like to go to 8 oz. to provide for louvers and/or other filters as necessary to meet viewability test in 2000 fc.

#### 4.5.2\* Display Viewability

Pending clarification of contract language, we would prefer to relegate item 4.5.2.3 (contrast) to the two samples described in Section 3B above.

#### 4.5.5\* Humidity

Change specification so that power dissipation shall be measured at 40°C after removal from 96 hour, 90% humidity environment.

#### 4.5.9\* Steady State Life

We have previously demonstrated the capability of our phosphor layer and application to meet this requirement subject to the following conditions.

1. Light emission does not exceed 12 fL
2. Samples are not encapsulated
3. Environment is vacuum or dry air

When the development effort of this program was terminated in July, 1979 some 330 1/2 DMD circuits were fabricated in the pilot facility: of these 60 circuits were coated with electroluminescent powdered phosphor and inspected visually; and of these, 16 full DMD panels were made by joining two half panels on a common glass carrier and encapsulating with a top glass and suitable resin. All of the full panels were given visual inspection under operation by the viewability tester, but only preliminary environmental tests were performed and only one complete DMD display was subjected to a full viewability test, although at reduced brightness and ambient illumination levels.



The sections following discuss these various tests in greater detail, including the tests that were made of panels that were ultimately delivered under the contract.

#### 10.1 Visual Inspection.

The customary procedure for making completed panels from 1/2 DMD substrates made in the automated pilot facility includes the steps of examining the substrates visually and electrically, making whatever repairs are possible, especially with respect to bus opens and shorts, and sending the best substrate candidates to the phosphor coating facility. After the phosphor and semi-transparent front electrode have been applied these 1/2 DMD substrates are electrically connected and operated and visually inspected for quality. The best visual samples are then selected on the basis either of electrical matching, i.e. with respect to the required bias voltages or with respect to the brightness of the panels or combination of those. In the period from May 1978 through July 1979 a total of approximately 82 such substrates were coated with phosphor and evaluated. These are listed in Table 10.1 along with the percentage of recognizable characters seen initially in these panels under low voltage operating conditions prior to encapsulation. The substrate number consists of three digits indicating the serial day of the year on which the run was completed, i.e., Jan 1 being represented by the number 001 and December 31 by 365. The decimal fraction is simply the number of the substrate in the particular run. The performance of these substrates is presented in another fashion in Figure 10.1 as a scatter plot wherein it may quickly be seen that relatively few panels were obtained with readability equal to or exceeding 90%. The interruption in panel production following day 291 related to program reorganization and the new direction taken at that time. A new mask set for which design was initiated at that time was installed at day 94 in 1979; although there was time for relatively few runs following that date, it is evident that the experience curve was rapidly approaching the experience level gained in 1978, and if continued would rapidly have far exceeded it due to the superior nature of the mask set and the much fewer fabrication steps and shorter time

required per substrate. Viewability data in Table 10.1 and Figure 10.1 do not necessarily portray optimum panel operation, since they were obtained with the older exerciser discussed in Section 9.2, which drives all eight rows of characters in parallel so that a defect in any one row tends to be repeated in the other rows. A single defect may thus appear as eight defects, in which case the resultant viewability would be degraded from that obtainable in normal operation of the panel. Further, it should be noted that in most cases the substrates have been repaired after initial electrical tests to minimize bus bar opens and shorts, and also after phosphor coating to reduce the number of permanently lit elements or newly appearing bus defects.

From the better substrates with phosphor applied, full DMD displays were assembled on a single glass base and sealed with a suitable resin and top glass cover plate as discussed in Section 8. These panels used the substrates listed in Table 10.1, the only exception being the two engineering samples prepared in 1977. Twenty-five encapsulated panels prepared from 1/2-panels are shown in Table 10.2 along with the designations of the individual substrates from which they were assembled, readability information before and after packaging as available, known dates of assembly, and other comments. Readability of many of these panels was appreciably degraded from that of the individual substrates during the packaging and thereafter. Physical handling involved in the packaging process is partly responsible for this degradation, as well as occasional misalignment, making it more difficult to make good connections to the combined pairs. Figure 10.2 illustrates these effects as exhibited by panel #26, in which the viewability dropped from 96% average to about 78%. The picture of the completed panel includes an example of element defects repeated in vertical columns because of the exerciser's common connection of the character rows, as described earlier. The horizontal lines of faults may be due to a faulty connection in one or more of the horizontal bus bars. Two outstanding panels can be seen in Table 10.2, namely engineering sample #2 prepared in 1977 and panel #19 completed in September, 1978. Although character readability was nearly perfect in panel #19, there was appreciable

Table 10.1 Initial Viewability.  
1\2-DMD Substrates with Phosphor

Substrate Number	Viewability (percent recogniz- able char- acters)	Substrate Number	Viewability (percent recogniz- able char- acters)
1978		1978	
128.2	25	216.2	66
131.6	40	219.3	70
138.1	94	219.4	81
138.2	50	226.5	0
144.2	92	227.2	70
144.4	92	227.3	2
145.6	50	228.8	75
150.1	34	234.2	60
150.2	75	235.5	92
153.1	50	240.2	90
153.2	90	241.3	0
164.1	70	244.1	75
165.2	75	248.3	57
165.4	40	248.6	70
166.5	30	261.4	94
166.8	90	265.1	94
170.4	90	268.5	27
171.6	90	269.4	95
173.2	60	270.2	0
173.3	70	276.2	16
198.1	92	277.3	0
198.2	75	289.2	100
199.4	70	290.3	19
199.5	80	290.5	98
202.1	60	291.6	94
205.2	92	301.8	41
205.4	100	342.3	3
209.2	40		
209.3	80		
212.6	100		
1979		1979	
010.6	4	151.1	45
033.2	0	151.3	37
036.5	5	151.4	90
044.2	14	151.5	70
072.2	3	156.2	60
073.3	9	156.4	26
079.1	0	156.5	90
079.2	27	159.3	85
094.3	80	159.4	55
100.8	0	159.6	90
124.2	39	169.5	16
124.6	0	169.7	25
131.4	37		

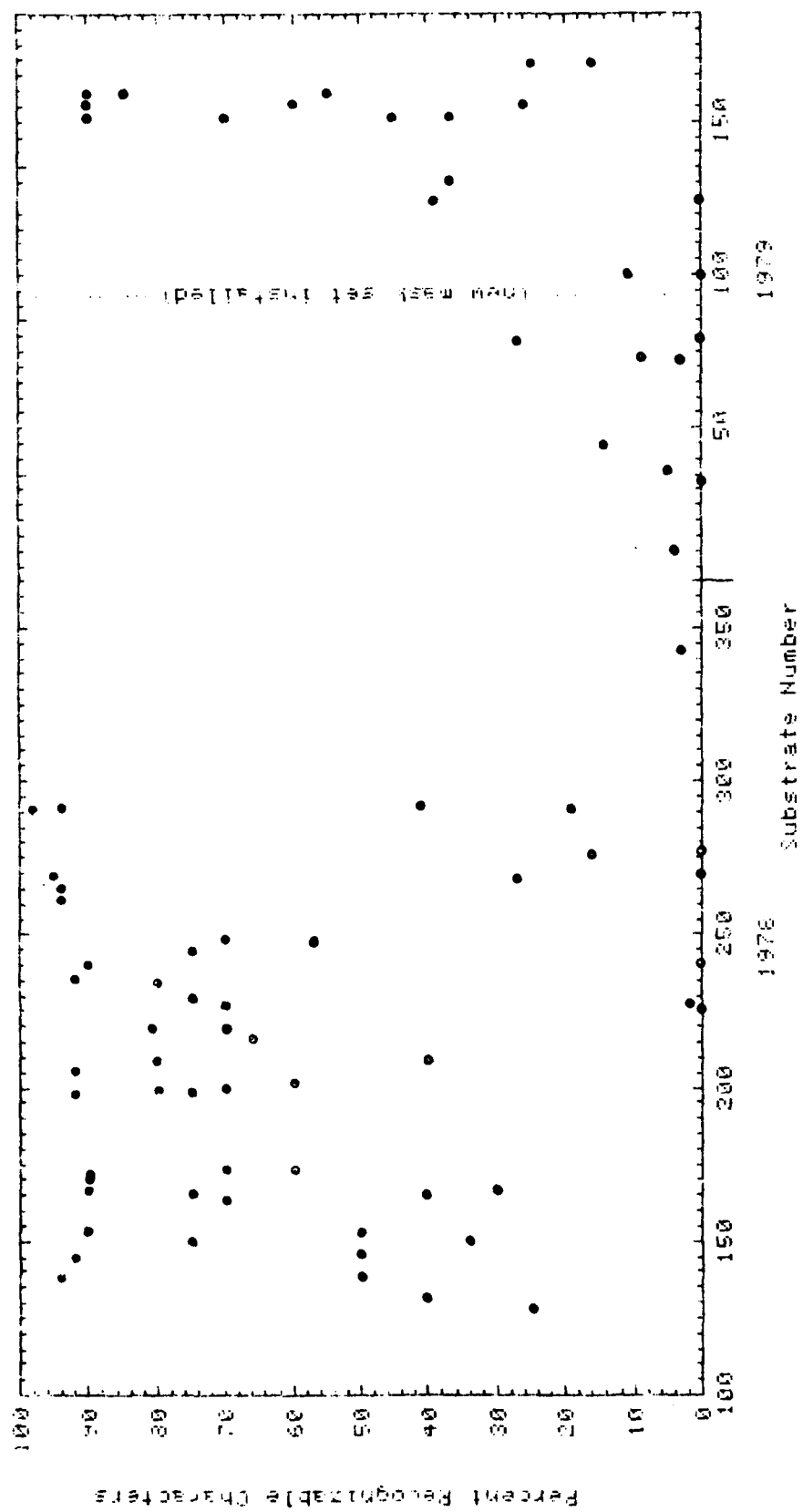
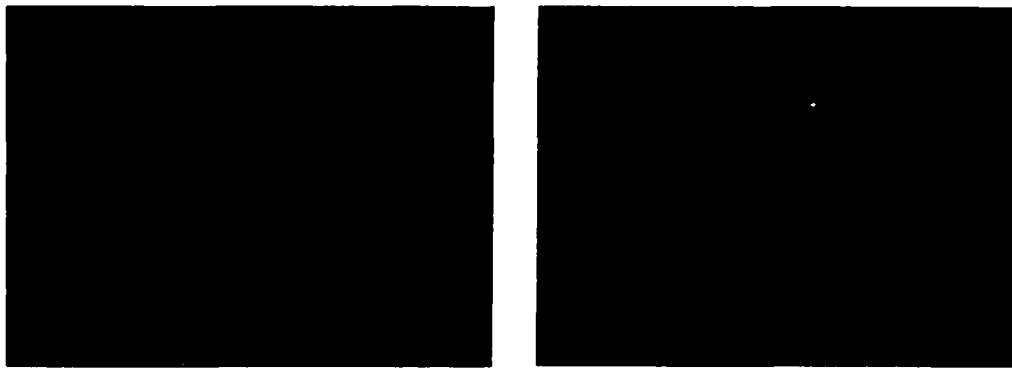


Figure 10.1

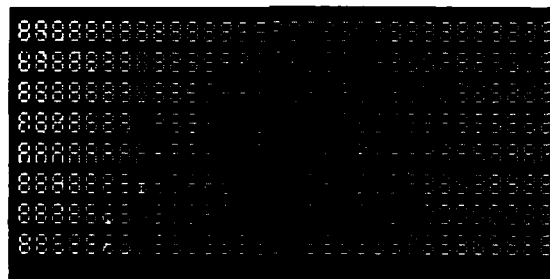
Table 1-2 Packaged PMO Panels

Panel No.	Left	Right	Shipped Date	Readability Before Recd (Avg, L&R)	Readability After Recd	Comments
Eng 1	7282-2	7282-3			98%	Report 11-17-77
Eng 2	7284-2	7282-3			100%	Report 11/17/77
7	8142-2	8144-4				
8	8141-2	8144-4	5-02-78	92%		
9	8153-1	8153-2	6-27-78	70%		Collapsed
10	8165-2	8164-1	6-30-78	77%	<5%	
11	8159-2	8145-6	6-30-78	42%		R. collapsed
12	8171-6	8170-4	7-12-78	90%		R. collapsed, L. open and
13	8173-2	8173-3	7-14-78	65%	60%-L	R. collapsed
14	8165-4	8166-5		35%		
15	8166-8	8198-1		91%		
16	8209-2	8219-3	8-26-78	55%		Krylon A CAB, Stucast
17	8216-6			100%-L		For alt. hum. temp. tests
18	8209-3	8235-5		86%		For enviro. tests
19	8234-2	8240-2		100%	106%	L & R. unequal brightness
20	8265-2	(olans)				For connector tests
24	8291-6	8290-5	6-27-79	95%		Cracked/packaging
25	8261-4	8269-4	6-29-79	94%	90%	
26*	8205-4	8235-4	6-29-79	96%	78%	
27**	9169-7	9159-3		55%	6%	Labeled No. 1
28**	9151-5	9156-2		65%	29%	Labeled No. 2
29**	9156-5	9159-4		72%	12%	Labeled No. 3
30**	8248-6	8216-2		68%	36%	Labeled No. 4
31**	9151-4	9159-6		90%	54%	Labeled No. 5
32**	8228-8	8219-4	5-31-79	78%	70%	Labeled No. 6

\* Panels shipped to ERADCOM  
 \* Pairs selected for brightness match



(a) Before



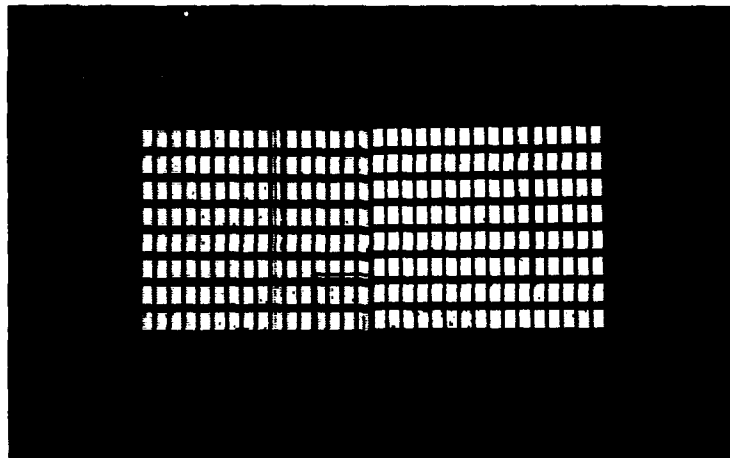
(b) After (Panel No. 26)

Figure 10.2. Viewability of DMD substrates before and after encapsulation.

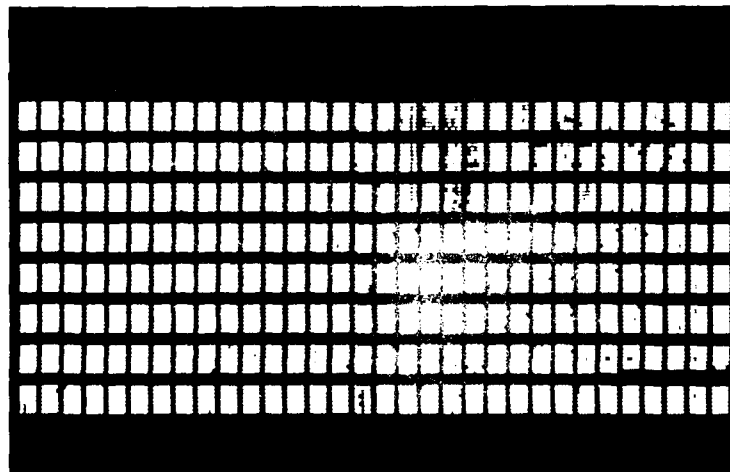
inequality in brightness levels for the left and right halves, giving it an undesirable viewing quality. Joining of substrates having similar electrical bias level requirements has been more or less essential with the old type exercisers because of a very narrow band of suitable levels. This is because of electrical interference effects from the high voltage AC appearing on the phosphor electrode, discussed in Section 9.5. When matching is performed in this fashion, the brightness inequalities between the two members often result. However, if a concerted effort is made to match substrates according to their brightness at a given excitation voltage, only possible if sufficient number of operating substrates of reasonable quality are available (which was the case near the end of the program), then considerable improvement in appearance with respect to brightness can be obtained. Figure 10.3 is an example of the appearance of two substrates selected for having similar bias setting requirements, shown in (a), and for having similar brightnesses, shown in (b). Substrate #9151-5 is common to both of these assemblies, but only the combination in (b) was packaged.

It is difficult to make a perfect match in physical appearance of these panels as well as in brightness because the color of the operating substrates as seen in room light varies from blue through green to a tannish color, depending on the method of phosphor application, the thicknesses involved, the type of Riston film used, and the nature of the semi-transparent front electrode. These are quite independent of the color of light emitted, which tends to be quite uniform in its green to bluish-green hue. The various packaged DMD panels are inspected not only for their readability or viewability but also for the number of permanently ON and permanently OFF defects by lighting the panels with all elements OFF or all elements ON, respectively. Figure 10.4 shows panel #6 in these two conditions plus the condition where all eights are written, the latter showing defects in the character spaces. The number of recognizable eights in this panel is 178 for a readability of 70%.

The best panels that could be assembled from approximately sixteen best quality substrates at the end of the program were finished



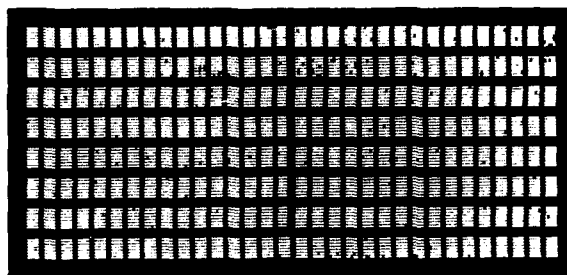
(a) For similar bias setting



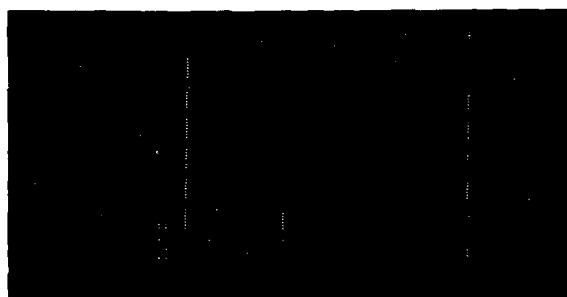
(b) For similar brightnesses

Figure 10.3. Substrate matching by bias settings or brightness.

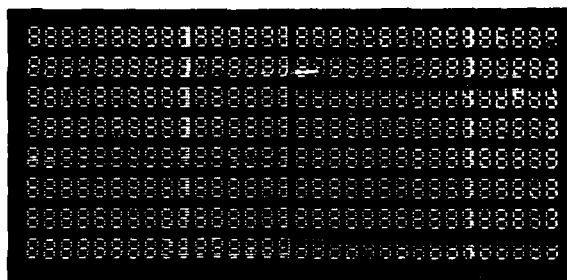




(a) All elements ON, showing OFF defects



(b) All elements OFF, showing ON defects



(c) All 8's, showing character defects

Figure 10.4 Packaged DMD appearance.  
(Panel No. 6, brightnesses matched)

from pairs selected on the basis of equal brightness. Six such panels were made and labeled 1 through 6. Number 1 panel was defective after packaging; the remaining five along with panels 19, 25 and 26 were selected for shipment to ERADCOM. Photographs of these panels as well as the two engineering samples delivered in 1977 are shown in Figures 10.5.1 through 10.5.5. The engineering samples are shown written with a series of numerals, whereas the other panels are shown with all 8's written. Panel #3 in Figure 10.5.3(c) has 1/2 of the display not operating. The cause is not known but may be due either to a blown ground bus or a bad connection in the viewing mount. Attempts to restore operation of this half were not successful, but the effort was not exhaustive.

From the total experience in making and testing packaged full DMD panels, it has become clear that care must be taken in the type of electronic circuitry used to operate these panels. In particular, the collapse of TFT's in several finished panels was caused by voltage transients in the driving circuitry. In addition, close adjustment of bias levels is required for good panel appearance using the older circuit designs. It is also obvious that the packaging technique itself is a source of panel deterioration. The forces and pressures involved in applying the RISTON photoresist film can be a source for circuit degradation, as well as the considerable handling involved in the process. Further improvements in this area are desirable.

## 10.2 Environmental Tests

### Requirements

Environmental requirements under the present program were given at the beginning of Section 10. A brief summary of them is as follows:

### Panel Drive — Environmental Tests

Life (@ 72°C), all gates and sources connected in parallel, gates pulsed during OFF and ON states (50 min. ON, 10 min. OFF), power dissipation measured once per day.

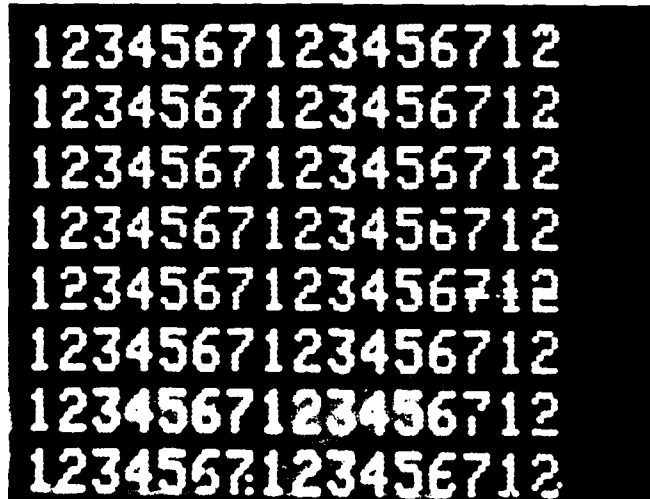
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SAMPLE #1, SIDE A, CHARACTERS ON

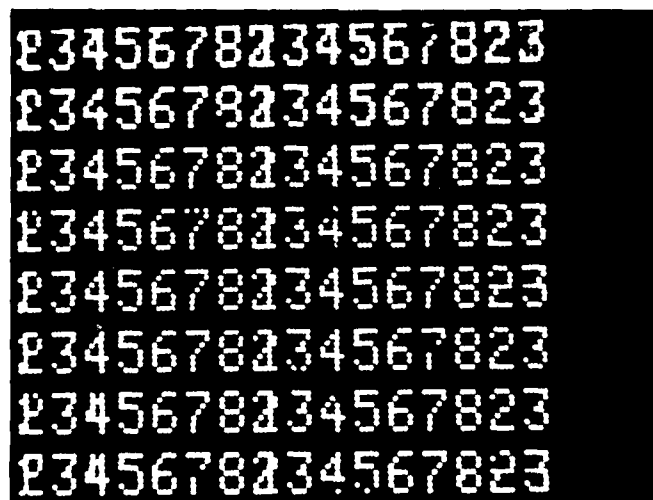
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SAMPLE #1, SIDE B, CHARACTERS ON

Figure 10.5.1. Viewability of packaged and delivered DMD panels.

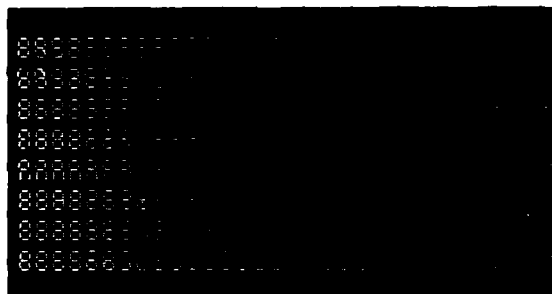


SAMPLE #2, SIDE A, CHARACTERS ON

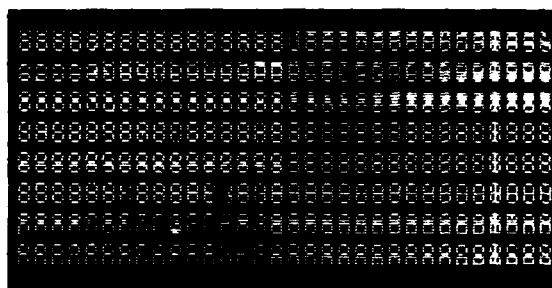


SAMPLE #2, SIDE B, CHARACTERS ON

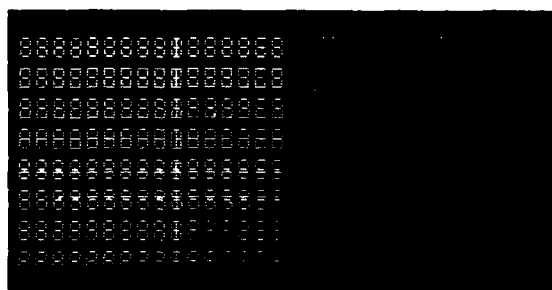
Figure 10.5.2. Viewability of packaged and delivered DMD panels.



(a) #26

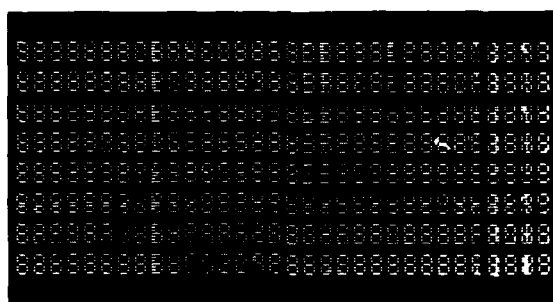


(b) #28 (No. 2, Br. Match)

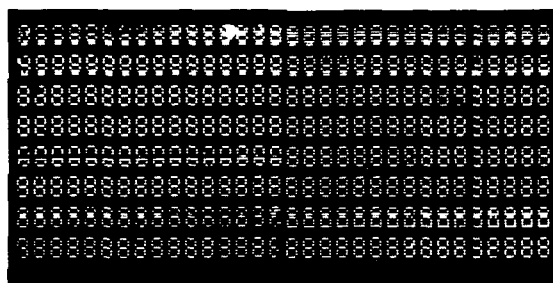


(c) #29 (No. 3, Br. Match)

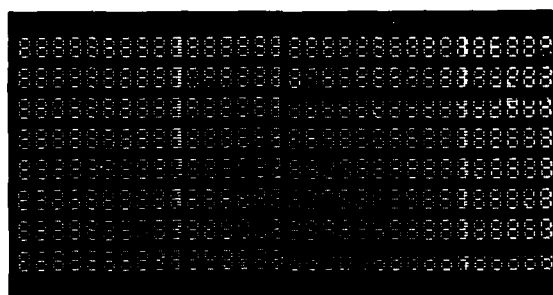
Figure 10.5.3. Viewability of packaged and delivered DMD panels.



(a) #30 (No. 4, br. match)

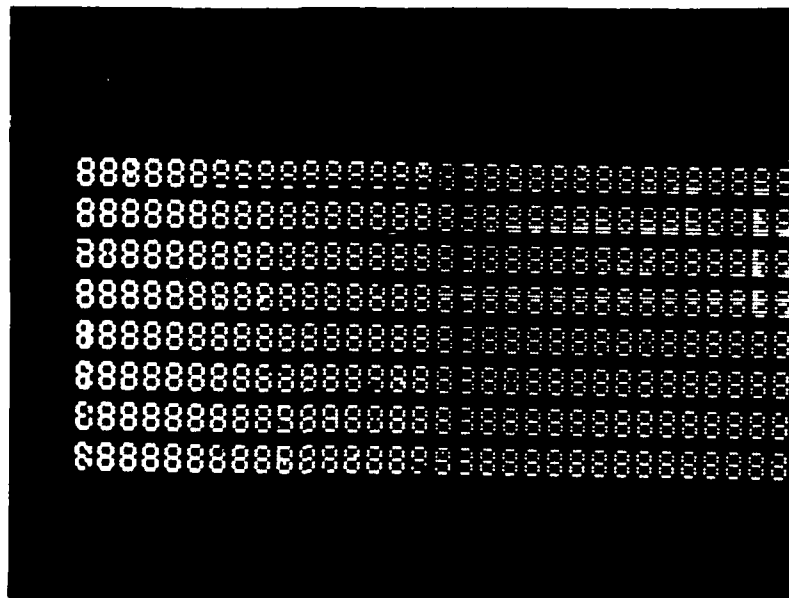


(b) #31 (No. 5, br. match)

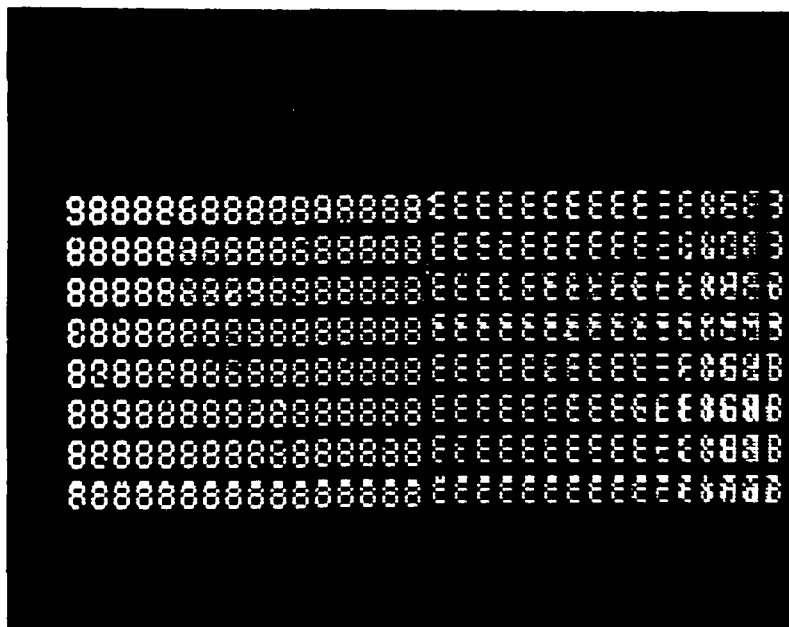


(c) #32 (No. 6, br. match)

Figure 10.5.4. Viewability of packaged and delivered DMD panels.



(a) No. 19



(b) No. 25

Figure 10.5.5 Viewability of packaged and delivered DMD panels.

Temp (-45 to 72°C), measure power dissipation (ON-OFF), same drive conditions as above (3 different temperatures).  
Humidity (40°C, 90-95%, 96 hours), measure power dissipation (ON-OFF), same drive conditions as above (after 96 hours).  
Altitude (30,000 feet, 5 minutes 50,000 feet, 5 minutes) measure power dissipation (ON-OFF) after 5 minutes at each altitude, same drive conditions as above.  
Shock/Vibration (no chips or cracks, no resonances less than 55 Hz) visual inspection, no drive conditions specified.

A detailed plan for conducting these tests including the assembly and preparation of appropriate apparatus, developing a simple ON-OFF exerciser to operate the panels under the various test conditions and of conducting the tests was developed. This plan is shown in Figure 10.6. The first fourteen weeks of the program involved the identification and setup of environmental test equipment, design and fabrication of drive electronics and connectors, and preliminary environmental tests. Packaging of confirmation test panels was planned for weeks 9 through 16 with the first 72°C life tests scheduled to start in week 13. The ON-OFF exerciser, which operated the panels under test over the same duty cycle as they would experience in actual operation but with all elements either turned ON or OFF, is described in Section 9.2.

#### Preliminary Results

A facility was set up with three life test ovens, two temperature chambers (-45°C + 72°C) and a humidity chamber. An X-Y panel was exposed to 95% relative humidity at 45°C for twelve days. Periodic testing showed that a row of characters closest to a sealed edge were becoming dimmer. This indicated a potential hermetic seal problem. Consequently, a major effort was undertaken to improve sealing and packaging (see Section 8).

Life testing of packaged panels at 72°C required the ON-OFF exerciser and fixturing. The fixture connected all gate and source pads on a panel to common external leads so that only four leads were required



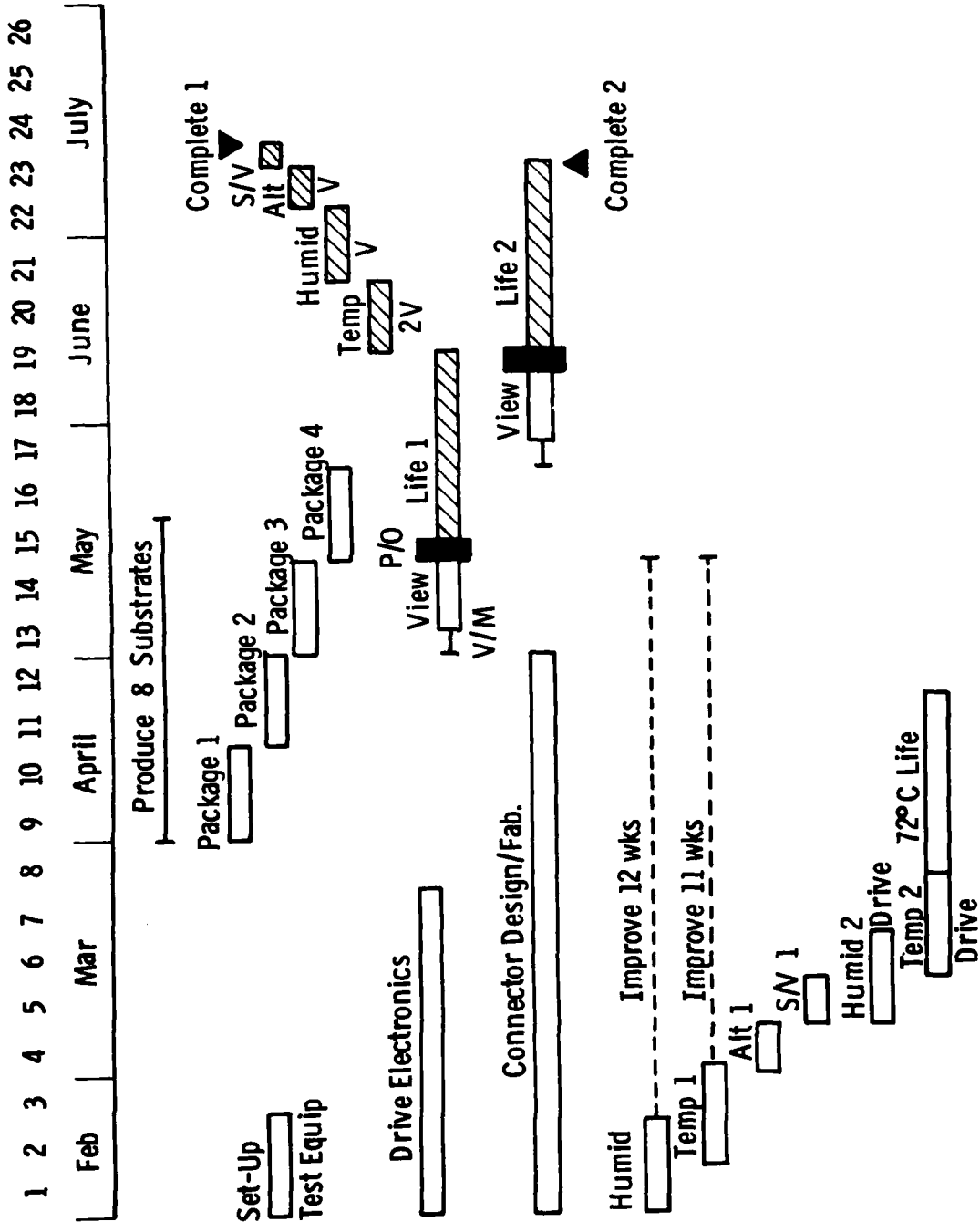


Fig. 10.6 -- Environmental test schedule for preliminary and final testing of confirmatory samples in 1978

to exercise a panel in a test chamber located at some distance away from the exerciser. This equipment was used to life test panel #8 at 72°C. The panel was electrically driven by the exerciser with the phosphor voltage set at 150 volts peak to peak. The average starting brightness of the phosphor elements was 10 fL. After four hours at 72°C the average brightness decreased to only 10% of the original level, or 1 fL. In the ON state the panel elements were barely visible in normal room lighting. The results of this test gave rise to an intensive program in phosphor application and panel encapsulation methods, as discussed in Sections 7 and 8 above.

A preliminary altitude test was run without power on one of the early panels. No problem areas were indicated. A series of altitude tests were conducted on panel #18 with power using the ON-OFF exerciser. The panel performed satisfactorily. Figure 10.7 shows the initial appearance on the panel with all elements OFF and ON, at the beginning of the test and after exposure to a low pressure environment corresponding to a 30,000 feet altitude and 50,000 feet altitude. No degradation was noted, as shown by the figure.

A shock and vibration test (MIL-STD-883C) was performed on a DMD panel mounted on a printed circuit board with film tape. No damage was evident at the conclusion of the test. The following is quoted from the test report:

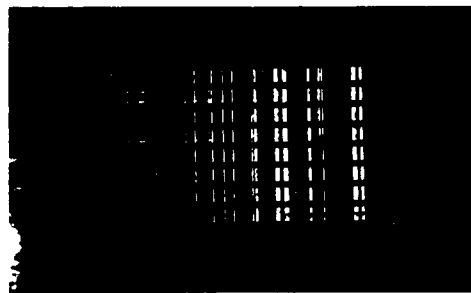
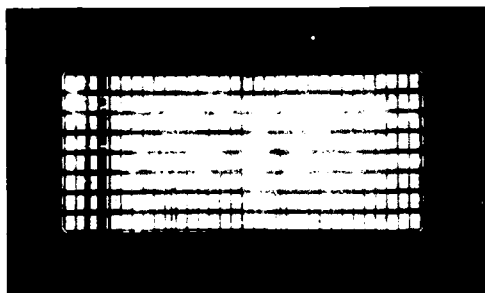
#### Vibration Test of Dummy DMD Display

At the request of T. Czaky of the Programmable Automation group, vibration and shock tests were performed on a three-inch by seven-inch DMD display. No damage was evident at the conclusion of the tests.

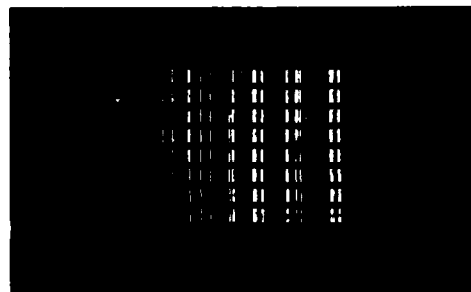
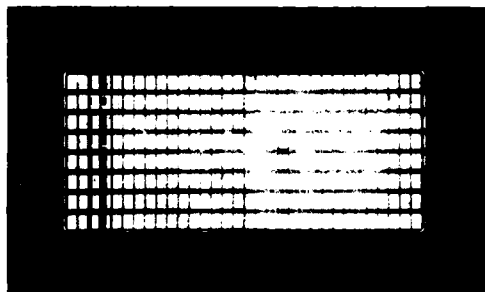
The vibration test specified was Method 514, Procedure IX of Mil Std 883C. According to Mil Std 883C this test is intended to simulate the vibration environment of loose cargo. The test is normally performed on equipment which is prepared for shipping. Thus, the test specified is inappropriate for the display which is an

Elements Off

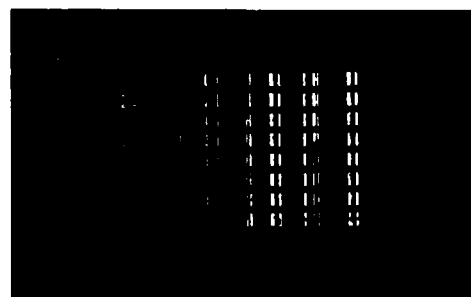
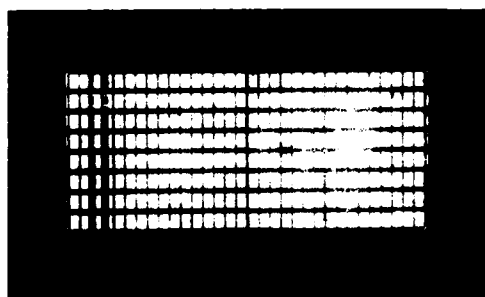
Elements On



(a) Initial



(b) After 30,000 ft. equivalent



(c) After 50,000 ft. equivalent

Figure 10.7. DMD panel, No. 18, subjected to altitude test.

electronic component. To subject this component to the test without the normal protection of both the assembly in which it is installed and the packing case is unreasonable. Only the first part of the procedure, a resonance search, could be applied to a component.

The display, mounted to a printed circuit board with foam tape, was subjected to vibration of 30 mils double amplitude from 10 to 55 Hz. The response was measured and recorded at 1 Hz intervals. This procedure was repeated in the three principal axes of the display. In no case did the response exceed twice the input, meeting the specification requirements.

The shock test specified was Method 516, procedure V of Mil Std 810B. This test is intended to simulate rough bench handling of subassemblies during repair. The test consists of holding the sub-assembly on each edge at a 45° angle and releasing it, letting it drop onto each of the faces. This test was performed as specified except that the display was not dropped directly onto the glass face. Dropping it onto this face was considered unreasonably harsh. No damage was observed as a result of this test.

The dummy display supplied survived the tests to the extent they could reasonably be applied without damage. It is felt, however, that the vibration test, in particular, is inappropriate for the component. A more realistic vibration test should be specified if the integrity of the display is to be verified.

These preliminary environmental tests of DMD panels made under the program were quite encouraging although the temperature and humidity tests indicated some problems. A summary of the findings is shown in Table 10.3.

TABLE 10.3  
Summary of Preliminary Environmental Tests

- Humidity  
40°C, 90-95% RH  
loss to brightness along row of characters closest to seal edge
- Temperature  
45°C to 72°C  
phosphor life greatly reduced
- Altitude  
30,000 and 50,000 feet  
no visible problems
- Shock/Vibration (MIL-STD 810B)  
panel attached to multi-layer PC board  
no failures indicated (chips, cracks or resonances)
- Conclusion  
humidity test shows potential problem, package redesigned (see Section 8)  
temperature test showed severe problem with phosphor; concentrated effort was given this problem (see section 7)

In view of the decision made in October 1978 to terminate the program after an eight month windup phase, the remaining effort was concentrated on improvements in the details of circuit fabrication; accordingly further environmental testing was suspended, and only the results of the preliminary tests, summarized above, were obtained.

### 10.3 Viewability Testing

The prescribed viewability tests include in brief the following requirements:

- All tests in room ambient temperature. A random set of characters is displayed one at a time in each character position.

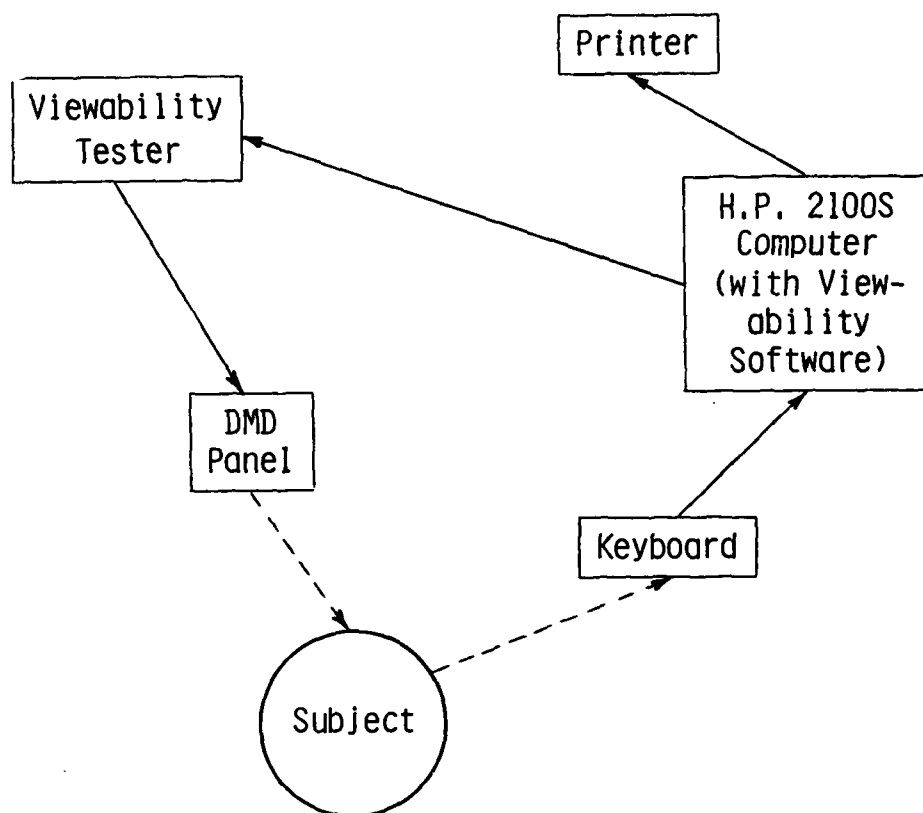


Figure 10.8 — Setup for Viewability Testing

- Six people view the panel, record by typing each character as they recognize it, and this is compared with the input data for correspondence.
- The test was to be performed eight times on two samples.

As the program developed, the only panel available with low defects was #19, referred to earlier in the Section 10.1. This panel was used in the viewability tests that were made. The general setup for this testing is indicated in Figure 10.8. The Hewlett-Packard 2100S computer, used to control the automated pilot fabrication facility, furnished a random alphanumeric character instructions manual together with character positions to the viewability exerciser, which in turn drove the display being tested. A keyboard associated with the Hewlett-Packard 2640B terminal was used by the subject to indicate the character he perceived and this information was entered in the computer. The answer was then compared with the random character displayed and a printout made of the characters chosen by the computer program together with the subject's answer. The number of errors were also tabulated. The results were furnished by a printer in hard copy form. Figure 10.8 shows a typical printout for one of the subjects. The non-correspondence of the computer selections and the subject's response have been circled for convenience in locating them. In this particular case the error rate was 4.679%. Seven different subjects performed this viewability test and the results are summarized in Table 10.4. One of the seven performed the test with room lights on; the others with lights off. The error rate per individual varied from 1.04% for Cresswell to 6.58% for Selchan. one half of display No. 19 is appreciably dimmer than the other half, it was expected that the error rate would be larger on that half (the right half, as mounted in the test). In point of fact, the error rate on the two halves was very nearly the same, being actually a slightly bit lower on the right hand or dim side.

The software written to perform this test automatically using the Hewlett Packard 2100S computer worked extremely well. It represented





an elegant solution to the efficient performance of this rather lengthy character recognition or viewability test, so essential in making an accurate evaluation of the quality or basic usefulness of the DMD display.

TABLE 10.4

Summary of Viewability Test Results, DMD Display No. 19

	<u>%</u>	<u>Errors</u>	<u>Recog.</u>	<u>Typing</u>	<u>Location</u>	
					<u>Bright</u> <u>L</u>	<u>Dim</u> <u>R</u>
Cresswell	1.04%	6	5	1	6	
Burkholder	1.38%	8	7	1	6	2
Kirkwood	2.25%	13	13		8	5
Shaffer	4.67%	27	22	5	12	15
Selchan	6.58%	38	33	5	18	20
Santoro	3.64%	21	20	1	13	8
Burkholder (Room Lights On)	2.94%	17	17		5	12
TOTAL		130			68	62

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# APPENDIX I

OGFIL\*LAMPLOTS(1).PLOTFOR

```

1 C
2 C
3 C
4 C ADDED CALCULATION OF LIFE AT 110 VRMS ON 3-29-79
5 C ADDED PROVISIONS TO GO TO 2100 HOURS 6-05-79
6 C GHGD VRMS TO 120 (340 P2P) 6-05-79
7 C
8 DIMENSION XSC(6),IHDG(12,10),LINE(71),IFXT(50),IFXV(50)
9 C
10 VMAX STORES ALLOWED MAX ORDINATES
11 TMAX STORES ALLOWED MAX ABSCISSAE
12 DIMENSION TMAX(6),VMAX(3),V(50),T(50),IERR(2),TADD(6)
13 DATA VMAX/100.,200.,300./,TADD/1.,2.,5.,10.,20.,20./
14 DATA TMAX/69.,138.,345.,690.,1380.,2080./
15 DATA IERR/6H TIME,6H VOLTS/
16 DATA IS1/1H!/,IS2/1H-/,IS3/1H+/,IS4/1H!/,IS5/1H*/
17 DATA NT/5/,V/55.8,65.2,71.6,88.8,106.1,45*0./
18 DATA T/0.,18.5,24.,48.,72.,45*0./,IHDG/120*1H /
19 C IV IS INDEX OF VMAX & IT OF TMAX FOR TEST SELECTION
20 WRITE (6,60123)
21 IV=1
22 DO 25000 I=1,2
23 60123 FORMAT(1H1)
24 DO 25001 J=1,4
25 K=6*(I-1)+1
26 L=K+5
27 READ (5,50025) (IHDG(M,J),M=K,L)
28 CONTINUE
29 25000 CONTINUE
30 DO 25002 I=5,9
31 READ (5,50026) (IHDG(M,I),M=1,6)
32 CONTINUE
33 25002 DO 25003 I=5,9
34 READ (5,50027) (IHDG(M,I),M=7,12)
35 CONTINUE
36 50025 FORMAT (6A6)
37 50026 FORMAT (9A,6A6)
38 50027 FORMAT (6A6)
39 NT=1
40 READ (5,55555) I
41 55555 FORMAT (A1)
42 DO 26000 I=1,9
43 IF ((I.EQ.5).OR.(I.EQ.10)) WRITE (6,66666)
44 66666 FORMAT ( )
45 WRITE (6,62600) (IHDG(J,I),J=1,12)
46 62600 FORMAT (1H,12A6)
47 26000 CONTINUE
48 20500 CONTINUE
49 READ (5,50000) T(NT),V(NT)
50 50000 FORMAT (7X,2(8X,F8.1))
51 IF (V(NT).LT..001) GO TO 20501
52 NT=NT+1
53 GO TO 20500
54 20501 CONTINUE
55 WRITE (6,66666)
56 NT=NT-1
57 20005 CONTINUE
58 NM2=NT-2
59 RM=IN=10.E20
60 SIGMAX=10.E20
61 DO 20030 IC=1,NM2
62 SIGX=0.
63 SIGY=0.
64 SIGXY=0.
65 SIGXSQ=0.
66 SIGYSQ=0.
67 DO 20040 ISQ=IC,NT
68 N=NT-IC+1
69 SIGX=SIGX+T(ISQ)
70 SIGY=SIGY+V(ISQ)
71 SIGXY=SIGXY+T(ISQ)*V(ISQ)
72 SIGXSQ=SIGXSQ+T(ISQ)**2
73 20040 CONTINUE
74 RM=(SIGX*SIGY-N*SIGXY)/(SIGX**2-N*SIGXSQ)
75 RATE =1./RM
76 PC=(SIGY-RM*SIGX)/FLOAT(N)
77 DO 20371 IJ=IC,NT

```

FORTTRAN coding which generates  
the phosphor plots by operating  
on data files such as .576  
(following)

```

76      SIGYSQ=SIGYSQ+(V(ISQ)-RM*T(ISQ)-RC)**2
77      20371 CONTINUE
78      SIGYSQ=SIGYSQ/(NT-IC+1)
79      C      WRITE (6,60030) IC,RATE,RC,SIGYSQ
80      IF (SIGYSQ.GT.SIGMAX) GO TO 20041
81      ISQEST=IC
82      RMMIN=RATE
83      RCMIN=RC
84      SIGMAX=SIGYSQ
85      20041 CONTINUE
86      60030 FORMAT(6X,5H IC=,I3,6H RATE=,F8.5,5H C=,F8.5,8H SIGYSQ=,E9.4)
87      20030 CONTINUE
88      60050 FORMAT(/9H SINCE ,F5.1,16H HOURS THIS LAMP,
89      & 21H HAS BEEN RUNNING AT ,F4.1,15H HOURS PER VOLT)
90      IT=1
91      DO 20000 I=1,NT
92      20003 CONTINUE
93      C      CHECK EACH INPUT VOLTAGE VS CURRENT VMAX
94      IF (V(I).LE.VMAX(IV)) GO TO 20004
95      IV= IV+1
96      IF (IV.LT.4) GO TO 20003
97      WRITE (6,60070) IERR(2),V(I)
98      STOP
99      20004 CONTINUE
100     C      NOW CHECK INPUT TIME VS CURRENT TMAX
101     20001 CONTINUE
102     IF (T(I).LE.TMAX(IT)) GO TO 20000
103     IT=IT+1
104     IF (IT.LT.7) GO TO 20001
105     WRITE (6,60060) IERR(1),T(I)
106     60060 FORMAT(/13HVALUE FOR ,A6, 4H OF ,F7.2,21HTOO HIGH - FIX INPUT ,
107     C      18HFILE AND RUN AGAIN//)
108     STOP
109     20000 CONTINUE
110     XS =( TMAX(IT)+TADD(IT))/7.
111     YS = VMAX(IV)/5.
112     C      WRITE (6,60001) XS,YS
113     C      Y1 & Y2 ARE VOLTAGE FOR FIT LINE MARKERS
114     C      THESE WILL BE USED WHEN LINE INDEX IS 2 & 70
115     Y1=XS/RMMIN/10. + RCMIN
116     Y2=6.9*XS/RMMIN + RCMIN
117     IY1 =IFIX(Y1*10./YS)+1
118     IY2=IFIX(Y2*10./YS)+1
119     C      WRITE (6,60040) Y1,Y2,IY1,IY2
120     60040 FORMAT (/2F9.3,2I9//)
121     60001 FORMAT (/7H XS=,F6.1,5H YS=,F6.1//)
122     C      DETERMINE OUTPUT MATRIX COORDINATES FROM
123     C      EACH INPUT DATA POINT
124     DO 20010 I=1,NT
125     IFXT(1) =IFIX(T(I)*10./XS)+1
126     IFXV(1)=IFIX(V(I)*10./YS)+1
127     20010 CONTINUE
128     C      START PRINTING FIRST PLOT (NO CURV FIT)
129     LIY2=0
130     IF (IY2.LE.55) GO TO 20705
131     LIY2=1
132     TOPT=(5.5*YS-RCMIN)*RMMIN
133     LIK=IY2-55
134     ITOPT=IFIX(TOPT*10./XS)+1
135     C      DO 20707 I=1,LIK
136     C      DO 20706 J=2,70
137     C      LINE(J)=1H
138     CQ706 CONTINUE
139     C      LINE(1)=1H
140     C      IF (I.EQ.1) LINE(70)=1H+
141     C      IF (I.EQ.1) LINE(1)=1HA
142     C      WRITE (6,60020) (LINE(J),J=1,70)
143     20707 CONTINUE
144     20705 CONTINUE
145     DO 20020 L=1,54
146     IF (L.EQ.2) WRITE (6,62121)
147     62121 FORMAT(2X,7H VOLTS)
148     DO 20013 I=2,70
149     LINE(I)=1H
150     20013 CONTINUE
151     LINE(1)=IS1

```

```

152      C      CHECK TO SEE IF THIS IF REF LINE
153      DO 20011 J=1,5
154      IF (L.NE.((J-1)*10+5)) GO TO 20011
155      LINE (1)=IS2
156      20011 CONTINUE
157      C      SEE IF WE HAVE AN OUTPUT POINT THIS LINE
158      DO 20014 I=1,NT
159      K=IFXT(I)
160      IF (IFXV(I).EQ.(56-L)) LINE(K)=IS5
161      20014 CONTINUE
162      IF ((56-L).EQ.IY1) LINE(2)=IS3
163      IF ((56-L).EQ.IY2) LINE(70)=IS3
164      ICROSS=1H
165      LL=57-L
166      DO 21000 IJ=1,5
167      IF (LL.NE.(10*IJ+2)) GO TO 21000
168      IF ((56-L).EQ.IY1) ICROSS=1H+
169      VOLT=(LL-2)/10*YS
170      WRITE (6,62100) ICROSS,VOLT,(LINE(I),I=7,70)
171      GO TO 21001
172      21000 CONTINUE
173      IF ((L.EQ.1).AND.(LIY2.EQ.0)) LINE(1)=1HA
174      IF ((LIY2.EQ.1).AND.(L.EQ.1)) LINE(1TOPT)=1H+
175      WRITE (6,60020) (LINE(I),I=1,70)
176      21001 CONTINUE
177      60020 FORMAT (2X,70A1)
178      20020 CONTINUE
179      62100 FORMAT(2X,1H-,1A1,F5.1,64A1)
180      DO 20028 I=2,70
181      LINE (I)=IS2
182      20028 CONTINUE
183      LINE (1)=IS3
184      DO 20029 I=1,6
185      LINE(10*I+1)=IS4
186      20029 CONTINUE
187      LINE(70)=1H>
188      WRITE (6,60020) (LINE(I),I=1,70)
189      DO 20767 I=1,6
190      XSC(I)=I*XS
191      20767 CONTINUE
192      WRITE (6,60767) (XSC(I),I=1,6)
193      60767 FORMAT (4X,6(4X,F6.1),3X,5HHOURS)
194      WRITE (6,60050) T(ISQBST),RMMIN
195      C
196      C
197      C ADDITION 3-29-79 TO CALCULATE 110 VRMS LIFE
198      C CHGD TO 120 VRMS 6-05-79
199      C
200      C
201      LIFE=FLOAT((120.-RCMIN)*RMMIN)
202      WRITE (6,61882) LIFE
203      61882 FORMAT (/3X,47H PROJECTED LIFE AT 12 FTL SPOT BRIGHTNESS & 1:
204      & 8H VRMS IS, 15,6H HOURS////////)
205      WRITE (6,60123)
206      STOP
207      END

```

DRESSWELL\*6MWC(1).BLANKDATA

```

1  @HDS UPDATE
2  @USE YYY., PROGFIL*LAMPLOTS.
3  @XOT YYY.ABSOL
4  SAMPLE NUMBER
5  SAMPLE TYPE
6  OVEN NUMBER
7  BRIGHTNESS
8  FIGUPING BOOK REFERENCE
9  DATE FABRICATED
10 TEST AMBIENT
11 TEST TEMPERATURE
12 PURPOSE
13 PURPOSE
14 PURPOSE
15 PURPOSE
16 PURPOSE
17 BASE COAT WT
18 TOP COAT 1
19 TOP COAT 2
20 PHOSPHOR WEIGHT
21 SHEET RESISTANCE
22 DATE TIME HOURS BRIGHT VOLTS
23 **--**--** **.* 00.0 **.* 000.0
24 **--**--** **.* 000.0 **.* 000.0
25 **--**--** **.* 000.0 **.* 000.0
26 **--**--** **.* 000.0 **.* 000.0
27 **--**--** **.* 000.0 **.* 000.0
28 **--**--** **.* 000.0 **.* 000.0
29 **--**--** **.* 000.0 **.* 000.0
30 **--**--** **.* 000.0 **.* 000.0
31 **--**--** **.* 000.0 **.* 000.0
32 **--**--** **.* 000.0 **.* 000.0
33 **--**--** **.* 000.0 **.* 000.0
34 **--**--** **.* 000.0 **.* 000.0
35 **--**--** **.* 000.0 **.* 000.0
36 **--**--** **.* 000.0 **.* 000.0
37 **--**--** **.* 000.0 **.* 000.0
38 **--**--** **.* 000.0 **.* 000.0
39 **--**--** **.* 000.0 **.* 000.0
40 **--**--** **.* 000.0 **.* 000.0
41 **--**--** **.* 000.0 **.* 000.0
42 **--**--** **.* 000.0 **.* 000.0
43 **--**--** **.* 000.0 **.* 000.0
44 **--**--** **.* 000.0 **.* 000.0
45 **--**--** **.* 000.0 **.* 000.0
46 **--**--** **.* 000.0 **.* 000.0
47 **--**--** **.* 000.0 **.* 000.0
48 **--**--** **.* 000.0 **.* 000.0
49 **--**--** **.* 000.0 **.* 000.0
50 **--**--** **.* 000.0 **.* 000.0

```

The "blank" data file  
used for formatting the  
experimental data



```

CRESSWELL*6MWC(1).HEADING
1  OLD BLANKDATA
2  QUERY S SAMPLE NUMBER?
3  QUERY P SAMPLE TYPE?
4  QUERY O OVEN NUMBER?
5  QUERY R BRIGHTNESS?
6  QUERY F FIG. BOOK REF.?
7  QUERY D DATE FABRICATED?
8  QUERY Q AMBIENT?
9  QUERY X TEMPERATURE?
10 SET INS=' '
11 SET LLL=19-LEN('%SX%')
12 SET CCC=0
13 1234 SET INS=INS' '
14 SET CCC=CCC+1
15 JUMP 1234 IF CCC<LLL
16 C \VER\ER %INS%XS%\ 130
17 SET INS=' '
18 SET LLL=21-LEN('%PX%')
19 SET CCC=0
20 18 SET INS=INS' '
21 SET CCC=CCC+1
22 JUMP 18 IF CCC<LLL
23 C \PE\PE %INS%XP%\ 140
24 SET INS=' '
25 SET LLL=21-LEN('%DX%')
26 SET CCC=0
27 19 SET INS=INS' '
28 SET CCC=CCC+1
29 JUMP 19 IF CCC<LLL
30 C \VER\ER %INS%XY%\ 150
31 SET INS=' '
32 SET LLL=22-LEN('%BX%')
33 SET CCC=0
34 20 SET INS=INS' '
35 SET CCC=CCC+1
36 JUMP 20 IF CCC<LLL
37 C \SS\SS %INS%XY%\ 160
38 SET INS=' '
39 SET LLL=19-LEN('%FX%')
40 SET CCC=0
41 21 SET INS=INS' '
42 SET CCC=CCC+1
43 JUMP 21 IF CCC<LLL
44 C \CE\CE %INS%FX%\ 170
45 SET INS=' '
46 SET LLL=17-LEN('%DX%')
47 SET CCC=0
48 22 SET INS=INS' '
49 SET CCC=CCC+1
50 JUMP 22 IF CCC<LLL
51 C \ED\ED %INS%DX%\ 180
52 SET INS=' '
53 SET LLL=20-LEN('%LX%')
54 SET CCC=0
55 23 SET INS=INS' '
56 SET CCC=CCC+1
57 JUMP 23 IF CCC<LLL
58 C \NT\NT %INS%LX%\ 190
59 SET INS=' '
60 SET LLL=16-LEN('%XX%')
61 SET CCC=0
62 24 SET INS=INS' '
63 SET CCC=CCC+1
64 JUMP 24 IF CCC<LLL
65 C \RE\PE %INS%XXX%\ 200
66 QUERY A BASE COAT WEIGHT?
67 QUERY P FIRST TOP COAT WEIGHT?
68 QUERY C SECOND TOP COAT WEIGHT?
69 QUERY D PHOSPHOR WEIGHT?
70 QUERY S SHEET RESISTANCE?
71 SET INS=' '
72 SET LLL=17-LEN('%DX%')
73 SET CCC=0
74 99 SET INS=INS' '
75 SET CCC=CCC+1

```

The UNIVAC CTS subroutine  
used for opening a data  
file from BLANKDATA for  
a new phosphor lamp experiment

```

76      JUMP 99 IF CCC<LLL
77      C \HT\HT %INS%%D%\ 285
78      SET INS=' '
79      SET LLL=16-LEN('%E%')
80      SET CCC=0
81      100 SET INS=INS' '
82      SET CCC=CCC+1
83      JUMP 100 IF CCC<LLL
84      C \CE\CE %INS%%E%\ 286
85      SET INS=' '
86      SET LLL=20-LEN('%A%')
87      SET CCC=0
88      101 SET INS=INS' '
89      SET CCC=CCC+1
90      JUMP 101 IF CCC<LLL
91      C \WT\WT %INS%%A%\ 260
92      SET INS=' '
93      SET LLL=22-LEN('%B%')
94      SET CCC=0
95      102 SET INS=INS' '
96      SET CCC=CCC+1
97      JUMP 102 IF CCC<LLL
98      C \ 1\ 1 %INS%%B%\270
99      SET INS=' '
100     SET LLL=22-LEN('%C%')
101     SET CCC=0
102     103 SET INS=INS' '
103     SET CCC=CCC+1
104     JUMP 103 IF CCC<LLL
105     C \ 2\ 2 %INS%%C%\280
106     TYPE ' '
107     TYPE 'DONT FORGET TO SAVE WHEN YOU ARE FINISHED'
108     TYPE ' '

```

```

CRESSWELL*6MWC(1).E
1  TYPE ' '
2  TYPE 'NEXT EMPTY LINE IS...'
3  LOC '.*' 000.0' 300.900
4  5 REMARK CONTINUE FROM LINE 330
5  TYPE ' '
6  QUERY L LINE?
7  QUERY F HOURS?
8  QUERY G VOLTS?
9  SET X=%F%
10 SET Y=%G%
11 SET I=%L%
12 JUMP 7 IF I=300
13 JUMP 1 IF X>99.99
14 JUMP 2 IF Y>99.99
15 REMARK BOTH ARE LESS THAN 100
16 C /000.0 ***. 000.0/ %F% ***. %G% / %L%
17 JUMP 6
18 1 JUMP 3 IF Y>99.99
19 REMARK ONLY X IS GREATER THAN 100
20 C /000.0 ***. 000.0/ %F% ***. %G% / %L%
21 JUMP 9 IF X<1000.0
22 REMARK X IS > 1000
23 C /.** /.**/ %L%
24 9 REMARK END CASE X>1000
25 JUMP 6
26 2 REMARK ONLY Y IS GREATER
27 C /000.0 ***. 000.0/ %F% ***. %G% / %L%
28 JUMP 6
29 3 REMARK BOTH > 100
30 C /000.0 ***. 000.0/ %F% ***. %G% / %L%
31 JUMP 8 IF X<1000.0
32 REMARK X IS > 1000
33 C /.** /.**/ %L%
34 8 REMARK END CASE X>1000
35 JUMP 6
36 7 REMARK SPECIAL CASE FOR LINE 300
37 REMARK THIS ONLY WORKS WHEN LIGHT UP VOLTS
38 REMARK ARE LESS THAN 100
39 C /000.0/ %G% / %L%
40 6 REMARK OFFER TO CONTINUE
41 QUERY J DO YOU HAVE ANOTHER LINE?
42 BRANCH %J%, 'YES', 'NO'(5,55)
43 55 REMARK NO MORE DATA
44 TYPE ' '
45 TYPE 'DONT FORGET TO REP OR SAVE WHEN YOU ARE FINISHED'
46 TYPE ' '
47 TYPE '....CALLING DATE FOR YOU.....'
48 TYPE ' '
49 CALL DATE
50 RETURN

```

The UNIVAC CTS subroutine  
used for updating an  
existing data file

```

CRESSWELL*6MWC(1).U
1  QUERY H ENTER PURPOSE DATA FOR LINE 210
2  SET INS=' '
3  SET B=LEN('%H%')
4  SET B=15 - B/2
5  SET C=0
6  110 SET INS=INS' '
7  SET C=C+1
8  JUMP 110 IF C<B
9  C /SE/SE %INS%H%/210
10 QUERY H ENTER PURPOSE DATA FOR LINE 220
11 SET INS=' '
12 SET B=LEN('%H%')
13 SET B=15 - B/2
14 SET C=0
15 210 SET INS=INS' '
16 SET C=C+1
17 JUMP 210 IF C<B
18 C /SE/SE %INS%H%/220
19 QUERY H ENTER PURPOSE DATA FOR LINE 230
20 SET INS=' '
21 SET B=LEN('%H%')
22 SET B=15 - B/2
23 SET C=0
24 310 SET INS=INS' '
25 SET C=C+1
26 JUMP 310 IF C<B
27 C /SE/SE %INS%H%/230
28 QUERY H ENTER PURPOSE DATA FOR LINE 240
29 SET INS=' '
30 SET B=LEN('%H%')
31 SET B=15 - B/2
32 SET C=0
33 410 SET INS=INS' '
34 SET C=C+1
35 JUMP 410 IF C<B
36 C /SE/SE %INS%H%/240
37 QUERY H ENTER PURPOSE DATA FOR LINE 250
38 SET INS=' '
39 SET B=LEN('%H%')
40 SET B=15 - B/2
41 SET C=0
42 510 SET INS=INS' '
43 SET C=C+1
44 JUMP 510 IF C<B
45 C /SE/SE %INS%H%/250
46 RETURN

```

..RUEMM

The UNIVAC CTS subroutine  
used for entering the lamp  
description into the  
corresponding data file

```

CRESSWELL*6MWC(1).RJEMMT
1 SEND/PR501, WAIT
2 BASG, A PROGFI*LA*PLOTS.
3 BASG, A MWCRESSWELL*6MWC.
4 @USE M., M CRESSWELL*6MWC.
5 @USE P., PROGFI*LA*PLOTS.
6 @PPT, S P.PLOTFOR
7 @PPT, S M.BLANKDATA
8 @PPT, S M.576
9 @PPT, S M.HEADING
10 @PPT, S M.E
11 @PPT, S M.U
12 @PPT, S M.RJEMMT
13 @GO

```

The Remote Job Entry file  
used for generating this  
printout.

## APPENDIX II

# RISTON EQUIPMENT SYSTEMS

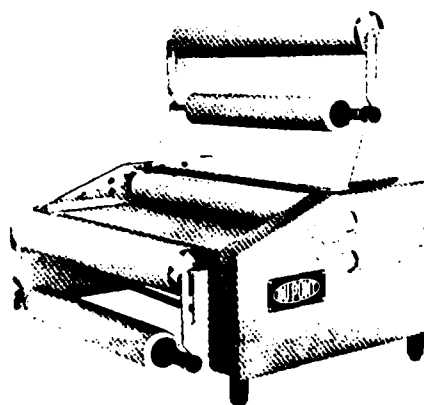
### A-24 LAMINATOR

RISTON I or RISTON II photopolymer film resist is applied to the clean surface of copper laminate with the RISTON A-24 Laminator. Using controlled heat and pressure, the A-24 Laminator automatically removes the polyolefin separator sheet and laminates the resist to the board surface.

An optional exhaust hood (LEH) may be mounted on the laminator directly over the heat shoe to provide positive removal of fumes generated in the normal operation with RISTON photopolymer film resists.

The A-24 Laminator is safe, efficient, and easy to operate. It accommodates RISTON film in widths to 24 inches and operates up to 13 fpm.

Dimensions	32.5"W x 23.5"L x 27.25"H
Weight	100 lb
Electrical	240/200V, 1 $\phi$ , 60/50 Hz, 15A
Laminating Speed	Variable to 13 fpm (60 Hz)
Panel Size	
Width	25" max
Laminating Width	24" max
Thickness	0.250" max
Recommended Work Space	3 ft on all sides



### FEATURES OF RISTON® A-24 LAMINATOR

- High thruput.
- Can be used with all types and thicknesses of RISTON® photopolymer film resist.
- Laminates both rigid and flexible substrates.
- Easy thread up; simple to use.
- Variable temperature and laminating speeds; controls conveniently located.
- Retrofit available to accommodate 1000-ft rolls.
- Optional exhaust hood for fume removal.

Du Pont's Series A-24 laminator is a machine designed for use with RISTON photopolymer film. The function of the laminator is to apply RISTON by means of heat and pressure to flexible or rigid materials up to 25 inches wide\* and up to 0.250 inches thick. Materials typically laminated with RISTON include copper-clad insulating boards used in the manufacture of printed circuits and sheets or rolls of metal for chemical machining. Resist can be applied to one or both sides of the working material in a single pass through the laminator (heat control is automatic).

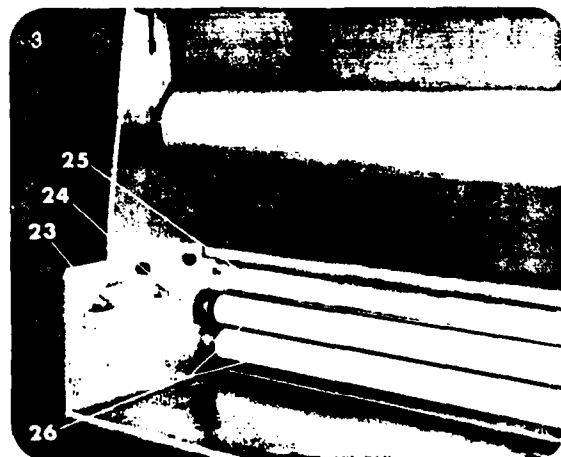
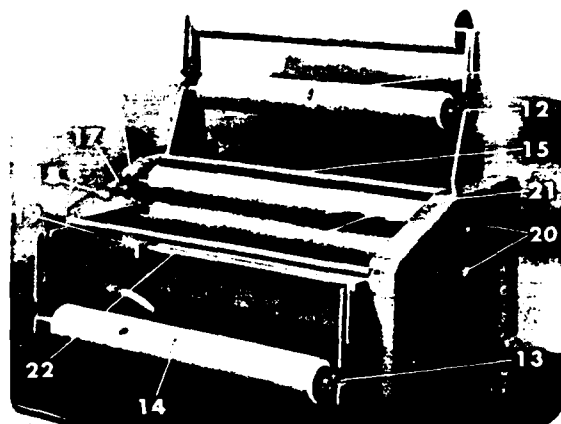
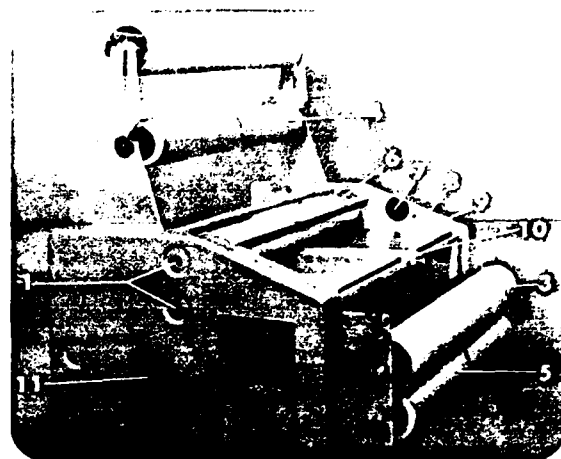
This manual contains essential information pertaining to the installation, operation and maintenance of the RISTON A-24 laminator. The manual should be reviewed carefully before the laminator is installed and operated.

The A-24 laminator has the following *general* characteristics:

Overall Dimensions —32½" W.x 23½" L.x 27¼" H.  
 Weight (approx.) —100 lbs.  
 Shipping Weight (approx.) —144 lbs.  
 Heater Capacity —3600 W  
 Maximum Panel Width —25"  
 Maximum Laminating Width —24"  
 Maximum Panel Thickness —0.250"  
 Speed Range —0 to 13 FPM  
 Working Range —5 to 8 FPM  
 Electrical Services  
     Required —200-240 V, 20A, 50-60 Hz  
 Principal controls and components for operation are shown in Photos 1 through 3.

\*Maximum film width 24 inches

- |                                    |                                |
|------------------------------------|--------------------------------|
| 1. Temperature Adjustment Controls | 12. Upper Tension Control Knob |
| 2. Upper Polyethylene Take Up Roll | 13. Lower Tension Control Knob |
| 3. Lower Polyethylene Take Up Roll | 14. Core Grippers              |
| 4. Upper RISTON Supply Mandrel     | 15. Upper Idler Roll           |
| 5. Lower RISTON Supply Mandrel     | 16. Red Heat Indicating Lights |
| 6. Shield for Top Heat Shoe        | 17. Heat Switch                |
| 7. Speed Control                   | 18. White Indicating Light     |
| 8. Motor Switch (Main)             | 19. Serial Number Plate        |
| 9. Feed Table                      | 20. Thermometers               |
| 10. Feed Guide Bar                 | 21. Heat Shoes                 |
| 11. Pressure Gap Adjustable Knob   | 22. Lower Idler Roll           |
|                                    | 23. Momentary Switch           |
|                                    | 24. Direction Switch           |
|                                    | 25. Top Idler Roll             |
|                                    | 26. Laminating Rolls           |



## **RISTON PRODUCTS SYSTEM AND THE RESISTS**

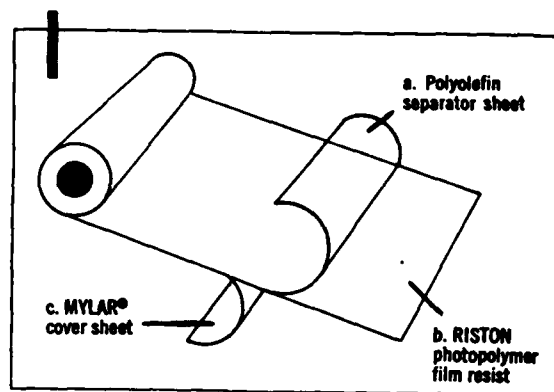
### **DESCRIPTION OF SYSTEM**

The RISTON System is a unique method of applying a film of photoresist onto a substrate for the production of printed circuits. Developed and patented by Du Pont, this system can make circuit board production easier, faster, and more economical than by most other methods. Although designed for manufacture of printed circuitry, the RISTON System is successfully employed in many other applications, including photofabrication, electroforming, and chemical machining.

The RISTON Products System is composed of three parts:

1. Resist
2. Laminator
3. Processor

### **RISTON PHOTOPOLYMER FILM RESIST**



RISTON photopolymer film resist is sandwiched between 1-mil layers of polyolefin and MYLAR. The polyolefin is a separator sheet which is automatically removed as resist is laminated to the board. The MYLAR protects the resist layer from damage by handling or contamination. It is peeled off just before development.

Exposure is by ultraviolet light. Where struck by UV, the resist is polymerized (hardened) and insolubilized to the developer. Imaged resist areas are revealed when unexposed portions are washed away during development.

RISTON photopolymer film resist is available in rolls of specified continuous lengths and in widths from 3 to 24 inches in 1/4-inch increments. A variety of types of RISTON, differing in thickness and formulation, fulfill the various end user requirements. Product characteristics of the various types are given in Data Sheets at the end of this volume. Your RISTON Technical Representative can help you select the types which best fulfill your needs.





# RISTON\*

## TECHNICAL DATA

### TYPE X113 S PHOTOPOLYMER FILM RESIST

RISTON Type X113 S is a solvent-processable dry film photopolymer resist combining good photospeed with wide latitude. It is tough and flexible, and has broad utility in print and etch and pattern plating applications.

Type X113 S is a blue, negative-working film  $1.40 \pm 0.1$  mils thick, sandwiched between 1-mil layers of MYLAR\* and polyolefin. The film lightens on exposure to ultraviolet radiation, producing a printout image.

#### Board Preparation

Recommended procedures for copper boards:

- Automatic pumice-slurry machines
- Pumice – hand scrub
- Wet "Scotch-Brite" or "Brushlon" brushes

#### Lamination

Laminate at  $230 \pm 10^\circ\text{F.}$ , 4-6 fpm on Du Pont **A-24** Laminator or

Laminate at  $210 \pm 10^\circ\text{F.}$ , 4-6 fpm on Du Pont HRL-24 Laminator.

No hold time required after lamination. Exposure can be made as soon as the board cools to room temperature.

#### Exposure

Exposure time required to yield the proper degree of polymerization is a function of the type and intensity of the light source as well as the type of artwork used; therefore, exposure times must be determined empirically for each unit. Density tablets provide a convenient means for establishing optimum exposure conditions. These recommendations are intended as guides and should be verified by trial runs through the entire process.

#### TYPICAL STEPS HELD ON DENSITY TABLETS

##### Alongside or Without Phototool

RISTON  
17 Step

$\sqrt[6]{2}$

8 – 14

Stouffer  
21 Step

$\sqrt{2}$

6 – 9

##### Under The Phototool (Preferred Procedure)

6 – 12

6 – 8

## Type X113 S

### Typical Exposures

Unit	Exposure
"Scanex" II (2" collimator)	30 - 35 sec
"DMVL" - HP	20 - 25 sec
Chemcut Pacer III	10 - 15 sec
Conex 4000	4 - 6 fpm

FOR BEST RESULTS, HOLD 15 MINUTES  
AFTER EXPOSURE BEFORE DEVELOPMENT.

### Development

RISTON Type X113 S develops in stabilized 1,1,1-trichloroethane at 60-70°F. When properly exposed, the film has wide development latitude (2-3X).

### Development Guidelines

Processor	Development
"A"	45 sec
"C"	50 sec (6-7 fpm)

### Etching

RISTON Type X113 S is compatible with common etchants including ferric chloride, ammonium persulfate, chromic-sulfuric acid, cupric chloride and the alkaline types. It is ready to etch after development.

### Plating

RISTON Type X113 S can be used for pattern plating of all metals common to the printed circuit industry. To obtain good adhesion between the laminate copper and the plated metals, the boards must be cleaned by standard preplate cleaning techniques such as those described in the RISTON Technical Manual.

### Stripping

RISTON Type X113 S strips rapidly and cleanly in any of the standard methylene chloride-based solvents commonly used for dry film photoresists.

Du Pont CS-24 Conveyorized Stripper      5-7 fpm

## SAFE HANDLING PROCEDURES

### Flammability

RISTON photopolymer resist supports combustion but is not highly flammable. A single sheet with large surface exposed to air will burn readily when ignited; a roll of film burns slowly and melts.

RISTON photopolymer resist has little inorganic content. Combustion products are primarily carbon dioxide, carbon monoxide, and water. With less than "ideal" combustion, the resist will burn with the generation of considerable quantities of smoke and soot.

**Safe Handling of RISTON X113 S**

The unexposed photoresist layer contains chemicals which can cause a skin irritation or sensitization reaction in some individuals, and contact with the unexposed photoresist should be avoided. Since the product is structured with the photoresist layer protected on both sides by the carrier and cover films, the need to handle the unexposed photoresist is eliminated.

In use, RISTON photopolymer resist is laminated with heat (approximately 230°F.) and pressure to the substrate. Lamination temperature and speed can be controlled to avoid volatilization of resist components. As a precaution, however, the lamination room should be well ventilated or an exhaust hood placed over the laminator.

In the development process, the unexposed photoresist is washed away with 1,1,1-trichloroethane. This is one of the least toxic chlorinated solvents, but care must be taken to observe the maximum allowable concentrations in the atmosphere. Typically, a figure of 350 ppm in air is quoted for 1,1,1-trichloroethane as the maximum allowable concentration for an 8-hour period.

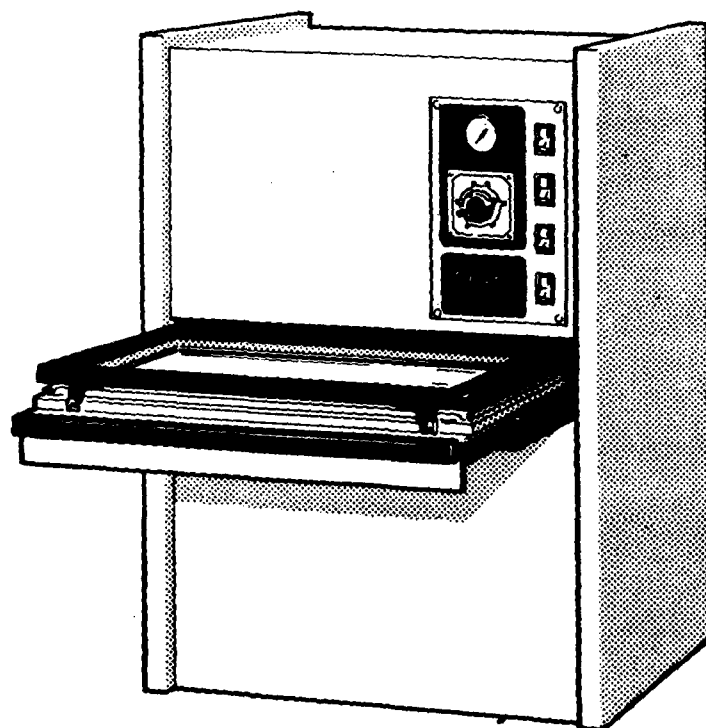
(Additional information on safe handling of RISTON may be found in Du Pont data sheet A-96650, "Handling Procedures for RISTON Photopolymer Film Resist." Request a copy from your RISTON Technical Representative.)

**General Safety Procedures**

- Wash hands before eating, smoking, or after any contact with unexposed RISTON or development and stripping solvents.
- Do not reuse either the separator or cover sheet for any purpose, because they may contain trace amounts of chemical irritants.
- Wear safety glasses or goggles when developing, etching, plating, or stripping the resist.
- Rings, bracelets, or watch bands should not be worn by operators. Solvent may be trapped in contact with the skin.
- Chlorinated solvents decompose to toxic or corrosive substances at high temperatures. Do not smoke or place hot objects near solvent. If welding or soldering is to be done on a RISTON Processor, the 1,1,1-trichloroethane should be completely drained and the equipment allowed to dry before work is begun.
- To minimize contact with chlorinated solvents, wear gloves made of, or impregnated with, polyvinyl alcohol or neoprene (not rubber).
- Developing areas should be well ventilated. Room air should be monitored periodically to check that solvent fumes remain below maximum allowable concentrations.
- Do not remove parts, tamper with interlocks, or make repairs to the equipment with power on. Running equipment should be attended.

APPENDIX III

**MODEL M-218**  
**DOUBLE SIDED EXPOSURE FRAME**



**INSTALLATION, OPERATION AND MAINTENANCE INSTRUCTIONS**

**Colight, Inc.**

123 North Third Street • Minneapolis, Minn. 55401

## SPECIFICATIONS

EXPOSURE AREA . . . . .	12 x 18, double-sided
ELECTRICAL REQUIREMENTS . .	220 volts, 60 hz, 15 amp, 1 phase
LAMPS . . . . .	(2) 400 watt, air cooled, mercury vapor
LAMP LIFE . . . . .	5,000 hours
VACUUM PUMP . . . . .	Rotary, 4.0 CFM, 1/3 H.P., oilless
EXPOSURE REGULATION . . . .	Reset timer 0-5 min., 15 sec. graduations
EXHAUST BLOWER . . . . .	350 CFM (free air)
CABINET SIZE . . . . .	Width 24", depth 22", height 34"
SHIPPING WEIGHT . . . . .	220 lbs.

\*\*\*\*\*

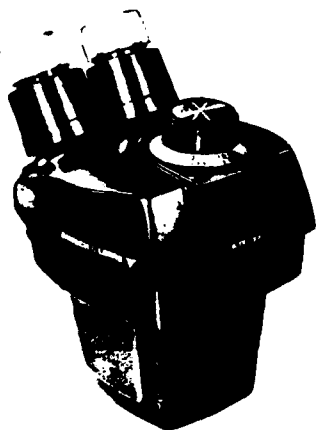
## FEATURES AND THEIR FUNCTIONS

1. Automatic exposure - Start exposure cycle and exposure stops automatically at the precise set time.
2. Automatic reset timer - Timer will automatically repeat the set time for subsequent exposures without resetting the timer.
3. Fused main power switch - Prevents electrical damage to all electrical components.
4. Air cooling system - Keeps the exposure frame and unit cool.
5. Mercury vapor lamp - Provides cool, clean, fast exposures.

# POWER PODS

The "Power Pod" concept of B&L StereoZoom microscopes provides complete flexibility in choice of equipment, at the time of purchase and at any later date. All optical elements are sealed into a compact unit (pod) that can be mounted onto any of the eight stands and arms offered with this series. Pods are completely and easily interchangeable among all stands. This is an important economical feature in those applications where viewing requirements differ from time to time, and where different stands are required.

## STEREOZOOM SERIES



### StereoZoom .7 × to 3 × Power Pod

Provides continuous magnification, always in sharp focus, in zoom ranges from 3.5 × to 198 ×. Pod may be turned 180° on any stand to provide conventional or reversed eyepiece orientation. Eyepieces are inclined 30° from vertical and are synchro-gearred for symmetrical separation. Accepts 10 ×, 15 ×, 20 × and 33 × eyepieces, and .5 × and 2 × supplementary lens attachments.

Catalog No. 31-26-94\*



### StereoZoom 1 × to 2.5 × Power Pod

Provides continuous magnification, always in sharp focus, in zoom ranges from 5 × to 165 ×. Pod may be turned 180° on any stand to provide conventional or reversed eyepiece orientation. Eyepieces are inclined 30° from vertical and are synchro-gearred for symmetrical separation. Accepts 10 ×, 15 ×, 20 × and 33 × eyepieces, and .5 × and 2 × supplementary lens attachments.

Catalog No. 31-26-93\*

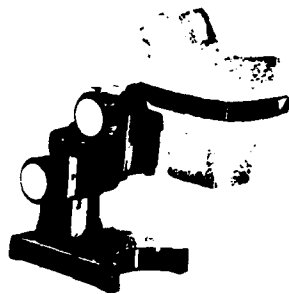


### Stereomicroscope 1 × and 2 × Fixed Magnification Power Pods

These Power Pods have magnifications from 5 × to 66 × and 10 × to 132 × respectively. Pods may be turned 180° on any stand to provide conventional or reversed eyepiece orientation. Eyepieces are inclined 30° from vertical and are synchro-gearred for symmetrical separation. Accepts 10 ×, 15 ×, 20 × and 33 × eyepieces, and .5 × and 2 × supplementary lens attachments.

Catalog No. 31-26-91\* 1 × Fixed Power Pod

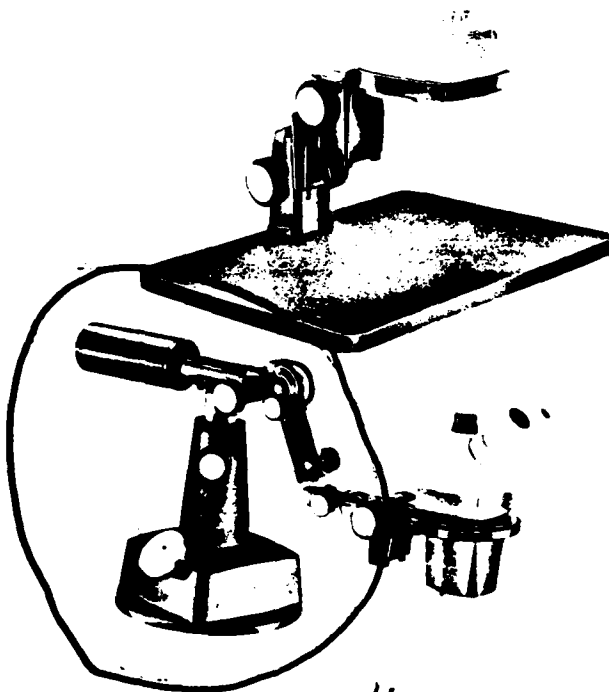
31-26-92\* 2 × Fixed Power Pod



## K Stand

Features two focusing ranges with the E or ER Arm. Either arm can be swiveled and inclined on its optical axis. The K Stand has a heavy, recessed cast base. Its extra long focusing range and wide range of adjustable positions make this stand well suited for industrial use. Requires the E or ER Arm.

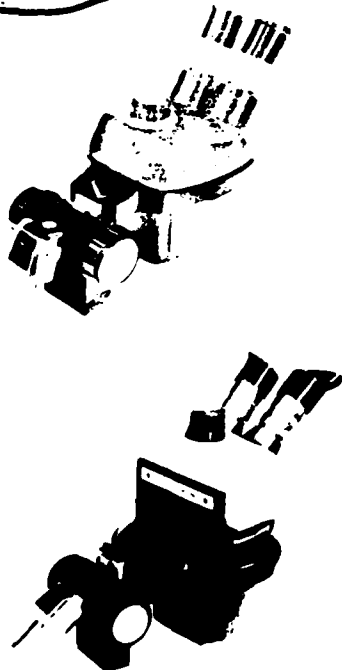
**Catalog Number 31-26-95 K Stand only**  
**31-26-59 E Arm (stationary)**  
**31-26-90 ER Arm (rotatable)**



## KT Stand

Similar to K Stand but with 12" x 16" composition base-board. For examination of large opaque objects. Requires the E or ER Arm.

**Catalog Number 31-26-65 KT Stand only**  
**31-26-59 E Arm (stationary)**  
**31-26-90 ER Arm (rotatable)**



## SK Stand

Permits examination of opaque objects in any plane. Provides maximum flexibility of shaft movement and adjustment. Horizontal motion has rack and pinion drive; vertical column has bevel and jack screw drive for accurately positioning pod. Requires either E or ER Arm.

**Catalog Number 31-26-97 SK Stand**  
**31-26-59 E Arm (stationary)**  
**31-26-90 ER Arm (rotatable)**

## E Arm

Designed to hold the Power Pod on machines or in special applications, as well as for use with S, SK, K and KT Stands. Arm can be inclined through 180° and pivoted through 360°. It contains its own focusing slide block. Mount it anywhere; it is highly suitable for equipment manufacturing and inspecting of electronic parts. Contains an illuminator port near the mounting bracket.

**Catalog Number 31-26-59 E Arm only**

## ER Arm

Similar to the E Arm, but with a ring that permits 360° rotation of the Power Pod. It does not contain an illuminator port, but permits illuminator linkage to be attached to underside of pod.

**Catalog Number 31-26-90 ER Arm only**

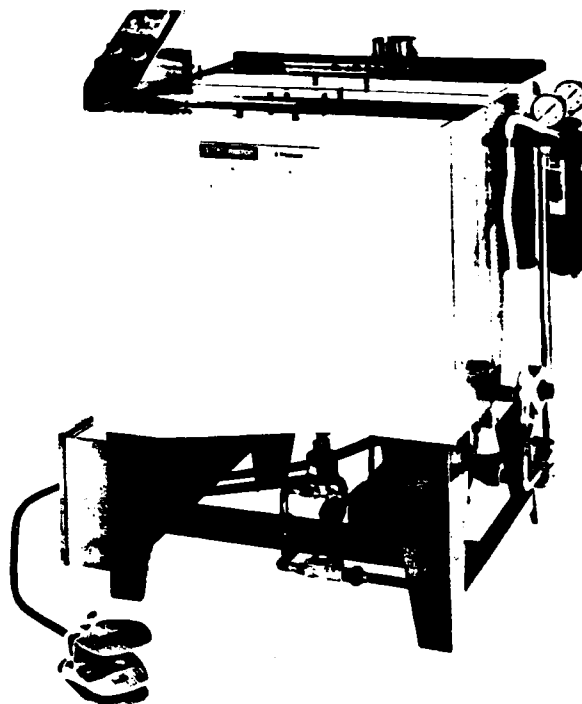
## APPENDIX IV

# RISTON EQUIPMENT SYSTEMS

## A-24 PROCESSOR

The RISTON A-24 Processor is designed for developing RISTON photopolymer film resists. It has three sections: spray developing chamber, solvent rinse tank, and spray-water rinse chamber. It can handle panels up to 19" x 24" with resist patterns to 18" x 20".

Dimensions	37.75"W x 32.75"L x 37"H
Weight	300 lb (empty); 425 lb (crated)
Electric Options	115V, 1 $\phi$ , 60 Hz, 20A 230V, 1 $\phi$ , 50 Hz, 10A
Water**	
Rinse	3 gpm at 30 psig, 80°F max
Cooling***	1 gpm at 30 psig, 60°F max
Drain	Gravity flow
Exhaust Air	100–150 cfm (plant)
Developer Capacity	14 gal
Panel Size	19" x 24" max
Developing Area	18" x 20" max
Development	Timer controlled
Recommended Work Space	3 ft on all sides
**Potable quality	
***If cooling water cannot be maintained below 60°F a chiller is recommended. The A-24 Processor heat output is about 3000 Btu.	



## FEATURES OF THE RISTON® A-24 PROCESSOR

- Consistent development provided by cooling coils which maintain developer temperature when adequate cooling media is used.
- Conveniently located gauges for monitoring spray pressures.
- Integral clean solvent dip chamber to provide for residue-free boards.
- Built-in spray water rinse.
- Accurate development time controlled by programmable timer.
- Corrosion resistant stainless steel construction.
- Simplified recharging due to pump-out feature.
- Accessible components for easy service and filter changing.
- Exhaust plenum for connection to plant exhaust for fume removal.
- Safety interlock on spray pump circuit.



### ACKNOWLEDGEMENTS

In the course of the MM&TE program a rather large number of people were involved in the many technical tasks, in various supporting services, in planning and administrative activities, management of the program, program monitoring, and in various aspects of communications. The present authors are those charged with preparation of the report, and do not include all principals. Among the other program contributors, most noteworthy are T. P. Brody who was department or program manager during most of the period, D. H. Davies who was directly involved in program planning and management in the early phases but who left Westinghouse to join Data Screen Corp. (now Kylex, Inc.), and M. Green of the Westinghouse Industrial and Government Tube Division (IGTD) in Horseheads, N.Y., who was program manager in 1976-1977 and IGTD/R&D Center liaison throughout the program period.

At Westinghouse R&D Center, Dr. T. P. Brody was responsible for proposing the work reported herein and for giving overall supervision to the program; he was Program Manager of the Westinghouse Thin Film Display Program, which included the MM&TE effort, from December 1977 to October, 1978. Over the years, Dr. Brody pioneered in many aspects of thin film transistors (TFTs) - in fabrication methods, investigations of materials and geometries, and in experiments for a wide range of applications of these evaporated film transistors. During the past ten years he has forcefully pursued the incorporation of TFTs in the display matrix of flat panel displays to improve and simplify display addressing and powering. As a result, there have been laboratory-made active matrix electroluminescent and liquid crystal displays possessing very superior characteristics and which yet have not been duplicated in any other laboratory in the world. This proof of an "existence theorem" for TFT active matrix flat panel displays has profound value as the foundation for a whole new flat panel display technology. Many believe that in the foreseeable future, say, the next ten to fifteen years, it will not only displace CRTs in most applications but will also give rise to a large number of new uses in the electronic office, teleconferencing

installations, word-processing typewriters, and eventually in TV communications systems and computerized terminals in the home. Dr. Brody has left Westinghouse Electric Corporation to form Panelvision, Inc., a small independent company, to develop a full manufacturing capability for displays of this kind, under Westinghouse license. His former associates express their appreciation and gratitude to him for introducing them to an exciting technology, and wish him success in his small business endeavor.

The authors wish to acknowledge important contributions to this program of other engineers in the Thin Film Device/Technology department, including J. A. Asars, S. D. Burkholder\*, Z. K. Kun, A. M. Lewis\*, F. C. Luo\*, J. X. Przybysz, and H. Y. Wey\*. They especially wish to thank department technicians involved in the program, all of whom showed sincere dedication to and enthusiasm for the effort; they include W. S. Escott, W. A. Hester, D. Leksell, G. Machiko, D. A. Riston\*, H. B. Shaffer, D. Yanda\*, and F. S. Youngk.

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Outside Westinghouse a most important contributor was the Towne Laboratories company which made the aperture masks used in the

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Essential motivation for the program was supplied by ERADCOM, U. S. Army, represented by E. Schlamm, principal contract monitor. All associated with the program are indebted to Dr. Schlamm for his sustained support and encouragement, and for his personal dedication to the active matrix display concept; his professional investment in this area has become a keystone in the building of this new flat display technology. Assisting him was R. Miller, who spent untold hours in monitoring and consulting activities. In addition, I. Reingold worked effectively for continued Army support of this and preceding programs, joining Dr. Schlamm in championing this display approach.

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from many authors and in editing and publishing it, have been gargantuan; the authors are deeply indebted to her for her dedicated and skillful efforts, her patient understanding and forbearance, and her cheerful optimism.

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